NOT RECOMMENDED FOR NEW DESIGNS

July 2014

SG6848x1
Low-Cost, Green-Mode PWM Controller for Flyback Converters

Features

- Green-Mode PWM Controller
- Low Startup Current: 5 µA
- Low Operating Current: 3 mA
- Programmable PWM Frequency
- Peak-Current-Mode Operation
- Leading-Edge Blanking
- Built-in Synchronized Slope Compensation
- Cycle-by-Cycle Current Limiting
- Constant Output Power Limit
- Gate Output Voltage Clamped at 15 V
- Small SSOT-6 Package

Applications

General-purpose switched-mode power supplies (SMPS) and flyback power converters, such as:

- Battery chargers for cellular phones, cordless phones, PDAs, digital cameras, and power tools
- Power adapters for ink jet printers, video game consoles, and portable audio players
- Open-frame SMPS for TV/DVD standby and auxiliary supplies, home appliances, and consumer electronics
- Replacements for linear transformers and RCC SMPS
- PC 5 V Standby Power

Description

This highly integrated PWM controller provides several enhancements to meet the low standby-power needs of low-power SMPS. To minimize standby power consumption, the proprietary Green Mode provides off-time modulation to continuously decrease PWM frequency under light-load conditions. Green Mode enables the power supply to meet even strict power conservation requirements.

The BiCMOS fabrication process enables reducing the startup current to 5 µA and the operating current to 3 mA. As a result, a large startup resistance can be used. Built-in synchronized slope compensation ensures the stability of peak-current-mode control. Proprietary internal compensation provides a constant output power limit over a universal AC input range (90 V_{AC} to 264 V_{AC}). Cycle-by-cycle current limiting ensures safe operation during short-circuits.

To protect the external power MOSFET from damage by supply over voltage, the SG6848X1 output driver is clamped at 15 V. The SG6848X1 controllers can be used to improve the performance and reduce the production cost of power supplies. The SG6848X1 can replace linear and RCC power supplies. It is available in DIP-8 and SSOT-6 packages.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
SG6848TZ1	-40 to +105°C	6-Lead, SUPERSOT™-6, JEDEC MO-193, 1.6 mm Wide	Tape & Reel
SG6848DZ1	-40 to +105°C	8-Lead, MDIP, JEDEC MS-001, .300" Wide, Two Dap	Tube
SG6848DY1	-40 to +105°C	8-Lead, MDIP, JEDEC MS-001, .300" Wide, Two Dap	Tube

Application Diagram

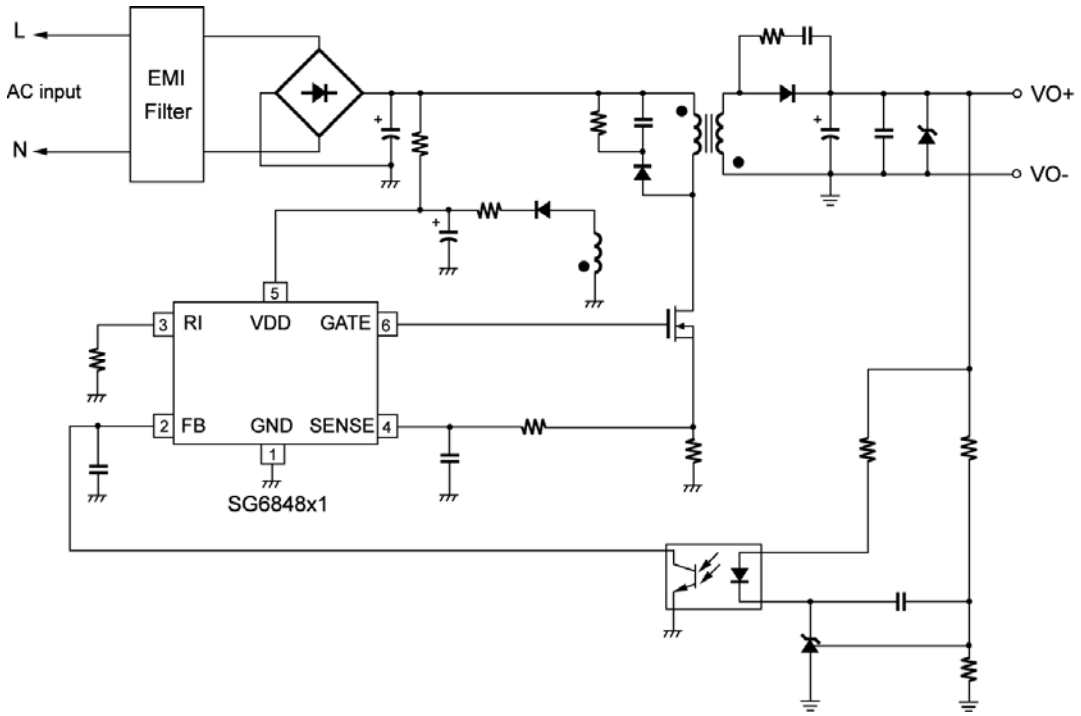


Figure 1. Typical Application

Internal Block Diagram

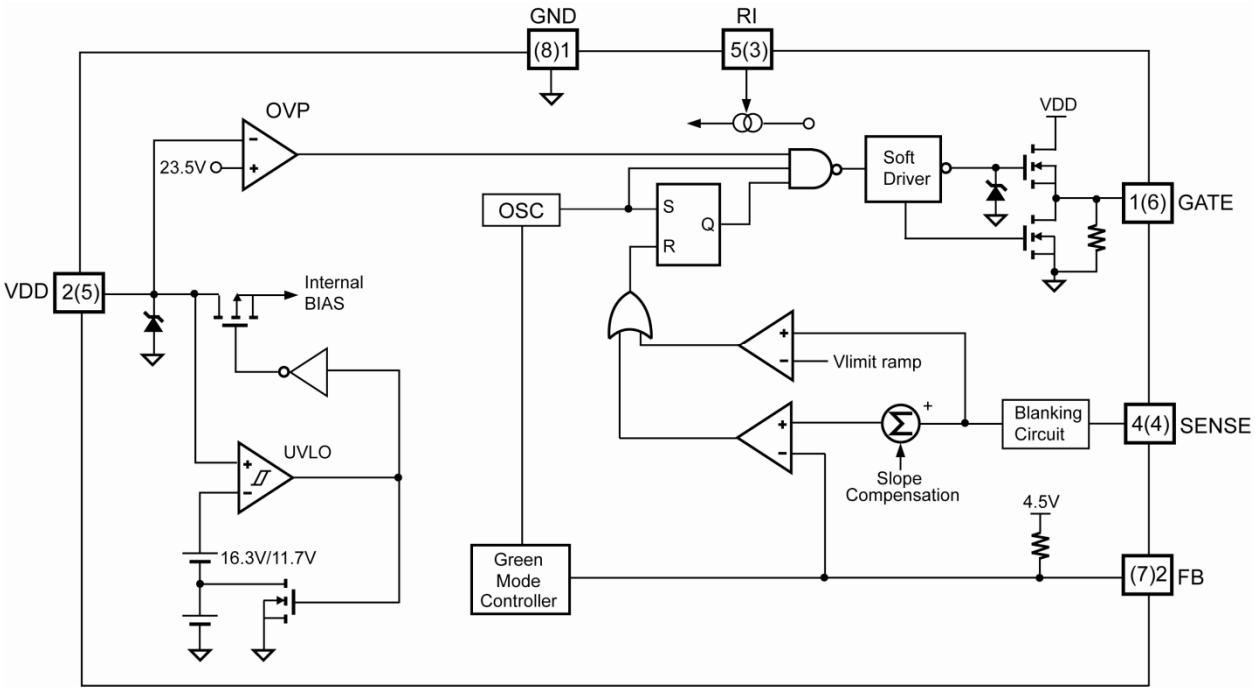
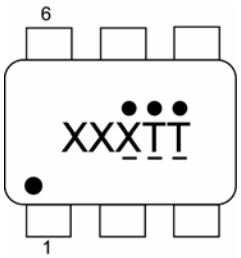


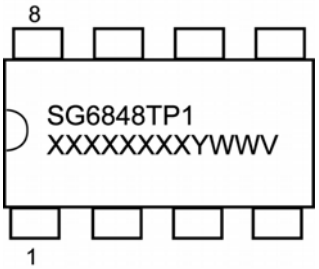
Figure 2. Functional Block Diagram

Marking Information



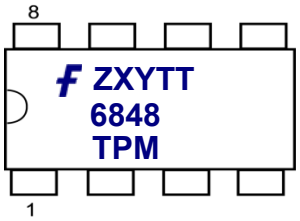
XXX: AAH=SG6848x1
TT : Die Run Code
. . . : Year Code
- - - : Week Code

*Marking for SG6848TZ1 (Pb-free)



T: D=DIP
P: Z= Lead Free + RoHS Compatible
Null=Regular Package
XXXXXXXX: Wafer Lot
Y: Year
WW: Week
V: Assembly Location

*Marking for SG6848DZ1 (Pb-free)



F- Fairchild Logo
Z- Plant Code
X- 1-Digit Year Code
Y- 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (D=DIP)
P: Z: Pb-free, Y: Green Package
M: Manufacture Flow Code

*Marking for SG6848DY1 (Green Compound)

Figure 3. Top Mark

Pin Configurations

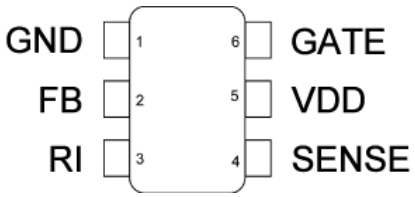


Figure 4. SSOT-6 Pin Configuration

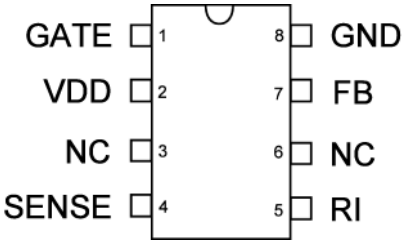


Figure 5. DIP-8 Pin Configuration

Pin Definitions

DIP Pin #	SSOT Pin #	Name	Description
1	6	GATE	The totem-pole output driver for driving the power MOSFET
2	5	VDD	Power supply
3		NC	No connection
4	4	SENSE	Current sense. This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled. This activates over-current protection. This pin also provides current amplitude information for current-mode control.
5	3	RI	A resistor connected from the RI pin to ground generates a constant current source used to charge an internal capacitor and determine the switching frequency. Increasing the resistance reduces the amplitude of the current source and the switching frequency. A 95 kΩ resistor, R_I, results in a 50 µA constant current, I_I, and a 70 kHz switching frequency.
6		NC	No connection
7	2	FB	Feedback. The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator, so that the PWM comparator can control the duty cycle.
8	1	GND	Ground

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{VDD}	DC Supply Voltage[1,2]			25	V
V_{FB}	Input Voltage to FB Pin		-0.3	6.0	V
V_{SENSE}	Input Voltage to Sense Pin		-0.3	6.0	V
T_J	Operating Junction Temperature			150	°C
Θ_{JA}	Thermal Resistance; Junction-to-Air	SSOT		208.4	°C/W
		DIP		82.5	°C/W
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature; Wave Soldering or IR, 10 Seconds			+260	°C
ESD	Human Body Model, JESD22-A114			3.0	kV
	Machine Model, JESD22-A115			300	V

Notes:
1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Electrical Characteristics

Unless otherwise noted, V_{DD}=15 V and T_A=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD-ON}	Turn-On Threshold Voltage		15.3	16.3	17.3	V
V_{DD-OFF}	Turn-Off Threshold Voltage		10.9	11.7	12.5	V
I_{DD-ST}	Startup Current	V_{DD}=15 V		5	30	µA
I_{DD-OP}	Operating Supply Current	V_{DD}=15 V, C_L=1 nF		3	5	mA
V_{DD-OVP}	Over Voltage Protection		22.0	23.5	25.0	V
Feedback Input Section						
Z_{FB}	Input Impedance			2		kΩ
I_{OZ}	Zero Duty Cycle Input Current			1.3	2.0	mA
V_{OP}	Open Loop Voltage			4.5		V
Current-Sense Section						
Z_{CS}	Input Impedance			10		kΩ
t_{PD}	Delay to Output			100		ns
V_{STHFL}	Flat Threshold Voltage for Current Limit			0.96		V
V_{STHVA}	Valley Threshold Voltage for Current Limit			0.81		V
t_{LEB}	Leading-Edge Blanking Time			200		ns
DC_{SAW}	Duty Cycle of SAW Limit			45		%
Oscillator Section						
f_{OSC}	Frequency	R_I=95 kΩ	65	70	75	kHz
f_{OSC-G}	Green-Mode Frequency	R_I=95 kΩ		15		kHz
I_N	Green-Mode Start Threshold FB Input Current			1		mA
I_G	Green-Mode Minimum Frequency FB Input Current			1.16		mA
S_G	Green-Mode Modulation Slope	R_I=95 kΩ		300		Hz/µA
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=14 to 20 V			2	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-30 to 105°C			2	%
Output Section						
DCY_{MAX}	Maximum Duty Cycle		70	75	80	%
DCY_{Min}	Minimum Duty Cycle			0		%
V_{GATE-L}	Output Voltage Low	V_{DD}=15 V, I_O=20 mA			1.5	V
V_{GATE-H}	Output Voltage High	V_{DD}=13.5 V, I_O=20 mA	8			V
t_r	Rising Time	V_{DD}=15 V, C_L=1 nF		250		ns
t_f	Falling Time	V_{DD}=15 V, C_L=1 nF		80		ns
$V_{GATE-CLAMP}$	Output Clamp Voltage	V_{DD}=20 V		15	17	V

Typical Performance Characteristics

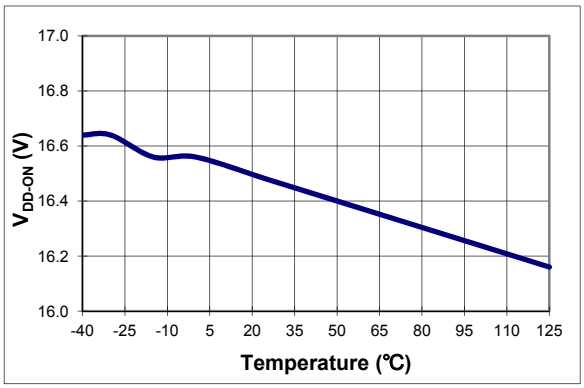


Figure 6. Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

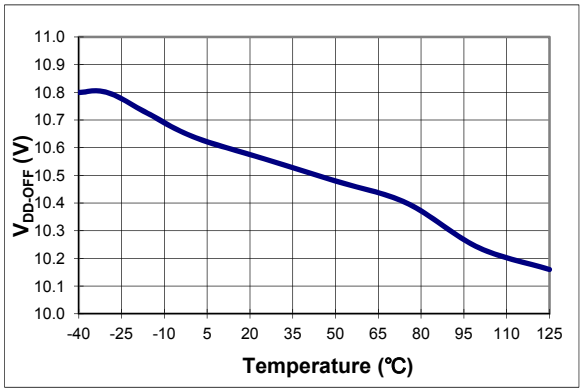


Figure 7. Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

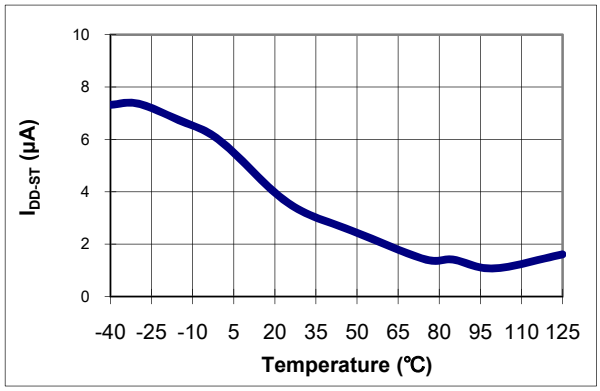


Figure 8. Startup Current (I_{DD-ST}) vs. Temperature

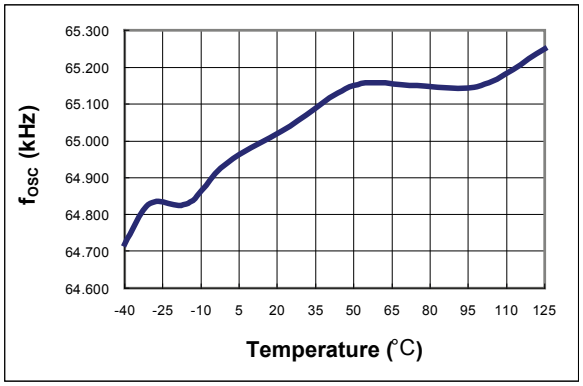


Figure 9. Center Frequency (f_{OSC}) vs. Temperature

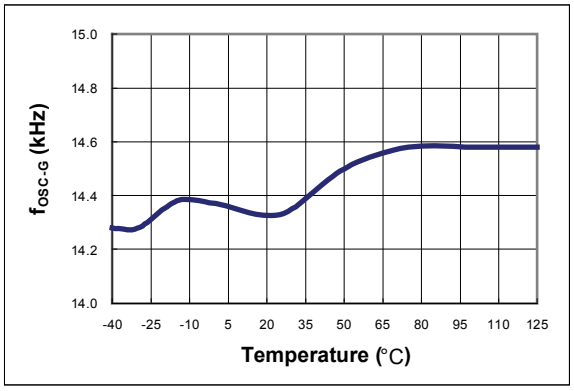


Figure 10. Green-Mode Frequency (f_{OSC-G}) vs. Temperature

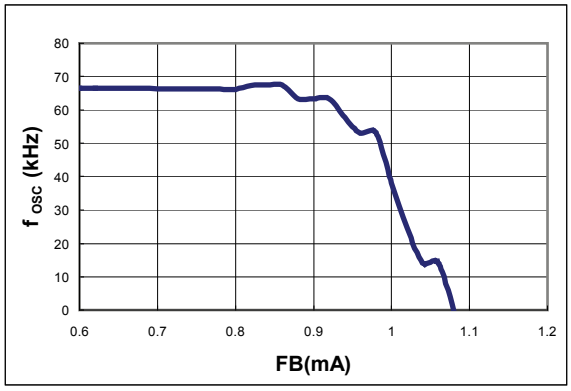


Figure 11. PWM Oscillator Frequency (f_{OSC}) vs. FB

Operation Description

The SG6848x1 devices integrate many useful functions into one controller for low-power switching mode power supplies. The following descriptions highlight some of the features.

Startup Current

The startup current is only 5 µA. Low startup current allows a startup resistor with a high resistance and a low-wattage to supply the startup power for the controller. A 1.5 MΩ, 0.25 W, startup resistor and a 10 µF/25 V V_{DD} hold-up capacitor are sufficient for an AC-to-DC power adapter with a wide input range (100 V_{AC} to 240 V_{AC}).

Operating Current

The operating current is reduced to 3 mA. The low operating current results in higher efficiency and reduces the V_{CC} hold-up capacitance requirement.

Green-Mode Operation

The proprietary Green Mode provides off-time modulation to linearly decrease the switching frequency under light-load conditions. On-time is limited to provide stronger protection against brownouts and other abnormal conditions. The feedback current, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback current exceeds the threshold current, the switching frequency starts to decrease. Green Mode dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using the SG6848X1 can meet even strict regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to ground generates a constant current source for the SG6848X1. This current is used to charge an internal capacitor. The charge-time determines the internal clock speed and the switching frequency. Increasing the resistance reduces the amplitude of the input current and reduces the switching frequency. A 95 kΩ R_I resistor results in a 50 µA constant current I_I and a 70 kHz switching frequency. The relationship between R_I and the switching frequency is:

$$f_{PWM} = \frac{6650}{R_I(k\Omega)}(kHz) \quad (1)$$

The range of the oscillation frequency is designed to be within 50 kHz ~ 100 kHz.

Leading-Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense-resistor. To avoid premature termination of the switching pulse, a 200 ns leading-edge blanking time is built in. Conventional RC filtering can be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Constant Output Power Limit

When the SENSE voltage across the sense resistor R_S reaches the threshold voltage (around 0.96 V), the output GATE drive is turned off after a short propagation delay, t_D. This delay introduces an additional current, proportional to t_D*V_{IN}/L_p. The propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltages result in larger additional currents. At high input line voltages, the output power limit is higher than at low input line voltages.

To compensate for this output power limit variation across a wide AC input range, the threshold voltage is adjusted by adding a positive ramp. This ramp signal rises from 0.81 V to 0.96 V, then flattens out at 0.96 V. A smaller threshold voltage forces the output GATE drive to terminate earlier. This reduces the total PWM turn-on time and makes the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for a wide AC input voltage range (90 V_{AC} to 264 V_{AC}).

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16.3 V and 11.7 V. During startup, the hold-up capacitor must be charged to 16.3 V through the startup resistor to enable the SG6848X1. The hold-up capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 11.7 V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 15 V Zener diode to protect power MOSFET transistors against undesired over-voltage gate signals.

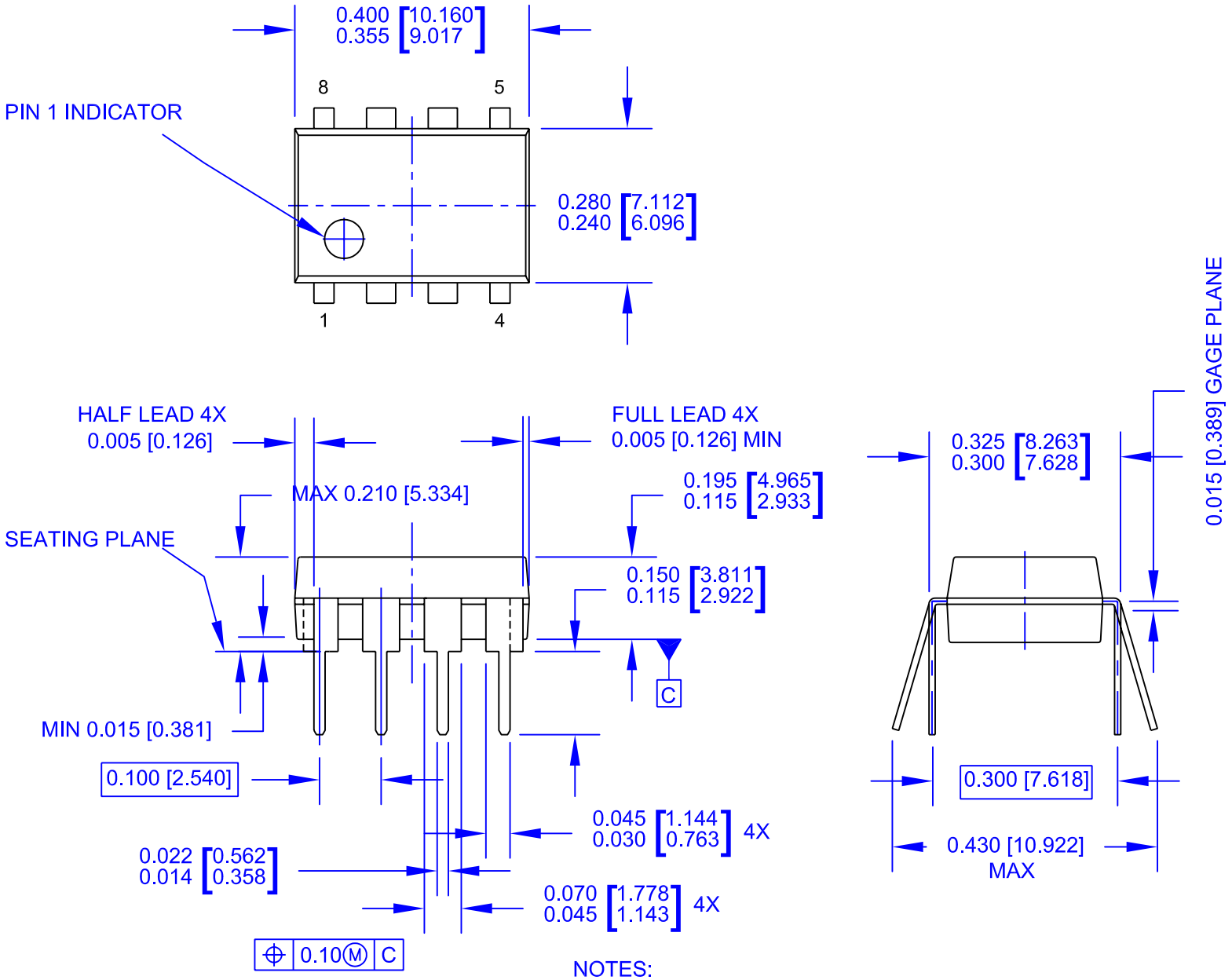
Built-In Slope Compensation

The sensed voltage across the current-sense resistor is used for current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillations due to peak-current mode control. A synchronized, positively-sloped ramp in each switching cycle is calculated as:

$$\frac{0.36 \times Duty}{Duty(max.)} \quad (2)$$

Noise Immunity

Noise from the current sense or control signal can cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps, but further precautions should be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the SG6848x1, and increasing the power MOS gate resistance are advised.



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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