64M Ver.B SPI NOR FLASH

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1. FEATURES

■ **SPI Flash Memory**
- 64M-bit / 8M–byte Serial Flash
- 256-bytes per programmable page
- 4K-bit secured OTP

■ **Standard, Dual or Quad SPI and QPI**
- Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
- Dual SPI: CLK, /CS, IO_0, IO $_1$, /WP, /Hold
- Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
- QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3

■ **High Performance**
- 133MHz clock operation
- 266MHz equivalent Dual SPI
- 532MHz equivalent Quad SPI
- 65MB/S continuous data transfer rate
- 40MB/S random access (32-byte fetch
- Comparable to X16 Parallel Flash

■ **Flexible Architecture**
- Uniform Sector Erase (4K-byte
- Block Erase (32K and 64K-bytes
- Erase/Program Suspend & Resume

■ **Endurance**
- 100K program/ erase cycles

■ **Low Power Consumption**
- Single 2.7 to 3.6V supply
- 5mA active current
- <3μA Deep Power-down (typ.

■ **wide Temperature Range**
- -40℃ to +85℃ operating range

■ **Advanced Security Features**
- Software and Hardware Write-protect
- Top or Bottom, Sector or Block selection
- Lock-Down and OTP protection
- Discoverable Parameters(SFDP Register

■ **Package Options**
- 8-pad WSON 6x5-mm
- 8-pin SOP 208-mil
- 8-pin TSSOP 173-mil
- 8-pin VSOP 208-mil
- 24-Ball TFBGA

■ **Package Material**
- Zetta all product Green package
  Lead-free & Halogen-free
  RoHS Compliant

2. GENERAL DESCRIPTION

The ZD25Q64B supports the standard Serial Peripheral Interface (SPI, and Quad Peripheral Interface (QPI: Serial Clock, Chip Select, Serial Data I/O0(DI, I/O1(DO, I/O2(/WP, and I/O3(/HOLD. SPI clock frequencies of up to 133MHz are supported allowing equivalent clock rates of 266MHz for Dual Output and 532MHz for Quad Output when using the QPI and Fast Read Dual/Quad I/O instructions.

The ZD25Q64B array is organized into 32,768 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instructions. Pages can be erased Sector, 32KB Block, 64KB Block or the entire chip.

The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 5mA active and 3μA for Deep Power-down. All devices offered in space-saving packages. The device supports JEDEC standard manufacturer and device identification with a 4K-bit Secured OTP.

3. PIN / PAD CONFIGURATION

3.1 8-Pin VSOP 208-MIL, SOP 208-MIL, TSSOP 173-MIL

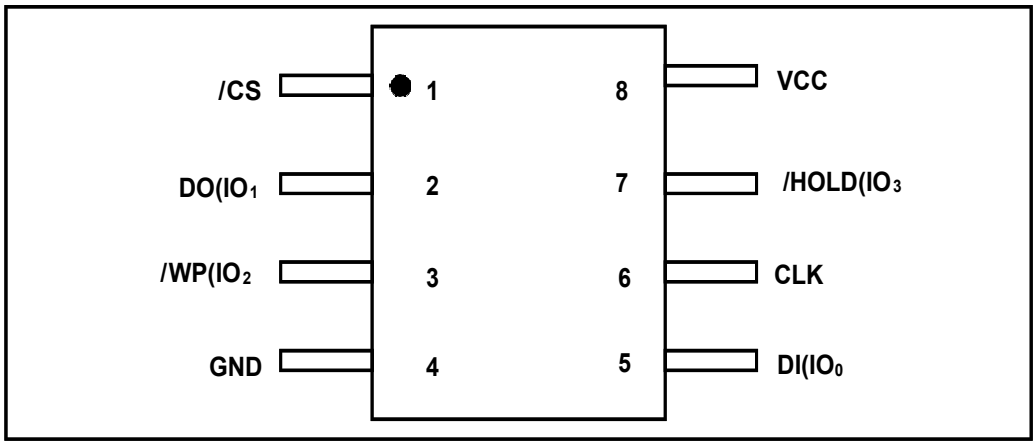


Figure 1a. Pin Assignments, 8-pin VSOP 208-mil, SOP 208-mil, TSSOP 173-mil

3.2 8-Pad WSON 6X5-MM, 8X6-MM

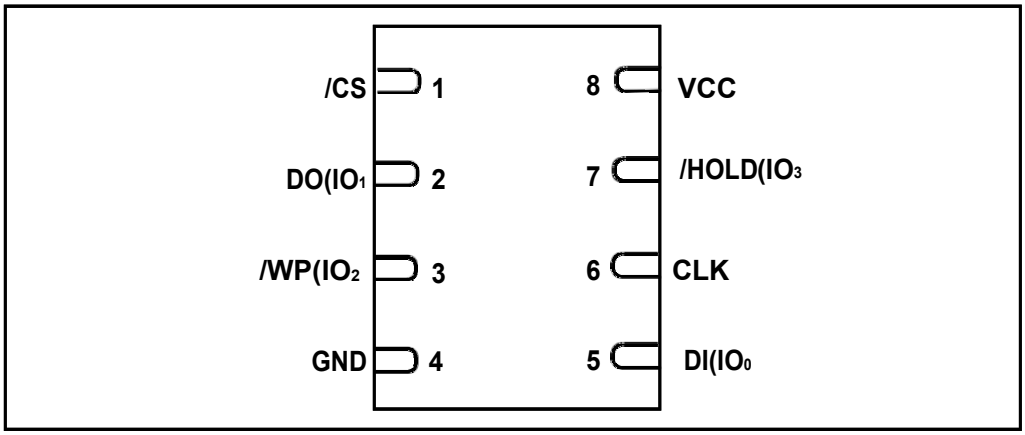


Figure 1b. Pad Assignments, 8-pad WSON

3.3 16-Pin SOP 300-MIL

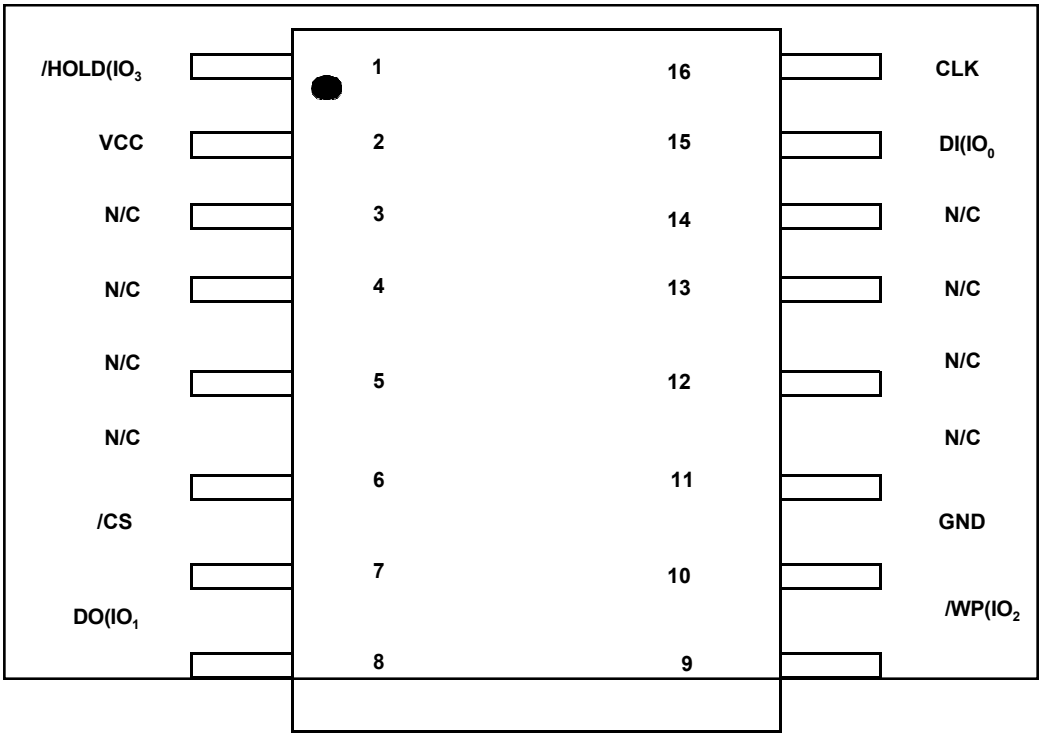
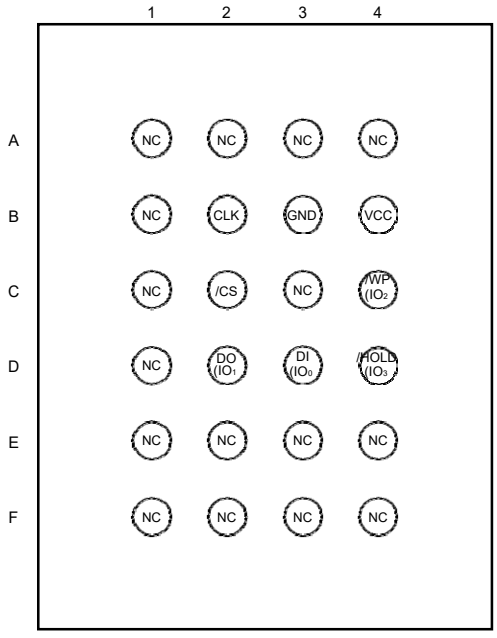


Figure 1c. Pin Assignments, 16-pin SOP 300-mil

3.4 24-Ball TFBGA



Top View

Figure 1d. Pin Assignments, 24-Ball TFBGA

4. PIN / PAD DESCRIPTION

4.1 VSOP 208-MIL, SOP 200-MIL, WSON 6X5-MM, WSON 8X6-MM, 24-Ball TFBGA

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO(IO1	I/O	Data Output (Data Input Output 1*¹
3	/WP(IO2	I/O	Write Protect Input (Data Input output 2*²
4	GND		Ground
5	DI(IO0	I/O	Data Input (Data Input Output 0*¹
6	CLK	I	Serial Clock Input
7	/HOLD(IO3	I/O	Hold Input (Data Input output 3*²
8	VCC		Power Supply

*1 IO0 and IO1 are used for Dual and Quad instructions

*2 IO0 – IO3 are used for Quad instructions

4.2 SOP 300-MIL

PAD NO.	PAD NAME	I/O	FUNCTION
1	/HOLD(IO3	I/O	Hold Input(Data Input Output 3* ²
2	VCC		Power Supply
3	N/C		No Connect
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO(IO1	I/O	Data output (Data Input Output 1* ¹
9	/WP(IO2	I/O	Write Protection Input / (Data Input Output 2* ²
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI(IO0	I/O	Data Input (Data Input Output 0* ¹
16	CLK	I	Serial Clock Input

*1 IO0 and IO1 are used for Dual and Quad instructions
*2 IO0_IO3 are used for Quad instructions

4.3 Package Type

ZD25Q64B is offered in an 8-pin plastic 208-mil width VSOP, 200-mil width SOP, 6x5-mm WSON, 8x6-mm WSON, 16-pin plastic 300-mil width SOP, 24-Ball TFBGA as shown in figure 1a, 1b, 1c and 1e respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

5. SIGNAL DESCRIPTION

5.1 Chip Select (/CS

When this input signal is high, the device is deselected and serial data output pins are at high impedance. Unless an internal program, erase or write status register cycle is in progress, the device will be in the standby power mode (this is not the deep power-down mode. Driving Chip Select (/CS low enables the device, placing it in the active power mode. After power-up, a falling edge on Chip Select (/CS is required prior to the start of any instruction.

5.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3

The ZD25Q64B supports standard SPI, Dual SPI, Quad SPI and QPI operation. Standard SPI instructions use the serial DI (input pin to write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK input pin. Standard SPI also uses the serial DO (output to read data or status from the device on the falling edge of CLK.

Dual, Quad SPI and QPI instructions use the serial IO pins to write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE in Status Register-2 to be set. When QE=1 the /WP pin becomes IO2 and /HOLD pin becomes IO3.

5.3 Write Protect (/WP

The Write Protect (/WP pin can be used to protect the Status Register against data modification. Used in company with the Status Register's Block Protect (SEC, TB, BP2, BP1 and BP0 bits and Status Register Protect (SRP bits, a portion or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin (Hardware Write Protect function is not available since this pin is used for IO2. See figure 1a, 1b and 1c for the pin configuration of Quad I/O and QPI operation.

5.4 HOLD (/HOLD

The /HOLD pin is used to pause any serial communications with the device without deselecting the device. When /HOLD goes low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care. When /HOLD goes high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set Quad I/O, the /HOLD pin function is not available since this pin used for IO3. See figure 1a, 1b and 1c for the pin configuration of Quad I/O and operation.

5.5 Serial Clock (CLK

This input signal provides the timing for the serial interface. Instructions, addresses, or data present at serial data input are latched on the rising edge of Serial Clock (CLK. Data are shifted out on the falling edge of the Serial Clock (CLK.

6.BLOCK DIAGRAM

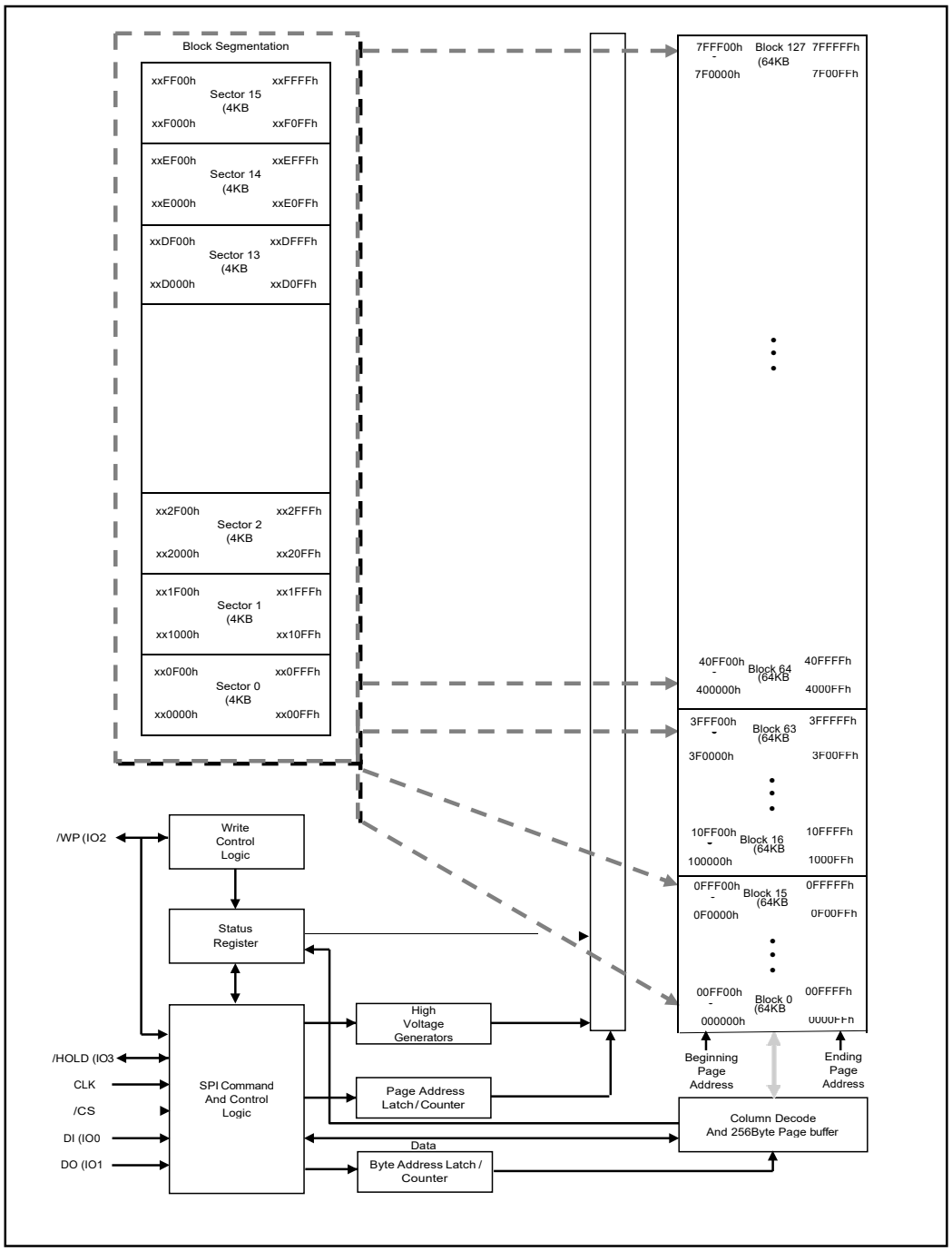


Figure 2. Block Diagram of ZD25Q64B

6. FUNCTIONAL DESCRIPTION

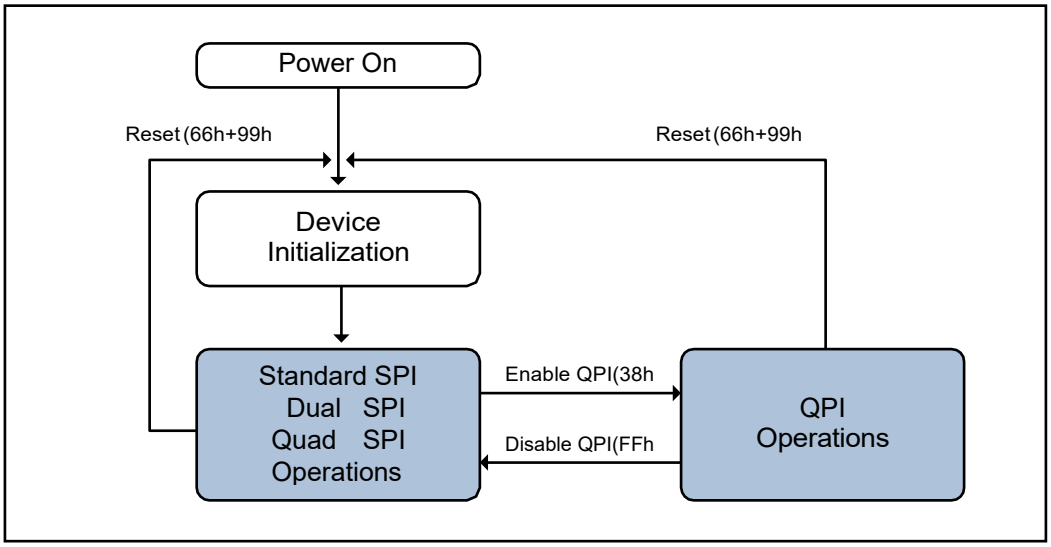


Figure 3. Operation Diagram of ZD25Q64B

6.1 Standard SPI Instructions

The ZD25Q64B features a serial peripheral interface on four signals: Serial Clock (CLK. Chip Select (/CS, Serial Data Input (DI and Serial Data Output (DO. Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Modes 0 (0, 0 and 3 (1, 1 are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3 the CLK signal is normally high on the falling and rising edges of /CS.

6.2 Dual SPI Instructions

The ZD25Q64B supports Dual SPI operation. This instruction allows data to be transferred to or from the device at two times the rate of the standard SPI. The Dual Read instruction is ideal for quickly downloading code to RAM upon power-up (code-shadowing or for executing non-speed-critical code directly from the SPI bus (XIP. When using Dual SPI instructions the DI and DO pins become bidirectional I/0 pins; IO0 and IO1.

6.3 Quad SPI Instructions

The ZD25Q64B supports Quad SPI operation. This instruction allows data to be transferred to or from the device at four times the rate of the standard SPI. The Quad Read instruction offers a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP. When using Quad SPI instruction the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE in Status Register-2 to be set.

6.4 QPI Function

The ZD25Q64B supports Quad Peripheral Interface (QPI operation when the device is switched from Standard/ Dual/ Quad SPI mode to QPI mode using the “Enable QPI (38h” instruction. To enable QPI mode, the non-volatile Quad Enable bit (QE in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See Figure 3 for the device operation modes.

The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/ Dual/ Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time, “Enable QPI” and “Disable QPI/ Disable QPI 2” instructions are used to switch between these two modes. Upon power-up or after software reset using “Reset (99h instruction, the default state of the device is Standard/ Dual/ Quad SPI mode.

6.5 Hold Function

The /HOLD pin is used to pause a serial sequence of the SPI flash memory without resetting the clocking sequence. To enable the /HOLD mode, the /CS must be in low state. The /HOLD mode effects on with the falling edge of the /HOLD signal with CLK being low. The HOLD mode ends on the rising edge of /HOLD signal with CLK being low.
In other words, /HOLD mode can’t be entered unless CLK is low at the falling edge of the /HOLD signal. And /HOLD mode can’t be exited unless CLK is low at the rising edge of the /HOLD signal. See Figure.4 for HOLD condition waveform.
If /CS is driven high during a HOLD condition, it resets the internal logic of the device. As long as /HOLD signal is low, the memory remains in the HOLD condition. To re-work communication with the device, /HOLD must go high, and /CS must go low. See 12.11 for HOLD timing.

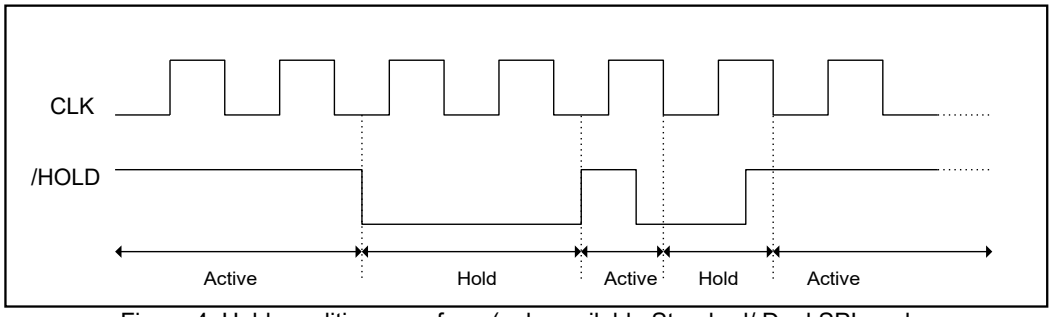


Figure 4. Hold condition waveform (only available Standard/ Dual SPI mode

7. WRITE PROTECTION

To protect inadvertent writes by the possible noise, several means of protection are applied to the Flash memory.

7.1 Write protect Features

- While Power-on reset, all operations are disabled and no instruction is recognized.
- An internal time delay of tPUW can protect the data against inadvertent changes while the power supply is outside the operating specification. This includes the Write Enable, Page program, Sector Erase, Block Erase, Chip Erase, Write Security Register and the Write Status Register instructions.
- For data changes, Write Enable instruction must be issued to set the Write Enable Latch (WEL bit to “0”. Power-up, Completion of Write Disable, Write Status Register, Page program, Sector Erase, Block Erase and Chip Erase are subjected to this condition.
- Using setting the Status Register protect (SRP and Block protect (SEC, TB, BP2, BP1, and BP0 bits a portion of memory can be configured as reading only called software protection.
- Write Protect (/WP pin can control to change the Status Register under hardware control.
- The Deep Power Down mode provides extra software protection from unexpected data changes as all instructions are ignored under this status except for Release Deep Power-down instruction.
- One time program(OTP mode provide protection mode from program/erase operation

8. STATUS REGISTER

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled the state of write protection and the Quad SPI setting. The Write Status Register instruction can be used to configure the devices writes protection features and Quad SPI setting. Write access to the Status Register is controlled by in some cases of the /WP pin.

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	SEC	TB	BP2	BP1	BP0	WEL	BUSY
Status Register Protect 0 (Non-Volatile	Sector Protect (Non-Volatile	Top/Bottom Write Protect (Non-Volatile	Block Protect (Non-Volatile	Block Protect (Non-Volatile	Block Protect (Non-Volatile	Write Enable Latch	Erase or Write in Progress

Figure 5a. Status Register-1

S15	S14	S13	S12	S11	S10	S9	S8
SUS	CMP	(R	(R	(R	(R	QE	SRP1
Suspend Status	Complement Protect (Non-Volatile	Reserved	Reserved	Reserved	Reserved	Quad Enable (Non-Volatile	Status Register Protect 1 (Non-Volatile

Figure 5b. Status Register-2

8.1 BUSY

BUSY is a read only bit in the status register (S0 that is set to a 1 state when the device is executing a Page Program, Erase, Write Status Register or Write Security Register instruction. During this time the device will ignore further instruction except for the Read Status Register and Erase / Program Suspend instruction (see tW, tPP, tSE, tBE1, tBE2 and tCE in AC Characteristics. When the Program, Erase, Write Status Register or Write Security Register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.2 Write Enable Latch (WEL

Write Enable Latch (WEL is a read only bit in the status register (S1 that is set to a 1 after executing a Write Enable instruction. The WEL status bit is cleared to a 0 when device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Erase and Write Status Register.

8.3 Block Protect Bits (BP2, BP1, BP0

The Block Protect Bits (BP2, BP1, BP0 are non-volatile read/write bits in the status register (S4, S3, and S2 that provide write protection control and status. Block protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics. All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table. The factory default setting for the Block Protection Bits is 0, none of the array protected.

8.4 Top/Bottom Block protect (TB

The Top/Bottom bit (TB is non-volatile bits in the status register (S5 that controls if the Block Protect Bits (BP2, BP1, BP0 protect from the Top (TB=0 or the Bottom (TB=1 of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

8.5 Sector/Block Protect (SEC

The Sector protect bit (SEC is non-volatile bits in the status register (S6 that controls if the Block Protect Bits (BP2, BP1, BP0 protect 4KB Sectors (SEC=1or 64KB Blocks (SEC=0 in the Top (TB=0 or the Bottom (TB=1 of the array as shown in the Status Register Memory protection table. The default setting is SEC=0.

8.6 Status Register protect (SRP1, SRP0

The Status Register Protect bits (SRP1 and SRP0 are non-volatile read/write bits in the status register (S8 and S7. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP protection.

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin no control. The register can be written to After a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and can not Be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle(1
1	1	X	One Time Program	Status Register is permanently protected and cannot be written to.

Note:
1. When SRP1, SRP0=(1,0, a power-down, power-up cycle will change SRP1, SRP0 to(0,0 state.

8.7 Quad Enable (QE

The Quad Enable (QE bit is a non-volatile read/write bit in the status register (S9 that allows Quad operation. When the QE bit is set to a 0 state (factory default the /WP pin and /Hold are enabled. When the QE pin is set to a 1 the Quad IO2 and IO3 pins are enabled.

WARNING : The QE bit should never be set to a 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins are tied directly to the power supply or ground.

8.8 Complement Protect (CMP

The Complement Protect bit (CMP is a non-volatile read/write bit in the status register (S14. It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

8.9 Erase/Program Suspend Status (SUS

The Suspend Status bit (SUS is a read only bit in the status register (S15 that is set to 1 after executing an Erase/Program Suspend (75h instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah instruction as well as a power-down, power-up cycle.

8.10 Status Register Memory Protection (CMP = 0

STATUS REGISTER					MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 and 127	7E0000h-7FFFFFh	128KB	Upper 1/64
0	0	0	1	0	124 thru 127	7C0000h-7FFFFFh	256KB	Upper 1/32
0	0	0	1	1	120 thru 127	780000h-7FFFFFh	512KB	Upper 1/16
0	0	1	0	0	112 thru 127	700000h-7FFFFFh	1MB	Upper 1/8
0	0	1	0	1	96 thru 127	600000h-7FFFFFh	2MB	Upper 1/4
0	0	1	1	0	64 thru 127	400000h-7FFFFFh	4MB	Upper 1/2
0	1	0	0	1	0 and 1	000000h-01FFFFh	128KB	Lower 1/64
0	1	0	1	0	0 thru 3	000000h-03FFFFh	256KB	Lower 1/32
0	1	0	1	1	0 thru 7	000000h-07FFFFh	512KB	Lower 1/16
0	1	1	0	0	0 thru 15	000000h-0FFFFFh	1MB	Lower 1/8
0	1	1	0	1	0 thru 31	000000h-1FFFFFh	2MB	Lower 1/4
0	1	1	1	0	0 thru 63	000000h-3FFFFFh	4MB	Lower 1/2
X	X	1	1	1	0 thru 127	000000h-7FFFFFh	8MB	ALL
1	0	0	0	1	127	7FF000h-7FFFFFh	4KB	U – 1/2048
1	0	0	1	0	127	7FE000h-7FFFFFh	8KB	U – 1/1024
1	0	0	1	1	127	7FC000h-7FFFFFh	16KB	U – 1/512
1	0	1	0	X	127	7F8000h-7FFFFFh	32KB	U – 1/256
1	1	0	0	1	0	000000h-000FFFh	4KB	L – 1/2048
1	1	0	1	0	0	000000h-001FFFh	8KB	L – 1/1024
1	1	0	1	1	0	000000h-003FFFh	16KB	L – 1/512
1	1	1	0	X	0	000000h-007FFFh	32KB	L – 1/256

Note:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignored.

8.11 Status Register Memory Protection (CMP = 1

STATUS REGISTER					MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 127	000000h - 7FFFFFh	8MB	ALL
0	0	0	0	1	0 thru 125	000000h – 7DFFFFh	8,064KB	Lower 63/64
0	0	0	1	0	0 thru 123	000000h – 7BFFFFh	7,936KB	Lower 31/32
0	0	0	1	1	0 thru 119	000000h – 77FFFFh	7,680KB	Lower 15/16
0	0	1	0	0	0 thru 111	000000h – 6FFFFFh	7,168KB	Lower 7/8
0	0	1	0	1	0 thru 95	000000h – 5FFFFFh	6MB	Lower 3/4
0	0	1	1	0	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/2
0	1	0	0	1	2 thru 127	020000h - 7FFFFFh	8,064KB	Upper 63/64
0	1	0	1	0	4 and 127	040000h - 7FFFFFh	7,936KB	Upper 31/32
0	1	0	1	1	8 thru 127	080000h - 7FFFFFh	7,680KB	Upper 15/16
0	1	1	0	0	16 thru 127	100000h - 7FFFFFh	7,168KB	Upper 7/8
0	1	1	0	1	32 thru 127	200000h - 7FFFFFh	6MB	Upper 3/4
0	1	1	1	0	64 thru 127	400000h - 7FFFFFh	4MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 127	000000h - 7FEFFFh	8,188KB	L – 2047/2048
1	0	0	1	0	0 thru 127	000000h - 7FDFFFh	8,184KB	L – 1023/1024
1	0	0	1	1	0 thru 127	000000h - 7FBFFFh	8,176KB	L – 511/512
1	0	1	0	X	0 thru 127	000000h - 7F7FFFh	8,160KB	L – 255/256
1	1	0	0	1	0 thru 127	001000h - 7FFFFFh	8,188KB	U – 2047/2048
1	1	0	1	0	0 thru 127	002000h - 7FFFFFh	8,184KB	U – 1023/1024
1	1	0	1	1	0 thru 127	004000h - 7FFFFFh	8,176KB	U – 511/512
1	1	1	0	X	0 thru 127	008000h - 7FFFFFh	8,160KB	U – 255/256

Note:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignored.

9. INSTRUCTIONS

The SPI instruction set of the ZD25Q64B consists of thirty eight basic instructions and the QPI instruction set of the ZD25Q64B consists of thirty one basic instructions that are fully controlled through the SPI bus (see Instruction Set table. Instructions are initiated with the falling edge of Chip Select (/CS. The first byte of data clocked into the input pins (DI or IO [3:0] provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB first.

Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 6 through 43. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte (/CS driven high after a full 8-bit have been clocked otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Register will be ignored until the program or erase cycle has completed.

9.1 Manufacturer and Device Identification

		ID code	Instruction
Manufacturer ID		BAh	90h, 92h, 94h, 9Fh
Device ID	ZD25Q64B	16h	90h, 92h, 94h, ABh
Memory Type ID	SPI / QPI	32h	9Fh
Capacity Type ID	64M	17h	9Fh

9.2 Instruction Set Table 1 (SPI instruction(1

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
(CLOCK NUMBER	(0 – 7	(8 - 15	(16 - 23	(24 - 31	(32 - 39	(40 - 47
Write Enable	**06h**					
Write Enable For Volatile Status Register	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(SR7-SR0(2				
Read Status Register-2	**35h**	(SR15-SR8(2				
Write Status Register-1	**01h**	(SR7-SR0	(SR15-SR8			
Write Status Register-2	**31h**	(SR15-SR8				
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0	
Fast Read Data	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0
Page Program	**02h**	A23-A16	A15-A8	A7-A0	(D7-D0(3	
Enable QPI	**38h**					
Sector Erase(4KB	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase(32KB	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase(64KB	**D8h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**60h/C7h**					
Erase/Program Suspend	**75h**					
Erase/Program Resume	**7Ah**					
Deep Power-down	**B9h**					
Release Deep power down/ Device ID(4	**ABh**	Dummy	dummy	dummy	(ID7-ID0(2	
Read Manufacturer/ Device ID(4	**90h**	00h	00h	00h or 01h	(MID7-MID0	(DID7-DID0
Read JEDEC ID	**9Fh**	(MID7-MID0 Manufacturer	(D7-D0 Memory Type	(D7-D0 Capacity Type		
Reset Enable	**66h**					
Reset	**99h**					
Enter Secured OTP	**B1h**					
Exit Secured OTP	**C1h**					
Read Security Register	**2Bh**	(SC7-SC0 (10				
Write Security Register	**2Fh**					
Read Serial Flash Discovery Parameter	**5Ah**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0

9.3 Instruction Set Table 2 (Dual SPI Instruction

(CLOCK NUMBER / INSTRUCTION NAME	(0 – 7	(8 - 15	(16 - 23	(24 - 31	(32 - 39	(40 - 47
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0(6
Fast Read Dual I/O	**BBh**	A23-A8(5	A7-A0, M7-M0(5	(D7-D0, …(6		
Read Dual Manufacture/ Device ID(4	**92h**	0000h	(00h, xxxx or (01h, xxxx	(MID7-MID0 (DID7-DID0(6		

9.4 Instruction Set Table 3 (Quad SPI Instruction

(CLOCK NUMBER / INSTRUCTION NAME	(0 – 7	(8 - 15	(16 - 23	(24 - 31	(32 - 39	(40 - 47
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0 (8
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0(7	(xxxx, D7-D0,…(9	(D7-D0, …(8		
Quad Page Program	**33h**	A23-A0 (D7-D0, …(8				
Read Quad Manufacture/Device ID(4	**94h**	(00_0000h, xx or (00_0001h, xx	(xxxx, MID7-MID0 (xxxx, DID7-DID0(9			
Word Read Quad I/O	**E7h**	A23-A0, M7-M0(7	(xx, D7-D0..	(D7-D0(8		
Set Burst with Wrap	**77h**	xxxxxx, W6-W4(7				

9.5 Instruction Set Table 4 (QPI instruction

INSTRUCTION NAME		BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8	BYTE 9
(CLOCK NUMBER		(0 , 1	(2 , 3	(4 , 5	(6 , 7	(8 , 9	(10 , 11	(12 , 13	(14 , 15	(16 , 17
Write Enable		06h								
Write Enable for Volatile Status Register		50h								
Write Disable		04h								
Read Status Register-1		05h	(SR7-SR0 (2							
Read Status Register-2		35h	(SR15-SR8(2							
Write Status Register-1(5		01h	(SR7-SR0	(SR15-SR8						
Write Status Register-2		31h	(SR15-SR8							
Fast Read Data	>80MHz	0Bh	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0		
	>108MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	(D7-D0	
	>133MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	dummy	(D7-D0
Page Program		02h	A23-A16	A15-A8	A7-A0	(D7-D0 (3				
Sector Erase(4KB		20h	A23-A16	A15-A8	A7-A0					
Block Erase(32KB		52h	A23-A16	A15-A8	A7-A0					
Block Erase(64KB		D8h	A23-A16	A15-A8	A7-A0					
Chip Erase		60h/ C7h								
Erase/Program Suspend		75h								
Erase/Program Resume		7Ah								
Deep Power-down		B9h								
Release Deep power down		ABh	Dummy	dummy	dummy	(ID7-ID0(2				
Read Manufacturer/ Device ID(4		90h	00h	00h	00h or 01h	(MID7-MID0	(DID7-DID0			
Read JEDEC ID(4		9Fh	(MID7-MID0 Manufacturer	(D7-D0 Memory Type	(D7-D0 Capacity Type					
Enter Security		B1h								
Exit Security		C1h								
Read Security Register		2Bh	(SC7-SC0 (10							
Write Security Register		2Fh								
Fast Read Quad I/O	>80MHz	EBh	A23-A16	A15-A8	A7-A0	(M7-M0	dummy	(D7-D0		
	>108MHz		A23-A16	A15-A8	A7-A0	(M7-M0	dummy	dummy	(D7-D0	
	>133MHz		A23-A16	A15-A8	A7-A0	(M7-M0	dummy	dummy	dummy	(D7-D0
Reset Enable		66h								

Reset		**99h**								
Disable QPI		**FFh**								
Burst Read with Wrap	>80MHz	**0Ch**	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0		
	>108MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	(D7-D0	
	>133MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	dummy	(D7-D0
Set Read Parameter		**C0h**	P7-P0							
Quad Page Program		**33h**	A23-A16	A15-A8	A7-A0	(D7-D0				

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "(" indicate data being read from the device on the IO pin.
2. SR = status register,
   The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Register, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. See Manufacturer and Device Identification table for Device ID information.
5. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
6. Dual Output data

   IO0 = (D6, D4, D2, D0
   IO1 = (D7, D5, D3, D1

7. Quad Input Address

   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap Input
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x x

8. Quad Input/ Output Data
   IO0 = (D4, D0…
   IO1 = (D5, D1…
   IO2 = (D6, D2…
   IO3 = (D7, D3…

9. Fast Read Quad I/O Data Output
   IO0 = (x, x, x, x, D4, D0…
   IO1 = (x, x, x, x, D5, D1…
   IO2 = (x, x, x, x, D6, D2…
   IO3 = (x, x, x, x, D7, D3…

10. SC = security register

9.6 Write Enable (06h

Write Enable instruction is for setting the Write Enable Latch (WEL bit in the Status Register. The WEL bit must be set prior to every Program, Erase and Write Status Register instruction. To enter the Write Enable instruction, /CS goes low prior to the instruction “06h” into Data Input (DI pin on the rising edge of CLK, and then driving /CS high.

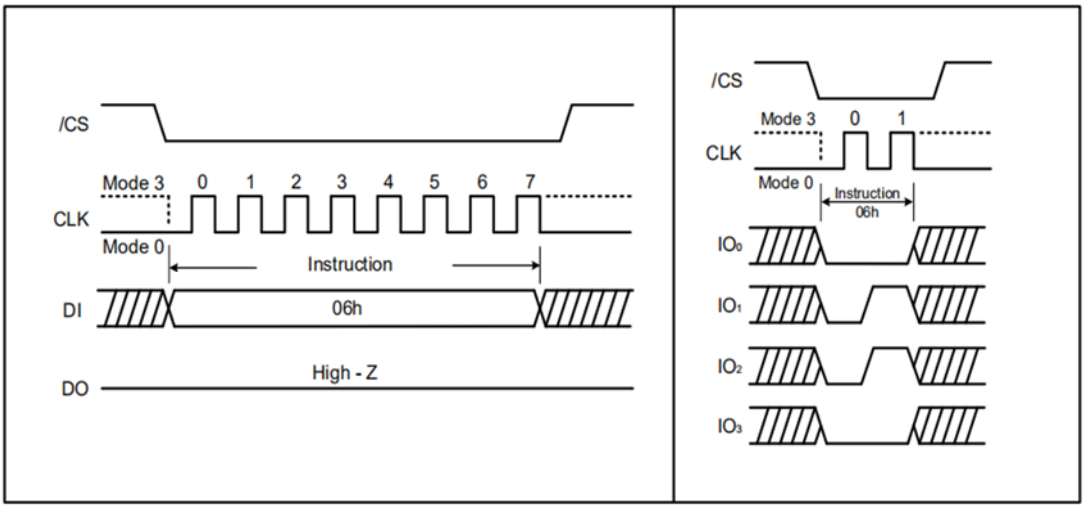


Figure 6. Write Enable Instruction for SPI Mode (left) and QPI Mode (right)

9.7 Write Enable for Volatile Status Register (50h

This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h instruction must be issued prior to a Write Status Register (01h instruction. Write Enable for Volatile Status Register instruction (Figure 7 will not set the Write Enable Latch (WEL bit. Once Write Enable for Volatile Status Register is set, a Write Enable instruction should not have been issued prior to setting Write Status Register instruction (01h or 31h.

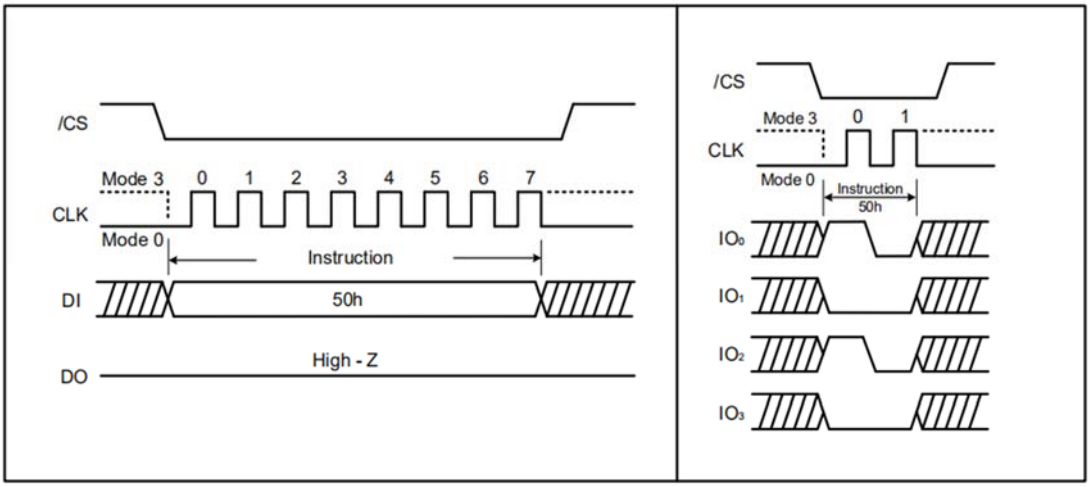


Figure 7. Write Enable for Volatile Status Register Instruction for SPI Mode (left) and QPI Mode (right)

9.8 Write Disable (04h

The Write Disable instruction is to reset the Write Enable Latch (WEL bit in the Status Register. To enter the Write Disable instruction, /CS goes low prior to the instruction “04h” into Data Input (DI pin on the rising edge of CLK, and then driving /CS high. WEL bit is automatically reset write-disable status of “0” after Power-up and upon completion of the every Program, Erase and Write Status Register instructions.

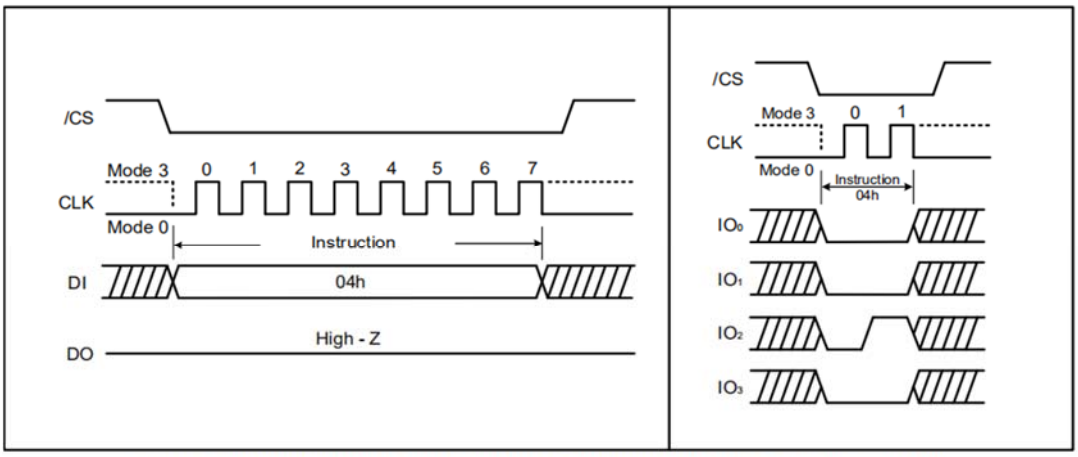


Figure 8. Write Disable Instruction for SPI Mode (left) and QPI Mode (right)

9.9 Read Status Register-1 (05h and Read Status Register-2 (35h

The Read Status Register instructions are to read the Status Register. The Read Status Register can be read at any time (even in program/erase/write Status Register and Write Security Register condition. It is recommended to check the BUSY bit before sending a new instruction when a Program, Erase, Write Status Register or Write Status Register operation is in progress.

The instruction is entered by driving /CS low and sending the instruction code “05h” for Status Register-1 or “35h” for Status Register-2 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB first as shown in (figure 9. The Status Register can be read continuously. The instruction is completed by driving /CS high.

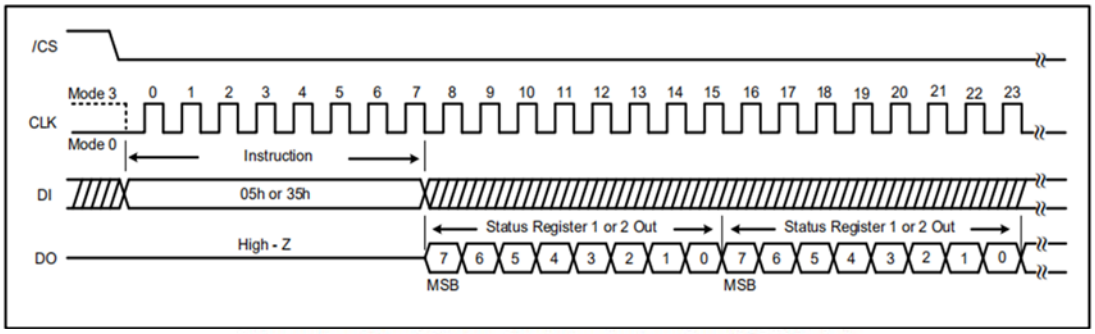


Figure 9a. Read Status Register Instruction (SPI Mode)

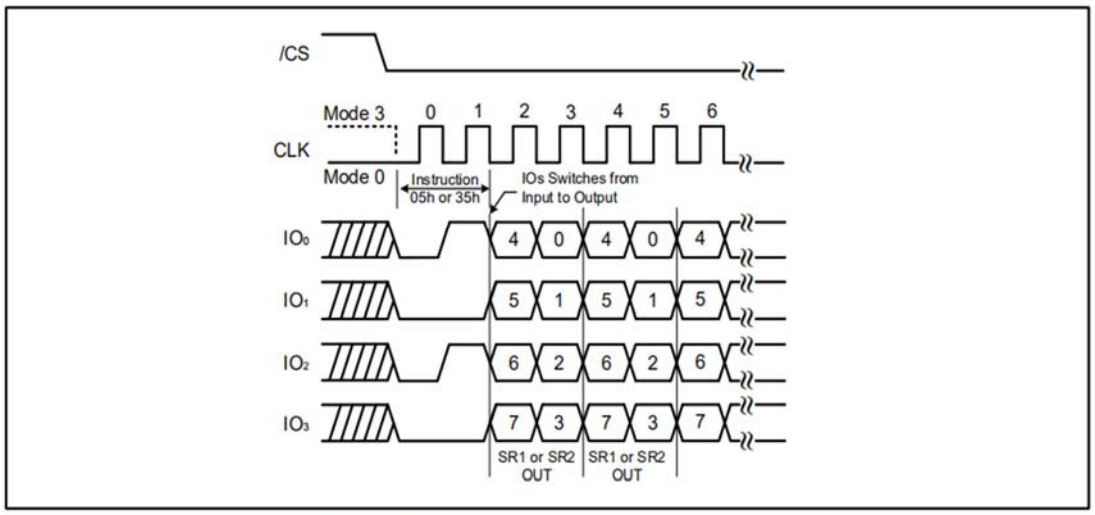


Figure 9b. Read Status Register Instruction (QPI Mode)

9.10 Write Status Register (01h

The Write Status Register instruction is to write only non-volatile Status Register-1 bits (SRP0, SEC, TB, BP2, BP1 and BP0 and Status Register-2 bits (CMP, QE and SRP1. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

A Write Enable instruction must previously have been issued prior to setting Write Status Register Instruction (Status Register bit WEL must equal 1. Once write is enabled, the instruction is entered by driving /CS low, sending the instruction code, and then writing the status register data byte as illustrated in figure 10.

The /CS pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register instruction will not be executed. If /CS is driven high after the eighth clock, the CMP, QE and SRP1 bits will be cleared to 0. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics.

While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL bit in Status Register will be cleared to 0.

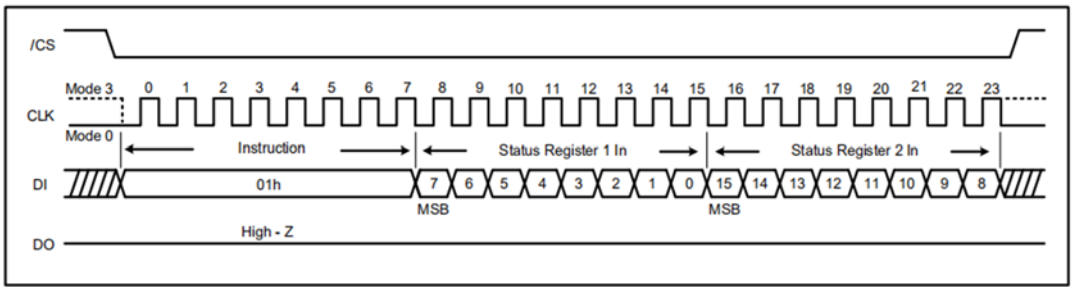


Figure 10a. Write Status Register Instruction (SPI Mode)

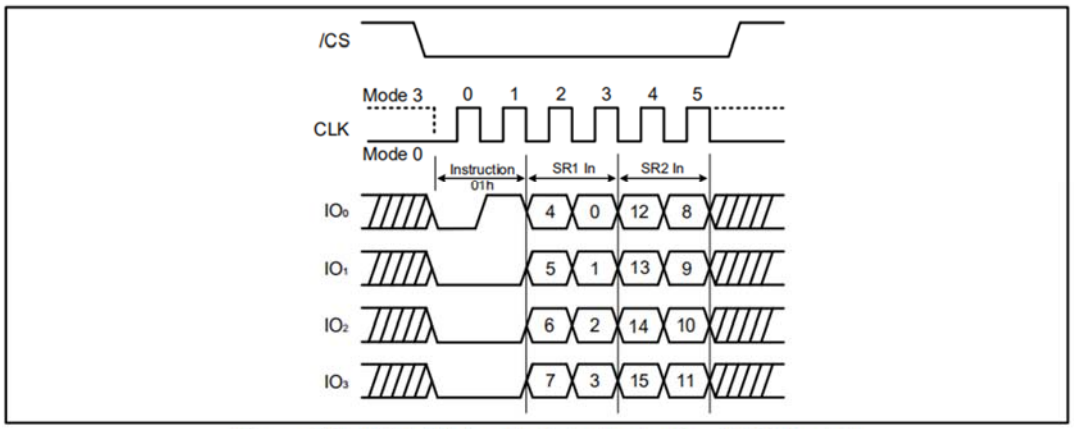


Figure 10b. Write Status Register Instruction (QPI Mode)

9.11 Write Status Register-2 (31h

The Write Status Register-2 instruction is to write only non-volatile Status Register-2 bits (CMP, QE and SRP1.

A Write Enable instruction must previously have been issued prior to setting Write Status Register Instruction (Status Register bit WEL must equal 1. Once write is enabled, the instruction is entered by driving /CS low, sending the instruction code, and then writing the status register data byte as illustrated in figure 11.

Using Write Status Register-2 (31h instruction, software can individually access each one-byte status registers via different instructions.

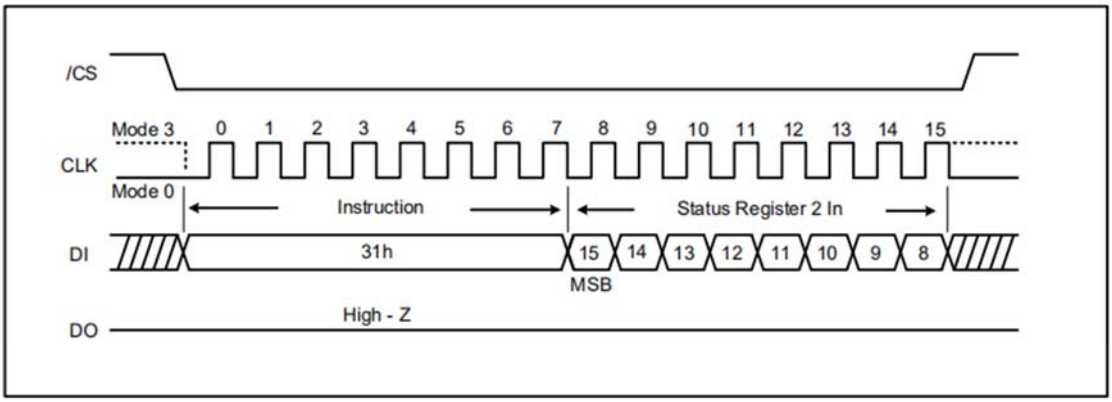


Figure 11a. Write Status Register-2 Instruction (SPI Mode)

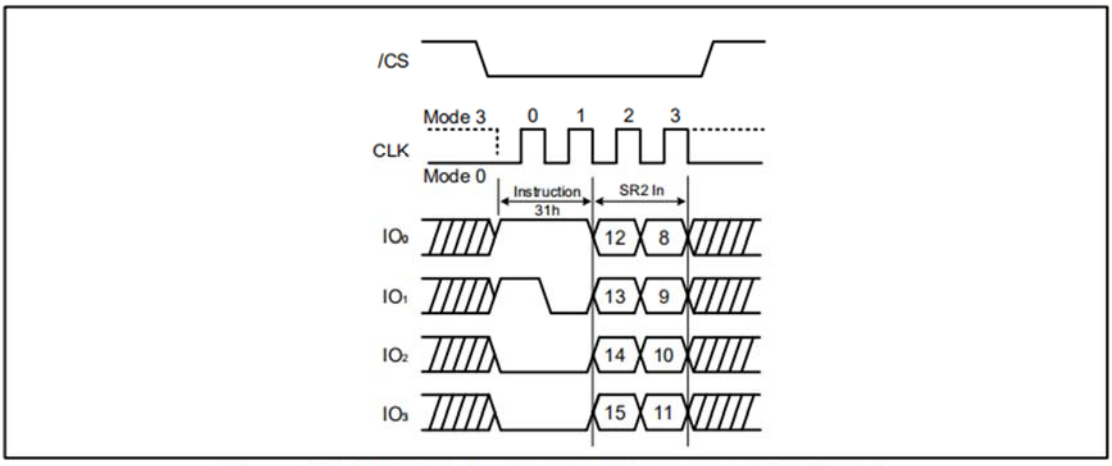


Figure 11b. Write Status Register-2 Instruction (QPI Mode)

9.12 Read Data (03h

The Read Data instruction is to read data out from the device. The instruction is initiated by driving the /CS pin low and then sending the instruction code “03h” with following a 24-bit address (A23-A0 into the DI pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB first. The address is automatically incremented to the next higher address after byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The Read Data instruction sequence is shown in (figure 12. If a Read Data instruction is issued while an Erase, Program or Write Status Register cycle is in process (BUSY=1 the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C to a maximum of f_R (see AC Electrical Characteristics.

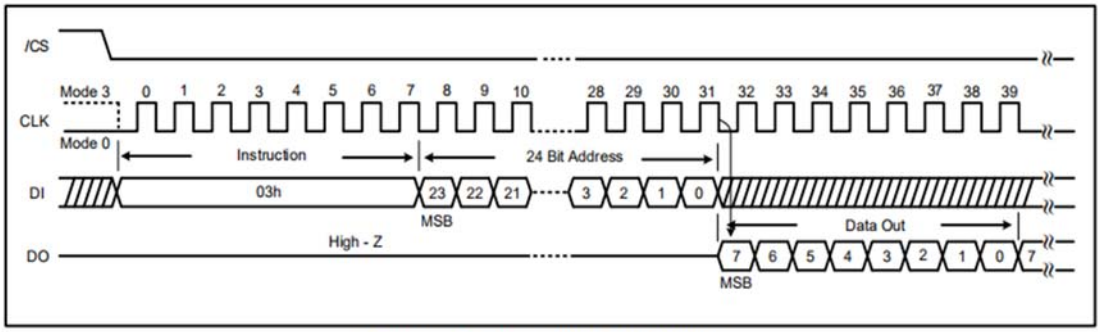


Figure 12. Read Data Instruction

9.13 Fast Read (0Bh

The Fast Read instruction is high speed reading mode that it can operate at the highest possible frequency of F_R. The address is latched on the rising edge of the CLK. After the 24-bit address, this is accomplished by adding “dummy” clocks as shown in (figure 13. The dummy clocks means the internal circuits require time to set up the initial address. During the dummy clocks, the data value on the DO pin is a “don’t care”. Data of each bit shifts out on the falling edge of CLK.

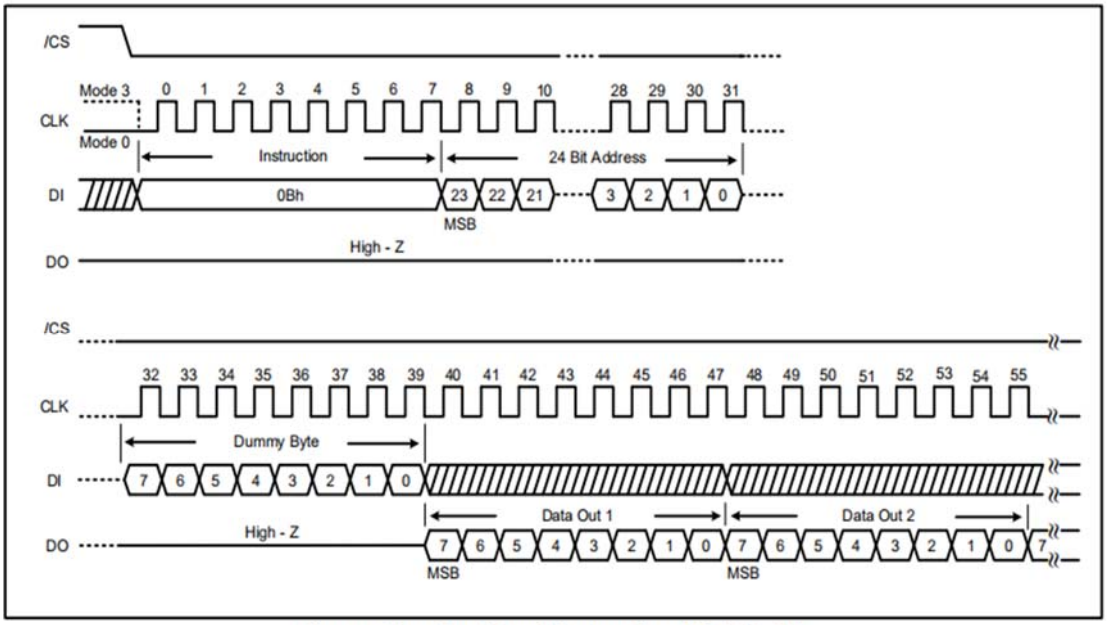


Figure 13a. Fast Read Instruction (SPI Mode)

Fast Read in QPI Mode

When QPI mode is enabled, the number of dummy clock is configured by the “Set Read Parameters (C0h” instruction to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bit P[4] and P[5] setting, the number of dummy clocks can be configured as either 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 4. (Please refer to figure 13b, 13c, 13d.

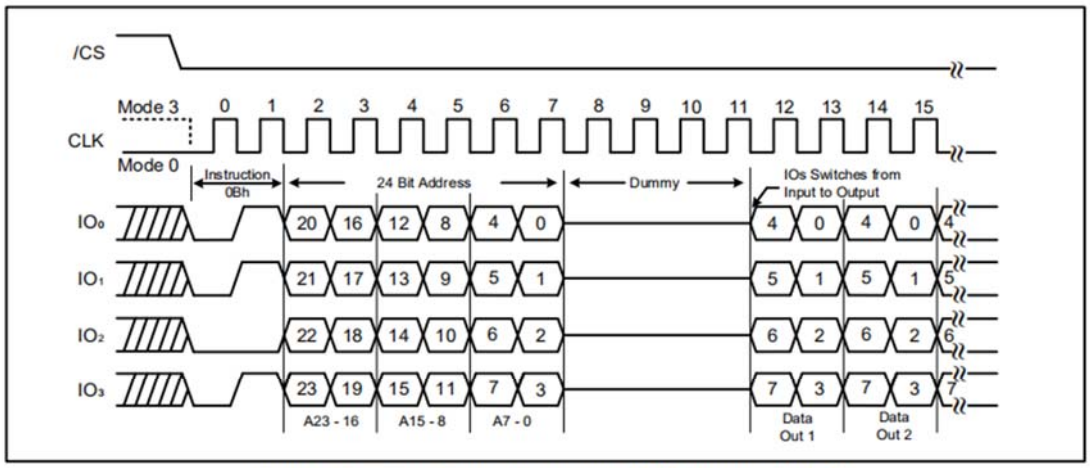


Figure 13b. Fast Read instruction (QPI Mode, 80MHz)

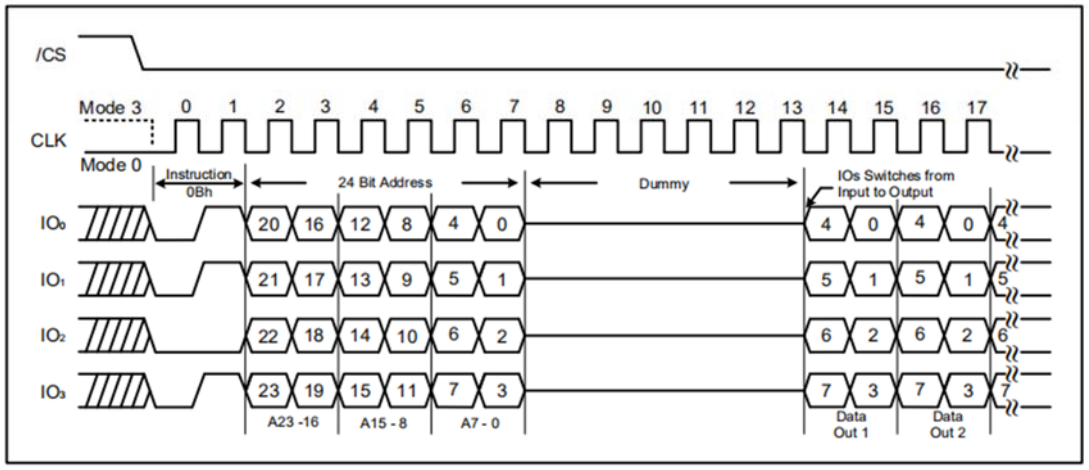


Figure 13c. Fast Read instruction (QPI Mode, 108MHz)

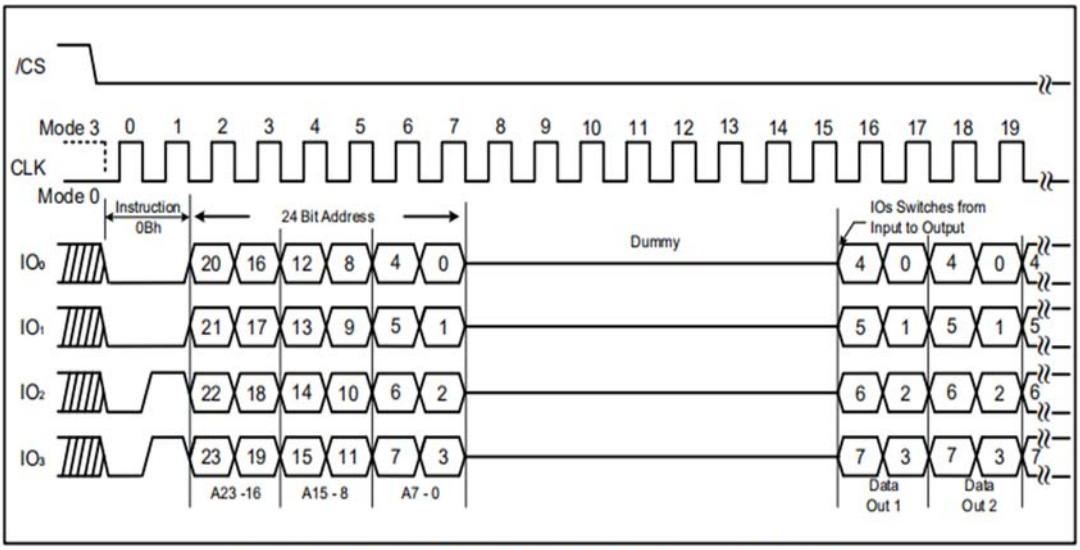


Figure 13d. Fast Read instruction (QPI Mode, 133MHz)

9.14 Fast Read Dual Output (3Bh

By using two pins (IO_0 and IO_1, instead of just IO_0, The Fast Read Dual Output instruction allows data to be transferred from the ZD25Q64B at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for application that cache code-segments to RAM for execution.

The Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics. After the 24-bit address, this is accomplished by adding eight “dummy” clocks as shown in (figure 14. The dummy clocks allow the internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the DO pin is a “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

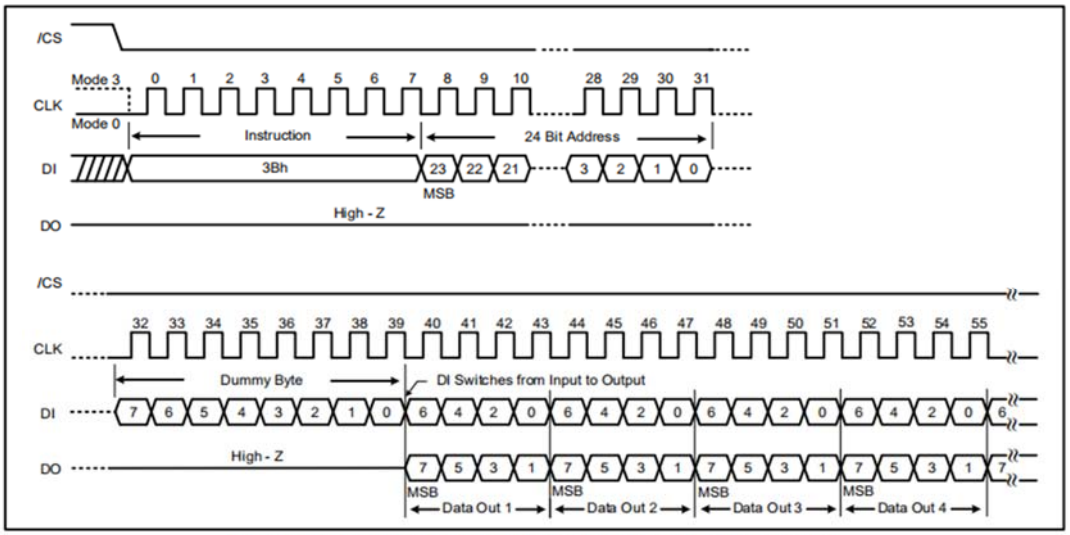


Figure14. Fast Read Dual Output instruction (SPI Mode)

9.15 Fast Read Quad Output (6Bh

By using four pins (IO_0, IO_1, IO_2, and IO_3, The Fast Read Quad Output instruction allows data to be transferred from the ZD25Q64B at four times the rate of standard SPI devices.
A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output instruction (Status Register bit QE must equal 1.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics. This is accomplished by adding eight “dummy” clocks after the 24- bit address as shown in (figure 15. The dummy clocks allow the internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the DO pin is a “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock

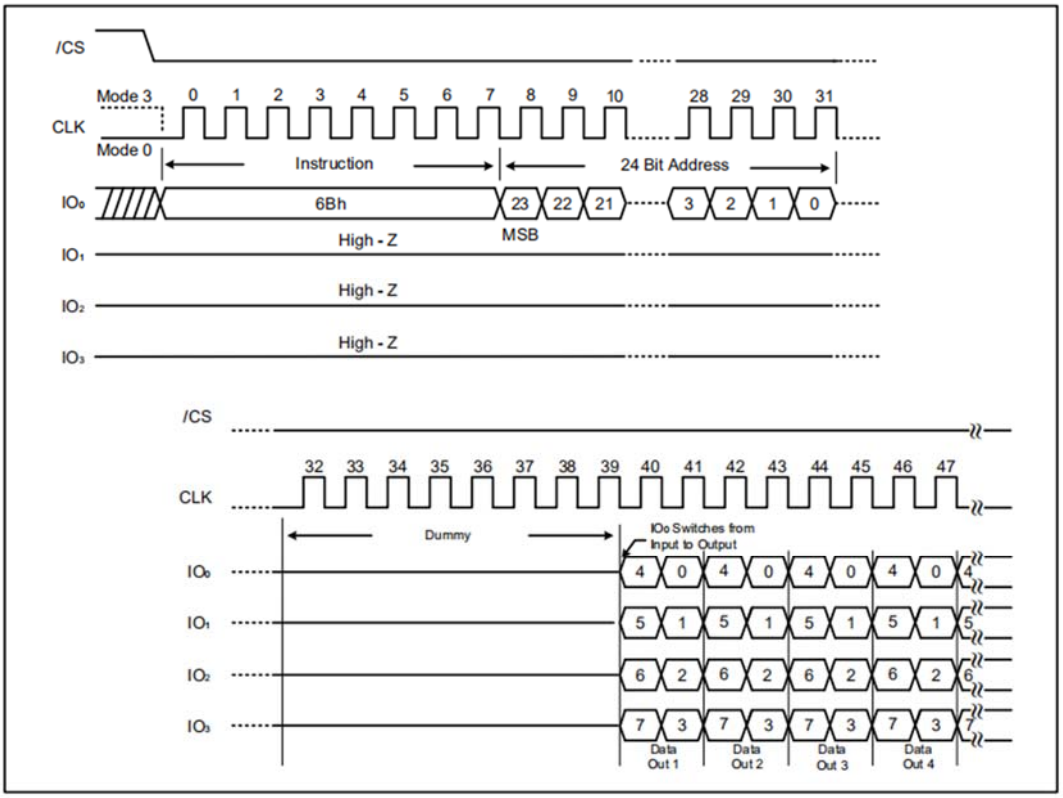


Figure 15. Fast Read Quad Output instruction (SPI Mode)

9.16 Fast Read Dual I/O (BBh

The Fast Read Dual I/O instruction reduces cycle overhead through double access using two IO pins: IO_0 and IO_1.

Continuous read mode

The Fast Read Dual I/O instruction can further reduce cycle overhead through setting the Mode bits (M7-0 after the input Address bits (A23-0. The upper nibble of the Mode (M7-4 controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the Mode (M3-0 are don't care ("X", However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Mode bits (M7-0 equal "Ax" hex, then the next Fast Dual I/O instruction (after /CS is raised and then lowered does not require the instruction (BBh code, as shown in (figure 16b. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after /CS is asserted low. If Mode bits (M7-0 are any value other "Ax" hex, the next instruction (after /CS is raised and then lowered requires the first byte instruction code, thus returning to normal operation. A Mode Bit Reset can be used to reset Mode Bits (M7-0 before issuing normal instructions.

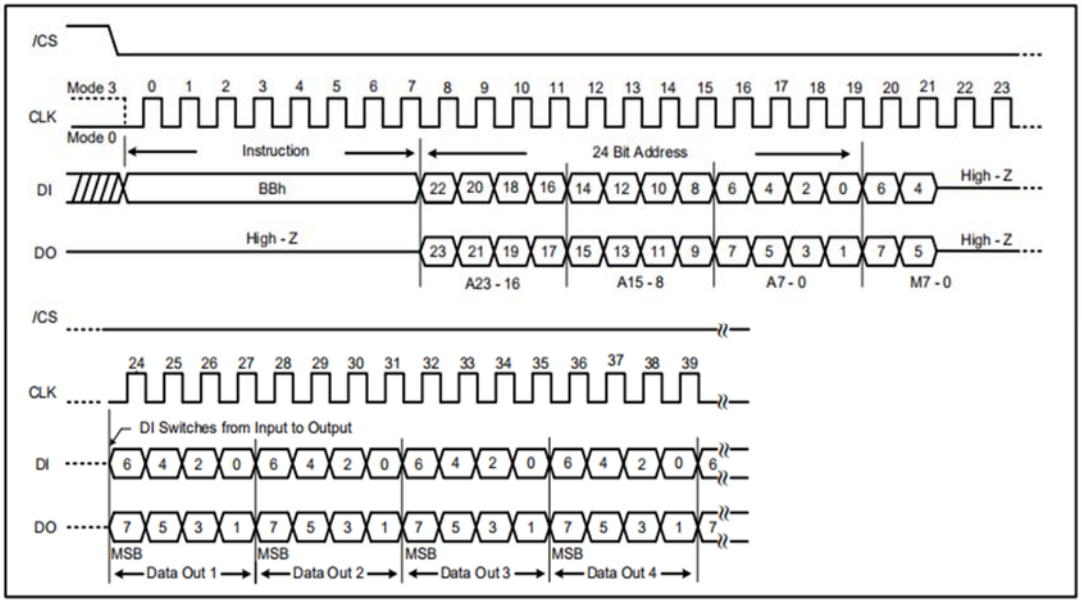


Figure 16a. Fast Read Dual I/O Instruction (initial instruction or previous M7-0≠ Axh)

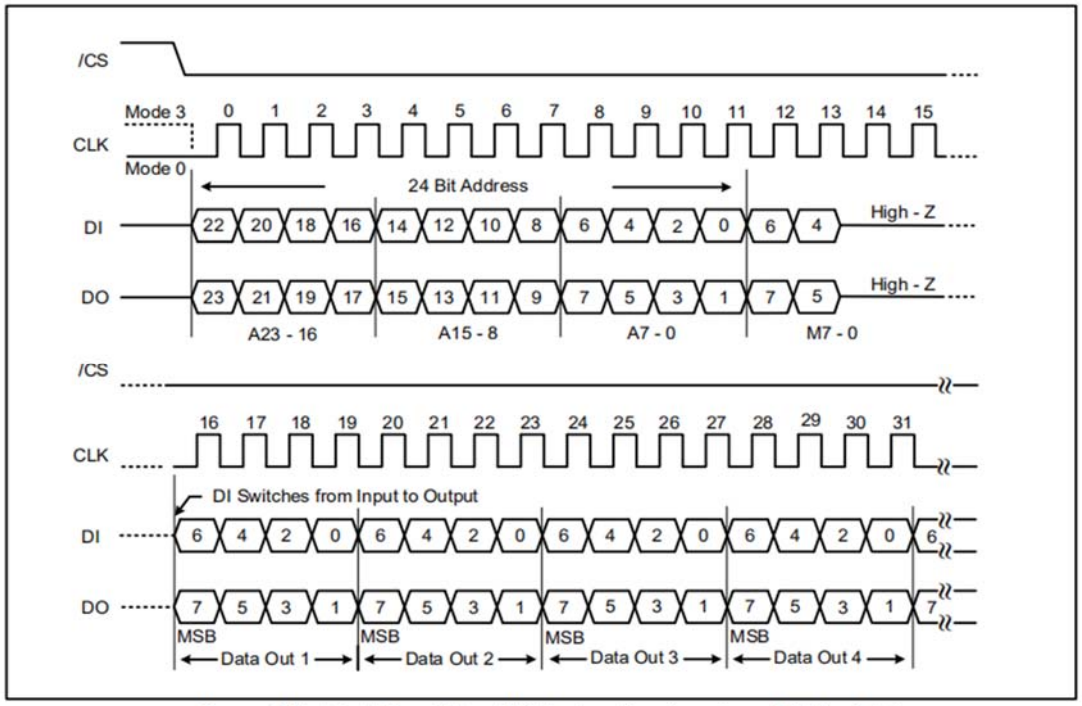


Figure 16b. Fast Read Dual I/O Instruction (previous M7-0= Axh)

9.17 Fast Read Quad I/O (EBh

The Fast Read Quad I/O instruction reduces cycle overhead through quad access using four IO pins: IO_0, IO_1, IO_2, and IO_3. The Quad Enable bit (QE of Status Register-2 must be set to enable the Fast read Quad I/O Instruction.

Continuous read mode

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Mode bits (M7-0 with following the input Address bits (A23-0, as shown in (figure 17a. The upper nibble of the Mode (M7-4 controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the Mode (M3-0 are don't care ("X". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Mode bits (M7-0 equal "Ax" hex, then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered does not require the EBh instruction code, as shown in (figure 17b. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after /CS is asserted low. If the Mode bits (M7-0 are any value other than "Ax" hex, the next instruction (after /CS is raised and then lowered requires the first byte instruction code, thus retuning normal operation. A Mode Bit Reset can be used to reset Mode Bits (M7-0 before issuing normal instructions.

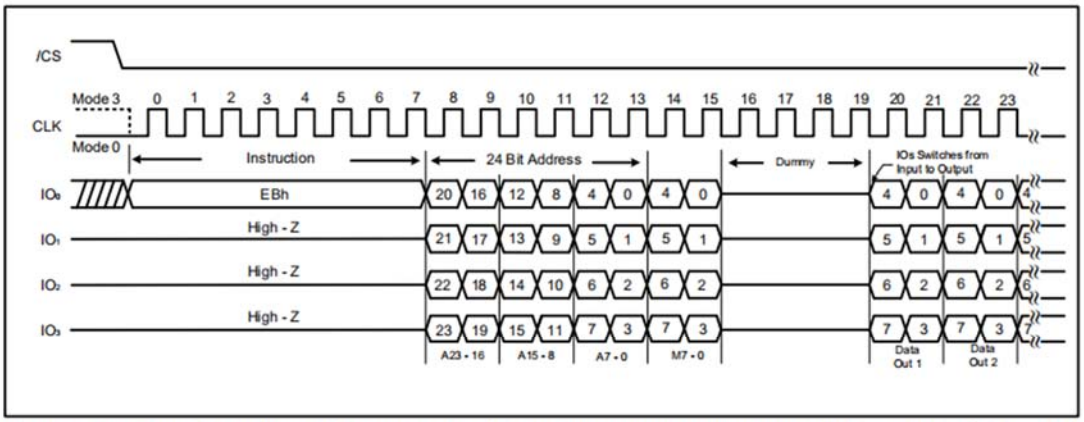


Figure 17a. Fast Read Quad I/O Instruction (Initial instruction or previous M7-0 ≠ Axh, SPI mode)

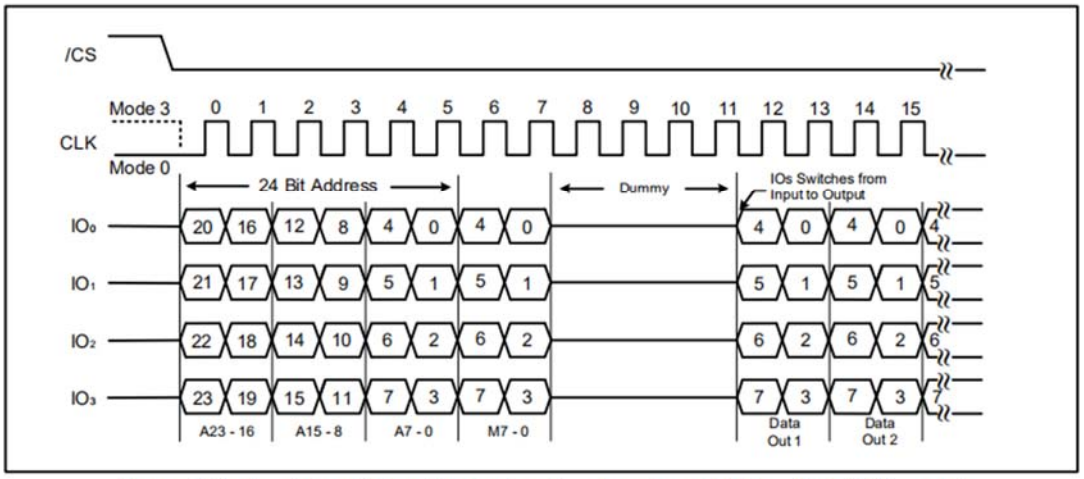


Figure 17b. Fast Read Quad I/O Instruction (previous M7-0 = Axh, SPI mode)

Wrap Around in SPI mode

The Fast Read Quad I/O instruction can also be used to access specific portion within a page by issuing a “Set Burst with Wrap” (77h instruction prior Fast Read Quad I/O (EBh instruction. The “Set Burst with Wrap” (77h instruction can either enable or disable the “Wrap Around” feature for the following Fast Read Quad I/O instruction.

When “Wrap Around” is enabled, the data being accessed can be limited to an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.
The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte of data without issuing multiple read instructions. (Please refer to 10.35 Set Burst with Wrap.

Fast Read Quad I/O in QPI mode

When QPI mode in enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h” instruction to accommodate a wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P [4] and P [5] setting, the number of dummy clocks can be configured as either 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset (99h instruction is 4.

“Continuous Read Mode” feature is also available in QPI mode for Fast Read Quad I/O instruction. In QPI mode, the “Continuous Read Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

“Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a “Burst Read with Wrap” (0Ch instruction must be used. (Please refer to 10.36 Burst Read with Wrap.

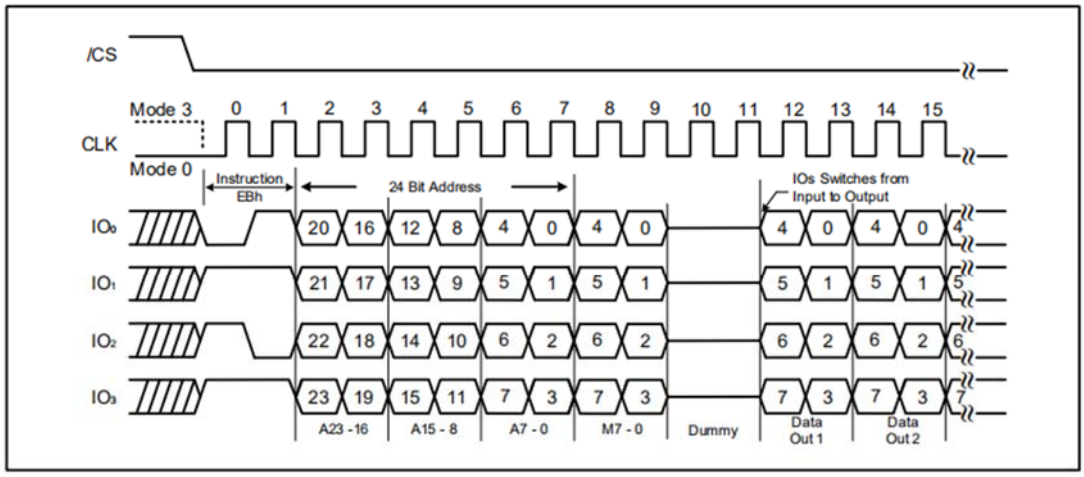


Figure 17c. Fast Read Quad I/O Instruction
(Initial instruction or previous M7-0 ≠ Axh, QPI mode, 80MHz)

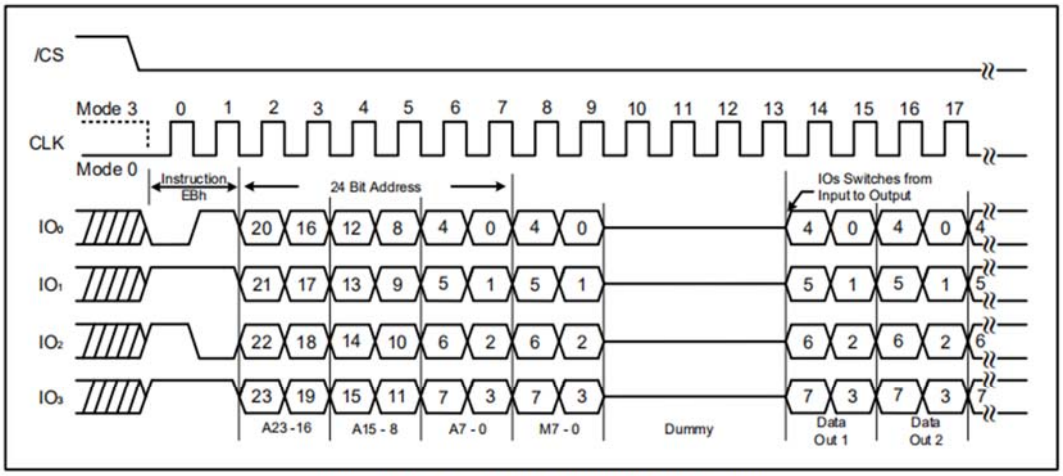


Figure 17d. Fast Read Quad I/O Instruction
(Initial instruction or previous M7-0 ≠ Axh, QPI mode, 108MHz)

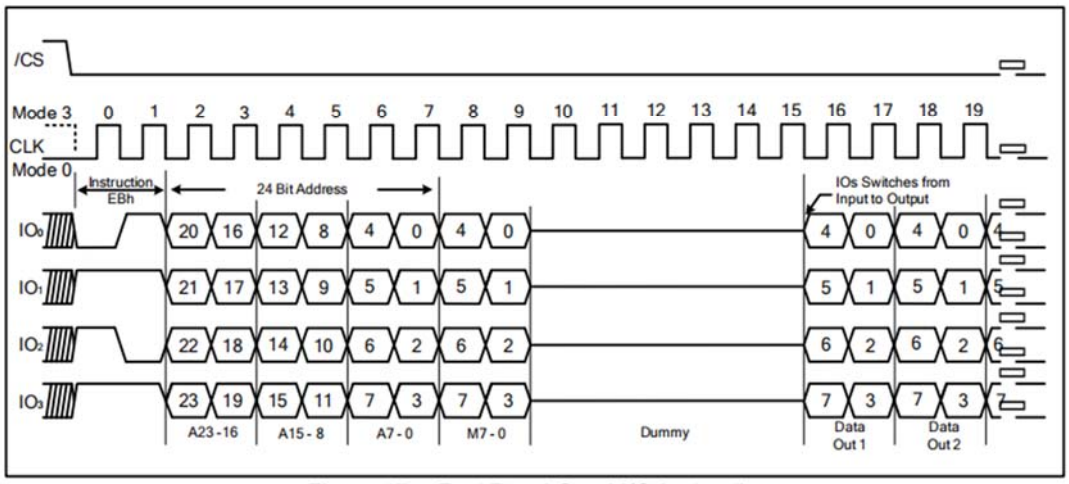


Figure 17e. Fast Read Quad I/O Instruction

9.18 Page Program (02h

The Page Program instruction is for programming the memory to be “0”. A Write Enable instruction must be issued before the device accept the Page Program Instruction (Status Register bit WEL= 1. After the Write Enable (WREN instruction has been decoded, the device sets the Write Enable Latch (WEL. The instruction is entered by driving the /CS pin low and then sending the instruction code “02h” with following a 24-bits address (A23-A0 and at least one data byte, into the DI pin. The /CS pin must be driven low for the entire time of the instruction while data is being sent to the device. (Please refer to figure 18.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tPP (See AC Characteristics. While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Protect (CMP, SEC, TB, BP2, BP1 and BP0 bits.

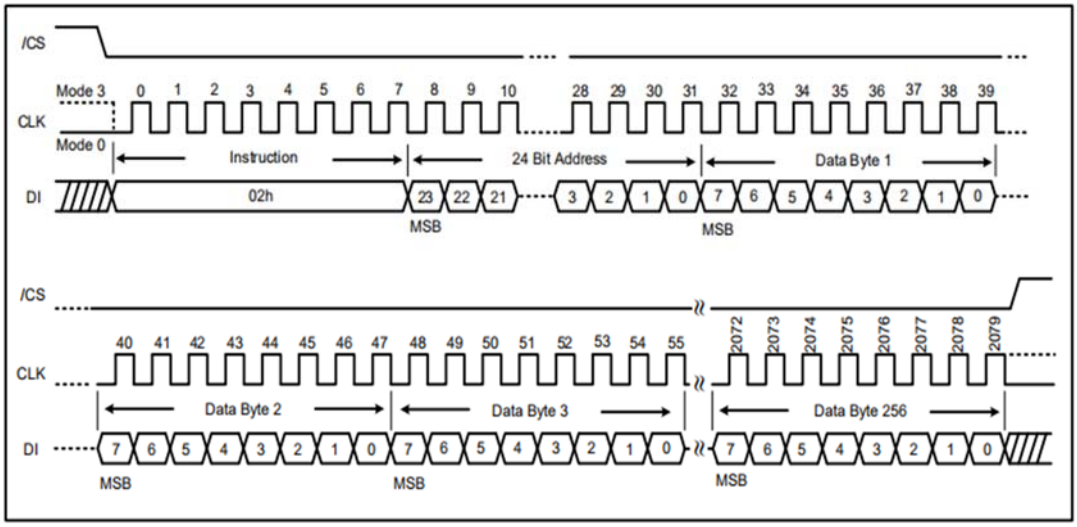


Figure 18a. Page Program Instruction (SPI Mode)

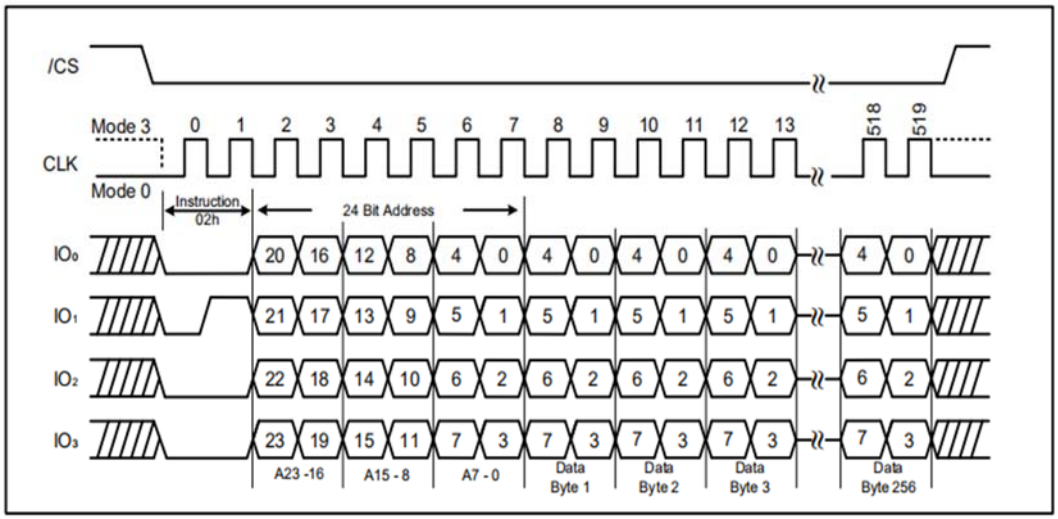


Figure 18b. Page Program Instruction (QPI Mode)

9.19 Quad Page Program (33h

The Quad Page Program instruction is to program the memory as being “0” at previously erased memory areas. The Quad Page Program takes four pins: IO_0, IO_1, IO_2 and IO_3 as address and data input, which can improve programmer performance and the effectiveness of application of lower clock less than 5MHz. System using faster clock speed will not get more benefit for the Quad Page Program as the required internal page program time is far more than the time data clock-in.

To use Quad Page Program, the Quad Enable bit must be set, A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1. The instruction is initiated by driving the /CS pin low then sending the instruction code “33h” with following a 24-bit address (A23-A0 and at least one data, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are perfectly same as standard Page Program. (Please refer to figure 19.

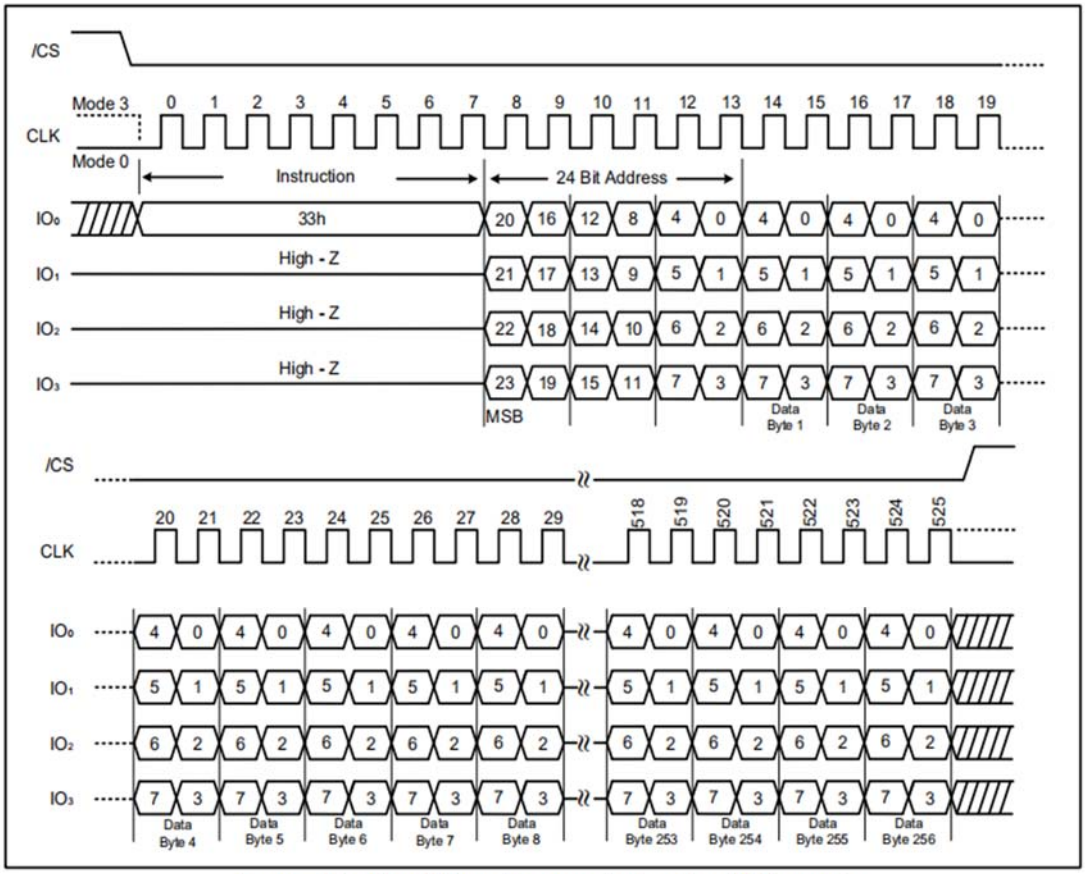


Figure 19a. Quad Page Program Instruction (SPI mode)

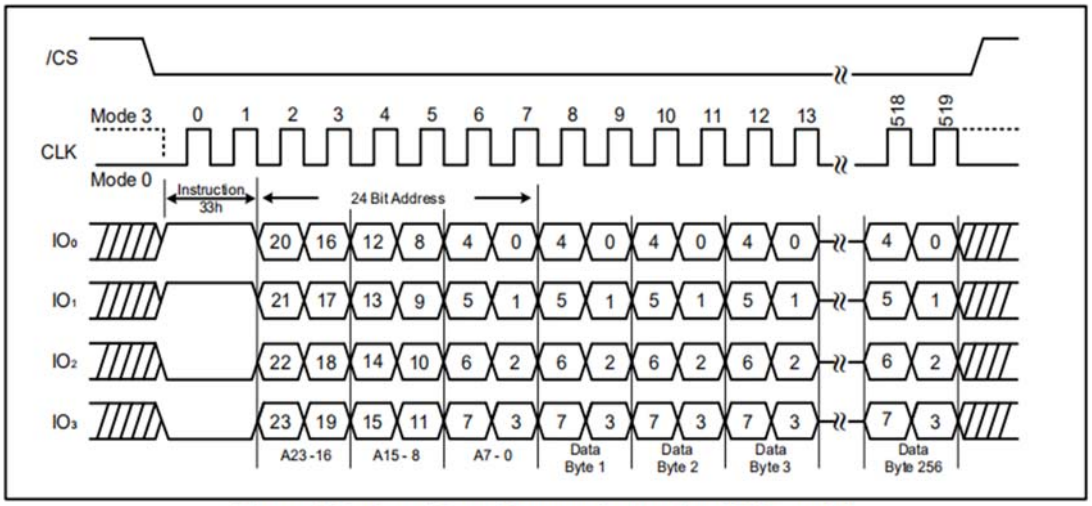


Figure 19b. Quad Page Program Instruction (QPI mode)

9.20 Sector Erase (20h

The Sector Erase instruction is to erase the data of the selected sector as being “1”. The instruction is used for 4K-byte sector. Prior to the Sector Erase Instruction, the Write Enable instruction must be issued. The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0. (Please refer to figure 20. The /CS pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Sector Erase instruction will not be executed. After /CS goes high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics.

While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL bit in the Status Register is cleared to 0. The sector Erase instruction will not be executed if the addressed page is protected by the Protect (CMP, SEC, TB, BP2, BP1 and BP0 bits.

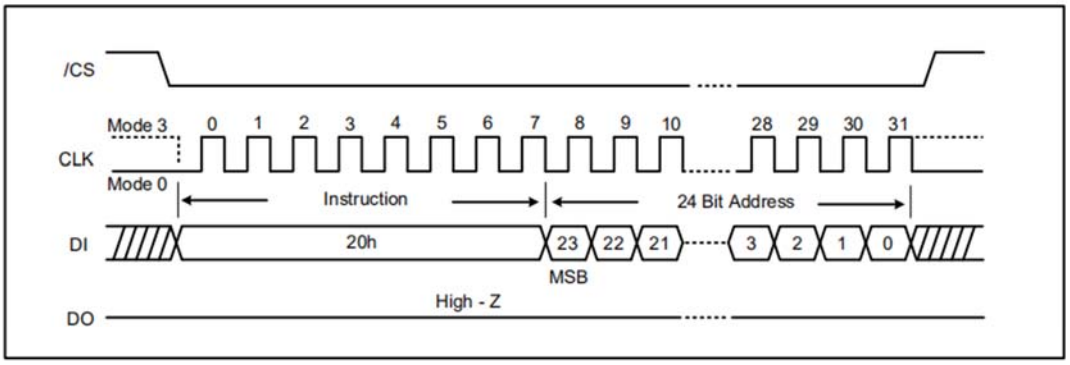


Figure 20a. Sector Erase Instruction (SPI Mode)

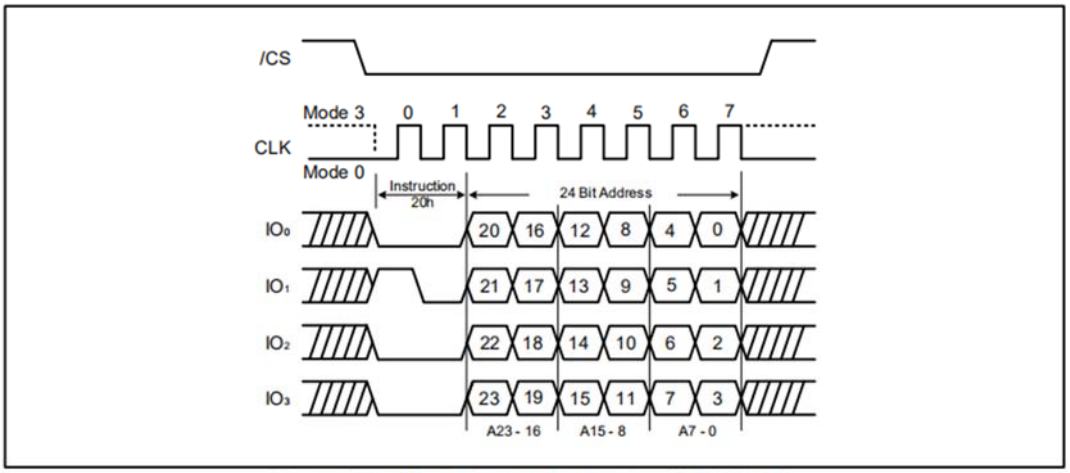


Figure 20b. Sector Erase Instruction (QPI Mode)

9.21 32KB Block Erase (52h

The Block Erase instruction is to erase the data of the selected block as being “1”. The instruction is used for 32K-byte Block erase operation. Prior to the Block Erase Instruction, a Write Enable instruction must be issued. The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0. (Please refer to figure 21. The /CS pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics.

While the Block Erase cycle is in progress, the Read Status Register instruction may still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL bit in the Status Register is cleared to 0. The Block erase instruction will not be executed if the addressed page is protected by the Protect (CMP, SEC, TB, BP2, BP1 and BP0 bits.

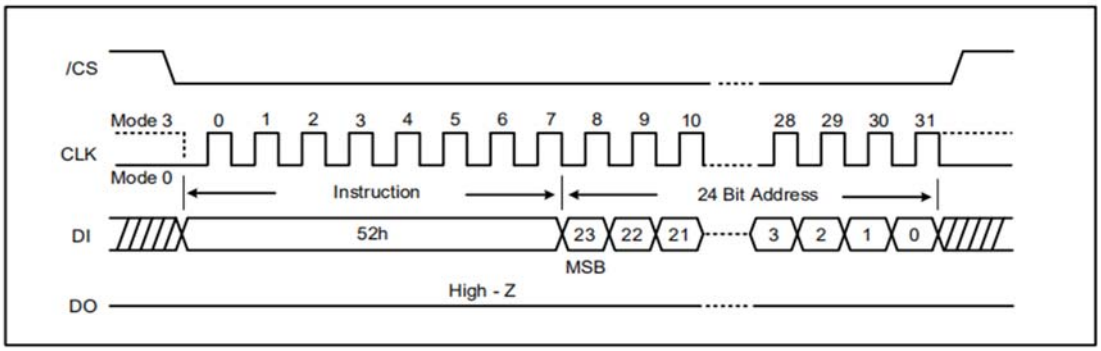


Figure 21a. 32KB Block Erase Instruction (SPI Mode)

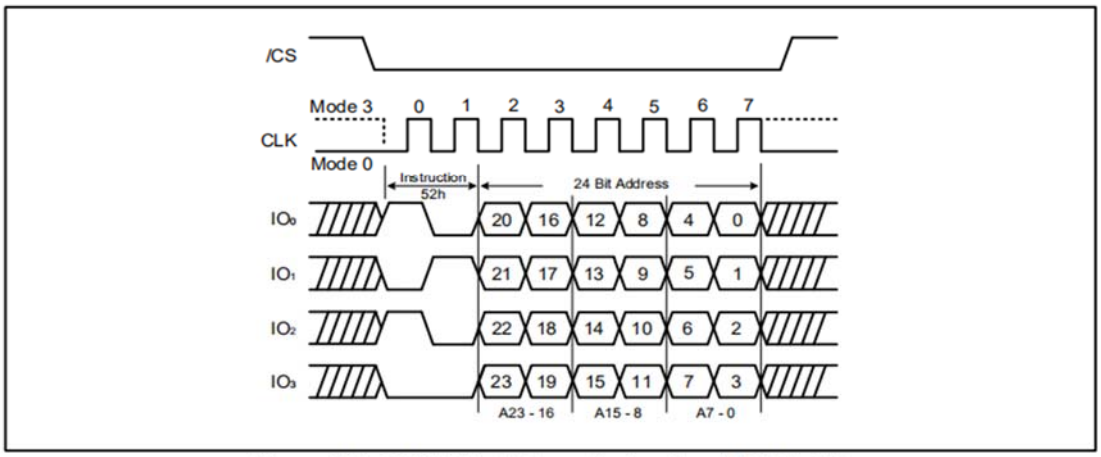


Figure 21b. 32KB Block Erase Instruction (QPI Mode)

9.22 64KB Block Erase (D8h

The Block Erase instruction is to erase the data of the selected block as being “1”. The instruction is used for 64K-byte Block erase operation. Prior to the Block Erase Instruction, a Write Enable instruction must be issued. The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0. (Please refer to figure 22. The /CS pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE2 (See AC Characteristics.

While the Block Erase cycle is in progress, the Read Status Register instruction may still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL bit in the Status Register is cleared to 0. The Block erase instruction will not be executed if the addressed page is protected by the Protect (CMP, SEC, TB, BP2, BP1 and BP0 bits.

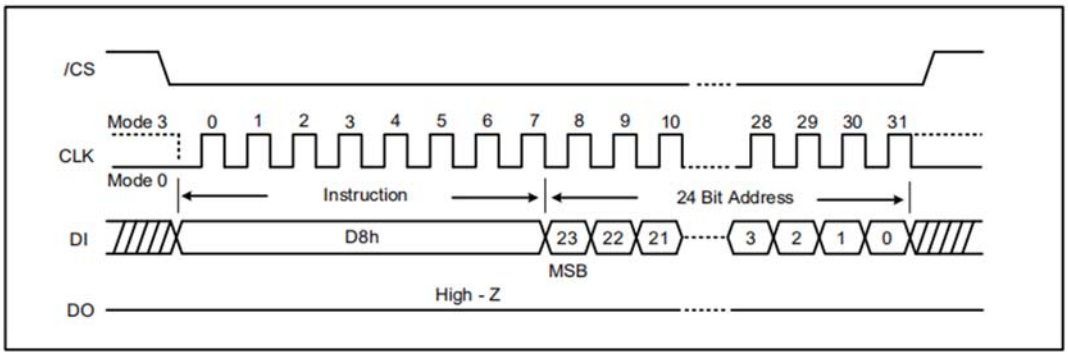


Figure 22a. 64KB Block Erase Instruction (SPI Mode)

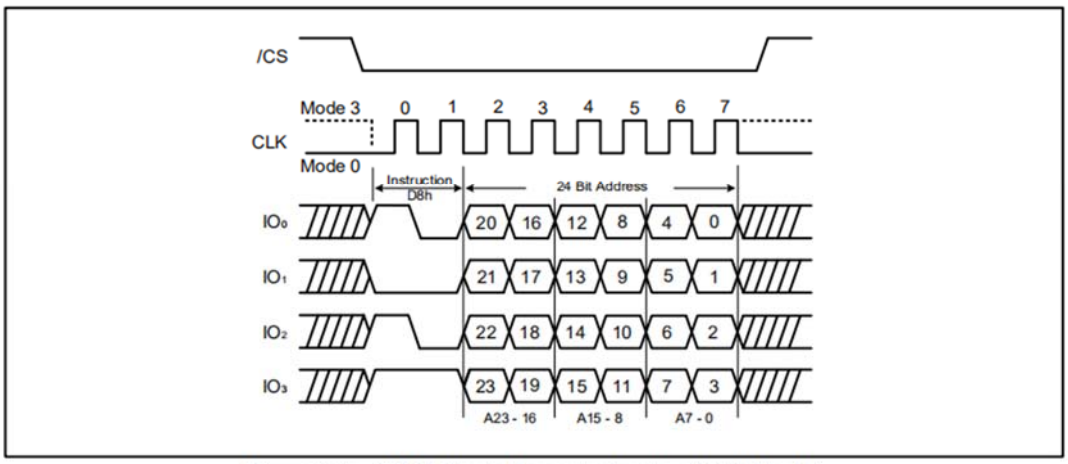


Figure 22b. 64KB Block Erase Instruction (QPI Mode)

9.23 Chip Erase (C7h / 60h

The Chip Erase instruction clears all bits in the device to be FFh (all 1s. Prior to the Chip Erase Instruction, a Write Enable instruction must be issued. The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. (Please refer to figure 23. The /CS pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a duration of tCE (See AC Characteristics.

While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. When the BUSY bit is asserted, the Write Enable Latch (WEL bit in the Status Register is cleared to 0. The Chip erase instruction will not be executed if any page is protected by the Protect (CMP, SEC, TB, BP2, BP1 and BP0 bits.

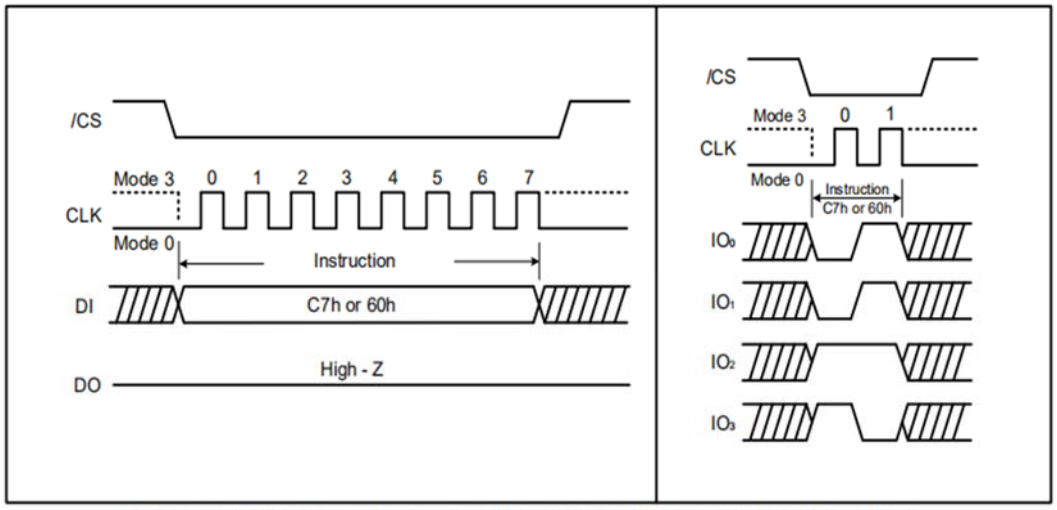


Figure 23. Chip Erase Instruction for SPI Mode (left) and QPI Mode (right)

9.24 Erase / Program Suspend (75h

The Erase/Program Suspend instruction allows the system to interrupt a Sector Erase, Block Erase operation or a Page Program, Quad Page Program operation.
Erase Suspend is valid only during the Sector or Block erase operation. The Write Status Register-1(01h, Write Status Register-2 (31h instruction and Erase instructions (20h, 52h, D8h, C7h, 60h are not allowed during Erase Suspend. During the Chip Erase operation, the Erase Suspend instruction is ignored.
Program Suspend is valid only during the Page Program, Quad Page Program operation. The Write Status Register-1(01h, Write Status Register-2 (31h instruction and Program instructions (02h and 33h are not allowed during Program Suspend.

The Erase/Program Suspend instruction "75h" will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of "tSUS" (See AC Characteristics is required to suspend the erase or program operation. After Erase/Program Suspend, the SUS bit in the Status Register will be set from 0 to 1 immediately and The BUSY bit in the Status Register will be cleared from 1 to 0 within "tSUS". For a previously resumed Erase/Program operation, it is also required that the Suspend instruction "75h" is not issued earlier than a minimum of time of "tSUS" following the preceding Resume instruction "7Ah".

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state. (Please refer to figure 24.

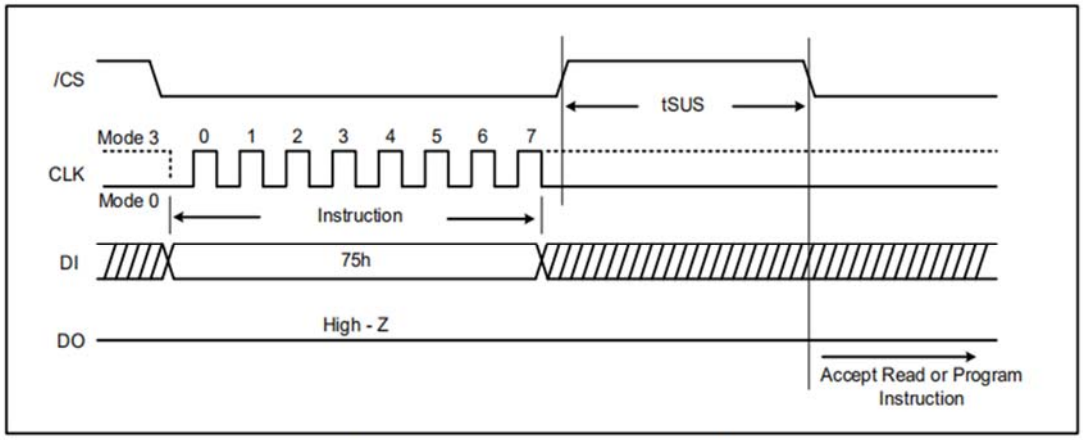


Figure 24a. Erase Suspend instruction (SPI Mode)

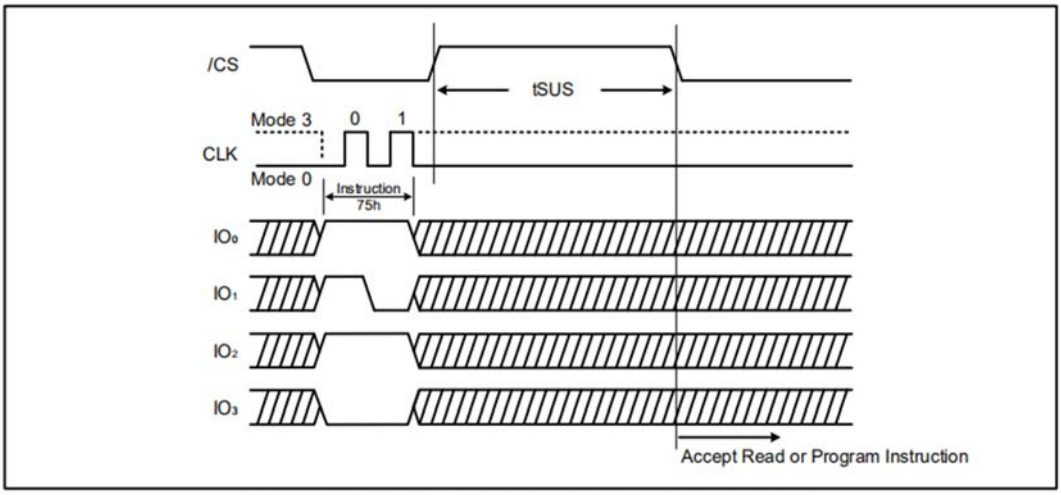


Figure 24b. Erase Suspend instruction (QPI Mode)

9.25 Erase / Program Resume (7Ah

The Erase/Program Resume instruction “7Ah” is to re-work the Sector or Block Erase operation or the Page Program operation upon an Erase/Program Suspend. The Resume instruction ″7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued, the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device.

Resume instruction cannot be accepted if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “tSUS” following a previous Resume instruction. (Please refer to figure 25.

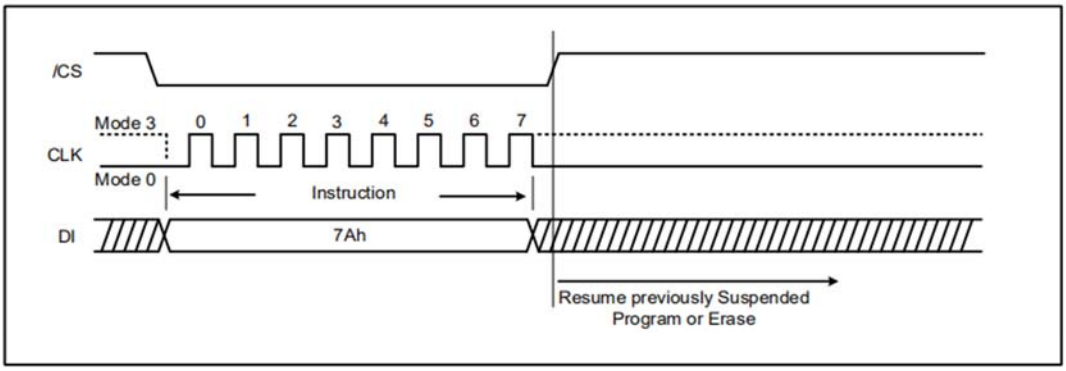


Figure 25a. Erase / Program Resume instruction (SPI Mode)

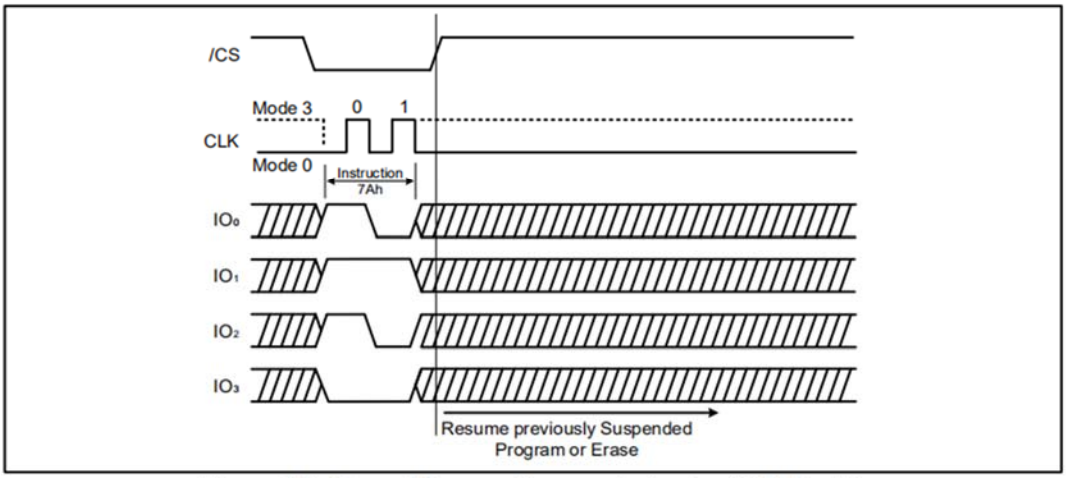


Figure 25b. Erase / Program Resume instruction (QPI Mode)

9.26 Deep Power-down (B9h

Executing the Deep Power-down instruction is the best way to put the device in the lowest power consumption. The Deep Power-down instruction reduces the standby current (from ICC1 to ICC2, as specified in AC characteristics. The instruction is entered by driving the /CS pin low with following the instruction code “B9h”. (Please refer to figure 26.

The /CS pin must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in; otherwise, the Deep Power-down instruction is not executed. After /CS goes high, it requires a delay of tDP and the Deep Power-down mode is entered. While in the Release Deep Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored including the Read Status Register instruction, which is always available during normal operation. Deep Power-down Mode automatically stops at Power-Down, and the device always Power-up in the Standby Mode.

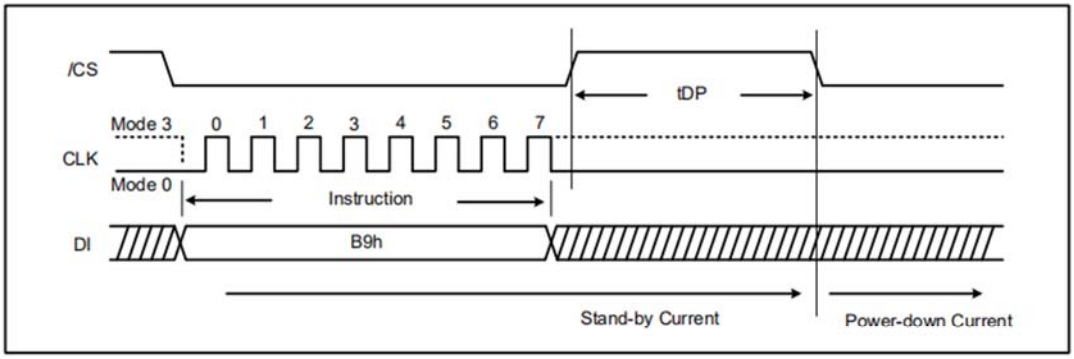


Figure 26a. Deep Power-down Instruction (SPI Mode)

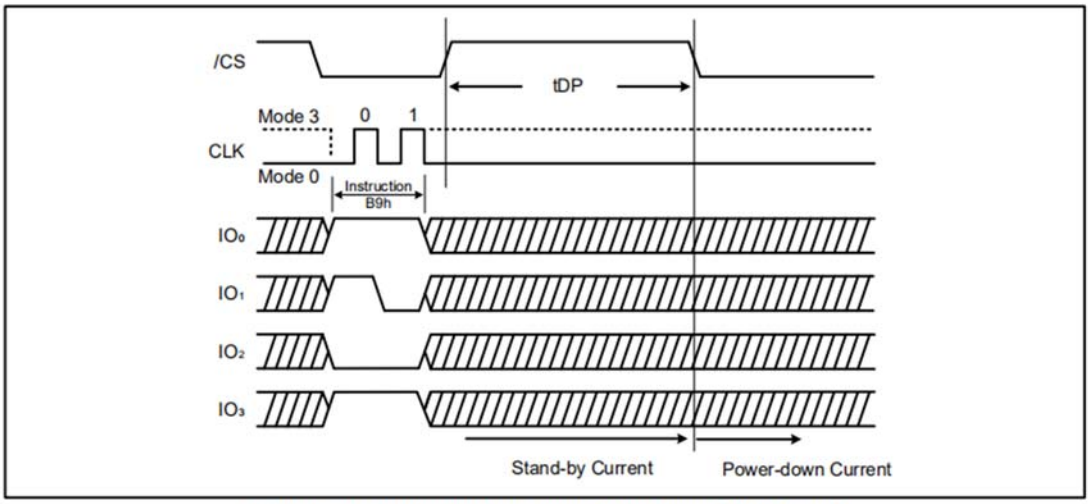


Figure 26b. Deep Power-down Instruction (QPI Mode)

9.27 Release Deep Power-down / Device ID (ABh

The Release Deep Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Deep Power-down state or obtain the device identification(ID.

The instruction is issued by driving the /CS pin low, sending the instruction code “ABh” and driving /CS high as shown in figure 27a & 27b. Release from Deep Power-down require the time duration of tRES1 (See AC Characteristics for re-work a normal operation and accepting other instructions. The /CS pin must keep high during the tRES1 time duration.

To obtain the Device ID in SPI mode, instruction is initiated by driving the /CS pin low and sending the instruction code “ABh” with following 3-dummy bytes. The Device ID bits are then shifted on the falling edge of CLK with most significant bit (MSB first as shown in figure 27c & 27d. After /CS is driven high it must keep high for a time duration of tRES2 (See AC Characteristics. The Device ID can be read continuously. The instruction is completed by driving /CS high.

If the Release from Deep Power-down /Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1 the instruction is ignored and will not have any effects on the current cycle.

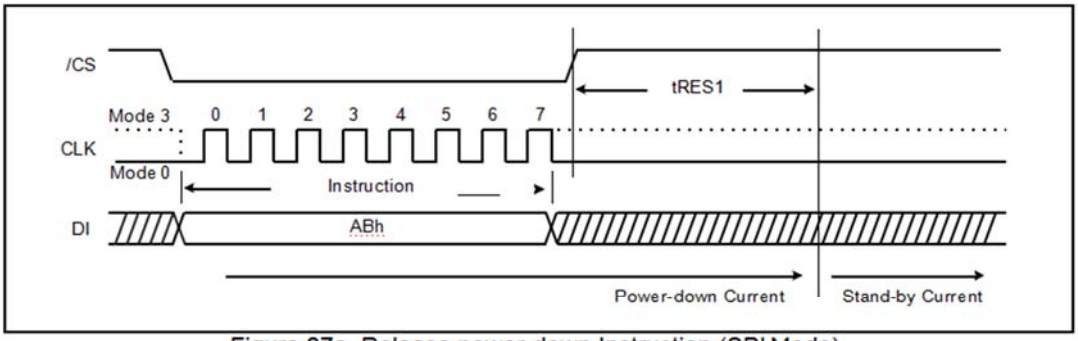


Figure 27a. Release power-down Instruction (SPI Mode)

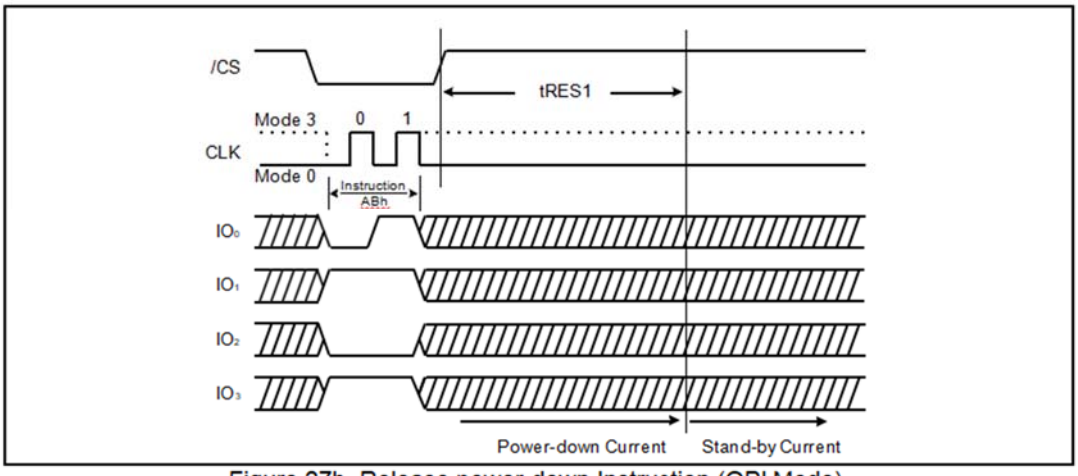


Figure 27b. Release power-down Instruction (QPI Mode)

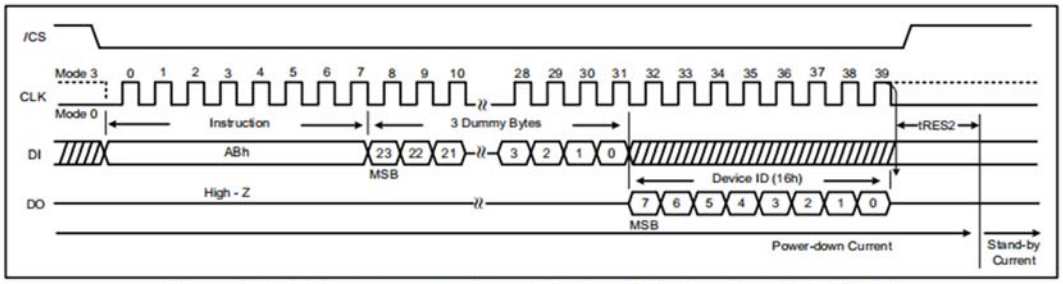


Figure 27c. Release power-down / Device ID Instruction (SPI Mode)

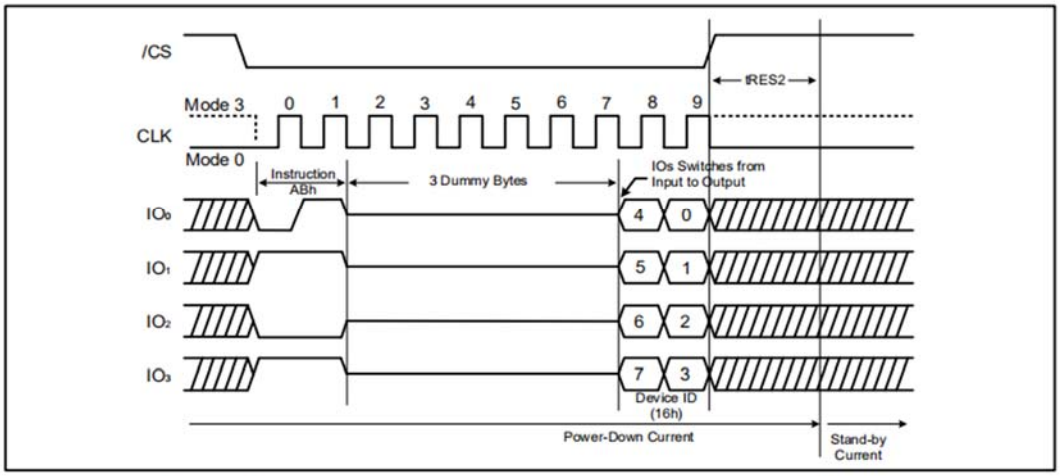


Figure 27d. Release power-down / Device ID Instruction (QPI Mode)

9.28 Read Manufacturer/ Device ID (90h

The Read Manufacturer/ Device ID instruction provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0 of 000000h. After which, the Manufacturer ID(BAh and the Device ID(16h are shifted out on the falling edge of CLK with most significant bit (MSB first as shown in figure 28a & 28b. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

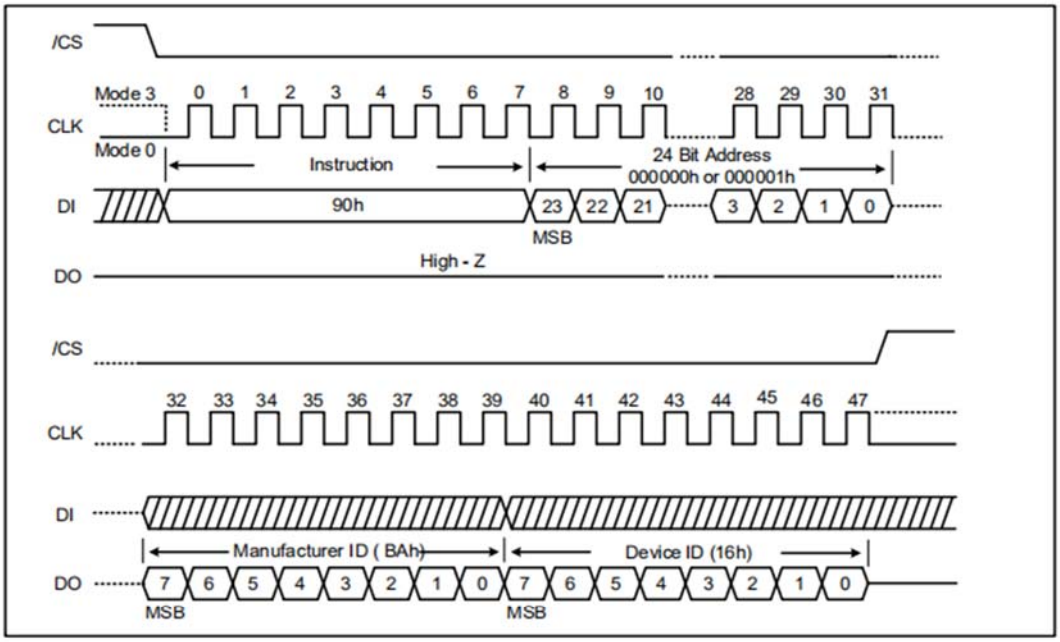


Figure 28a. Read Manufacturer/ Device ID instruction (SPI Mode)

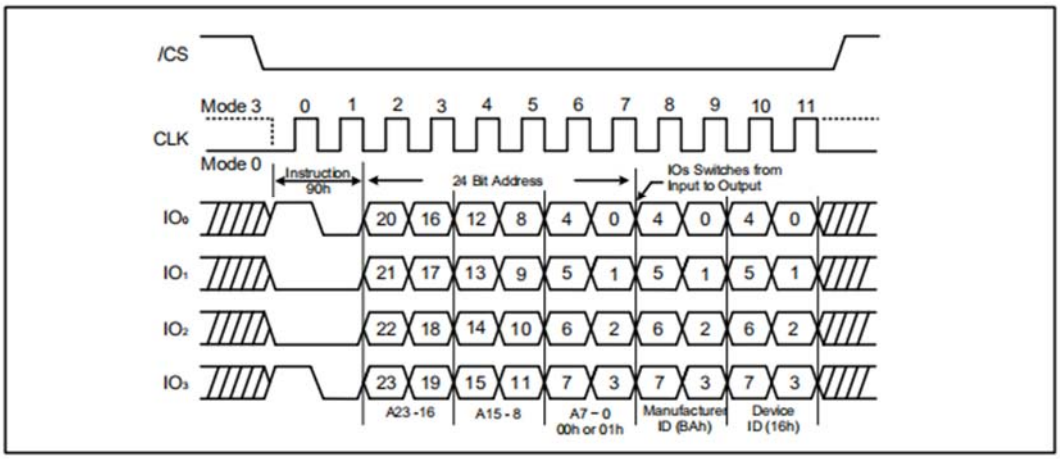


Figure 28b. Read Manufacturer/ Device ID instruction (QPI Mode)

9.29 Read Manufacturer / Device ID Dual I/O (92h

The Read Manufacturer/ Device ID Dual I/O instruction provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID instruction is very similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24-bit address (A23-A0 of 000000h. After which, the Manufacturer ID(BAh and the Device ID(16h are shifted out on the falling edge of CLK with most significant bit (MSB first as shown in figure 29. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

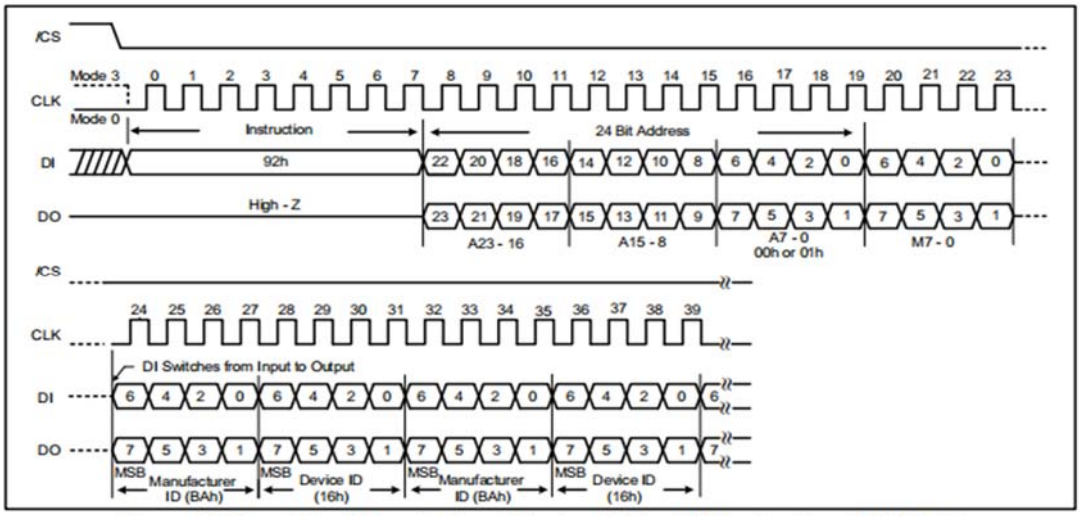


Figure 29. Read Dual Manufacturer/ Device ID Dual I/O instruction (SPI Mode)

9.30 Read Manufacturer / Device ID Quad I/O (94h

The Read Manufacturer/ Device ID Quad I/O instruction provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID instruction is very similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “94h” followed by a 24-bit address (A23-A0 of 000000h. After which, the Manufacturer ID(BAh and the Device ID(16h are shifted out on the falling edge of CLK with most significant bit (MSB first as shown in figure 30. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

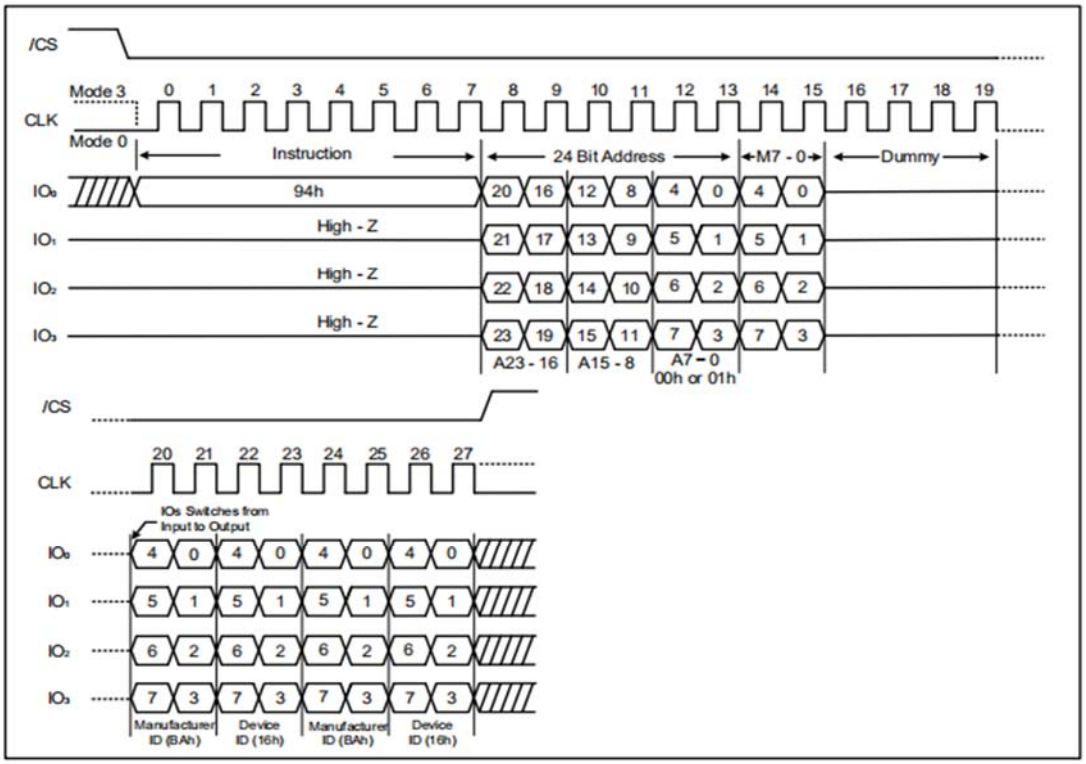


Figure 30. Read Quad Manufacturer/ Device ID Quad I/O instruction (SPI Mode)

9.31 JEDEC ID (9Fh

For compatibility reasons, the ZD25Q64B provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is congruous with the JEDEC standard for SPI compatible serial flash memories that was adopted in 2003. The instruction is entered by driving the /CS pin low with following the instruction code “9Fh”. JEDEC assigned Manufacturer ID byte and two Device ID bytes, Memory Type (ID-15-ID8 and Capacity (ID7-ID0 are then shifted out on the falling edge of CLK with most significant bit (MSB first shown in figure 31. For memory type and capacity values refer to Manufacturer and Device Identification table. The JEDEC ID can be read continuously. The instruction is terminated by driving/CS high.

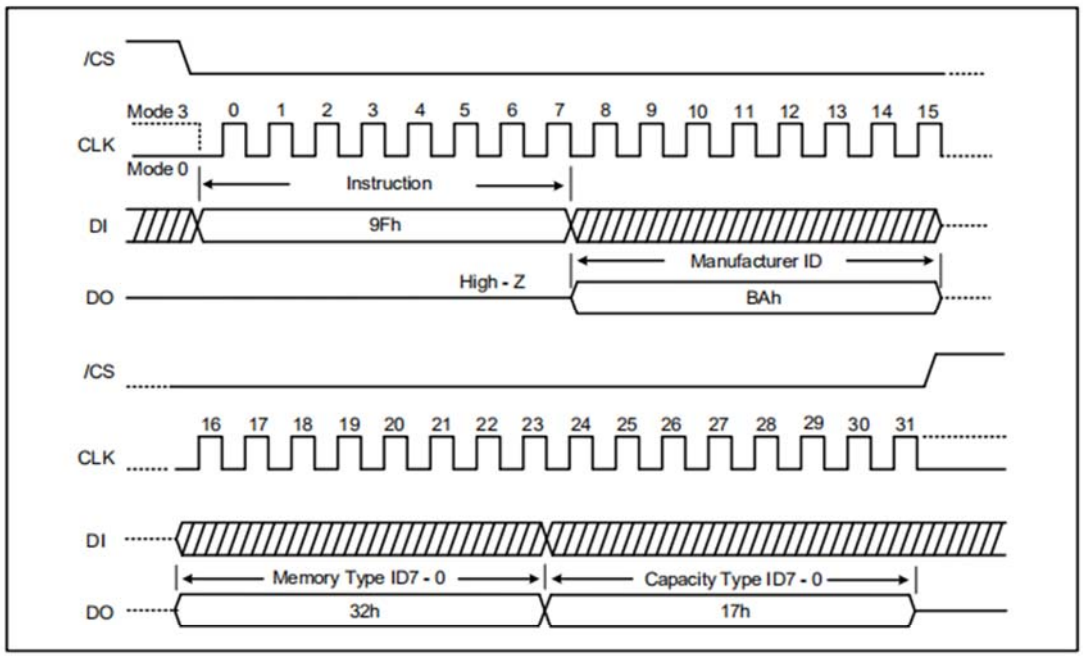


Figure 31a. Read JEDEC ID instruction (SPI Mode)

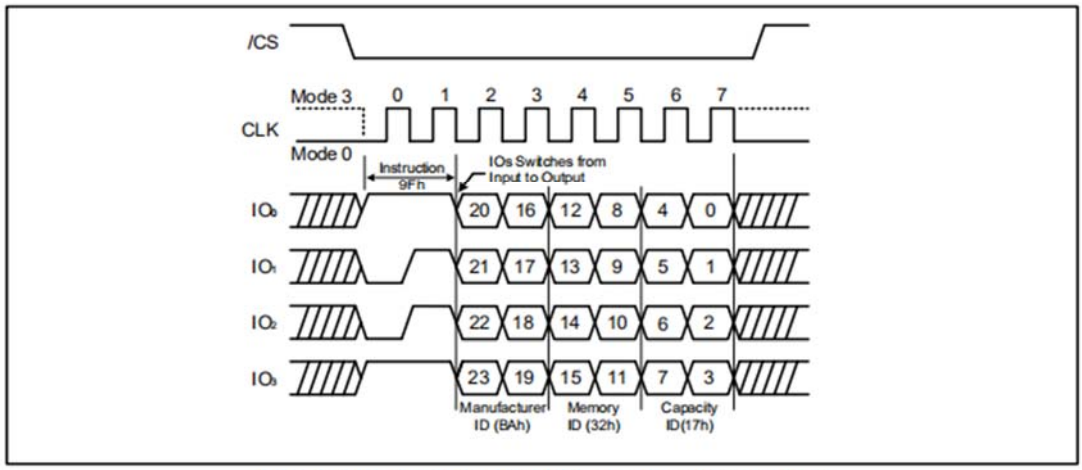


Figure 31b. Read JEDEC ID instruction (QPI Mode)

9.32 Enable QPI (38h

The ZD25Q64B support both Standard/Dual/Quad Serial Peripheral interface (SPI and Quad Peripheral Interface (QPI. However, SPI mode and QPI mode cannot be used at the same time. Enable QPI instruction is the only way to switch the device from SPI mode to QPI mode.

In order to switch the device to QPI mode, the Quad Enable (QE bit in Status Register 2 must be set to 1 first, and an Enable QPI instruction must be issued. If the Quad Enable (QE bit is 0, the Enable QPI instruction will be ignored and the device will remain in SPI mode.
After power-up, the default state of the device is SPI mode. See the instruction Set Table 1-3 for all the commands supported in SPI mode and the instruction Set Table 4 for all the instructions supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

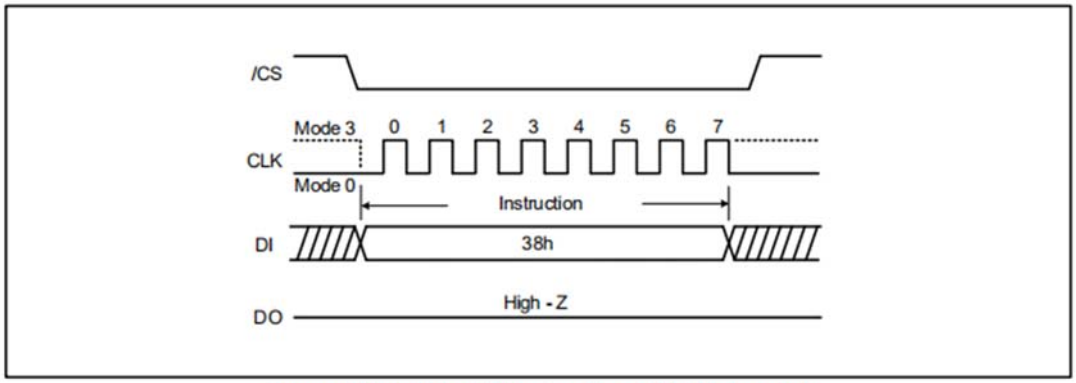


Figure 32. Enable QPI instruction (SPI Mode only)

9.33 Disable QPI (FFh

By issuing Disable QPI (FFh instruction, the device is reset SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

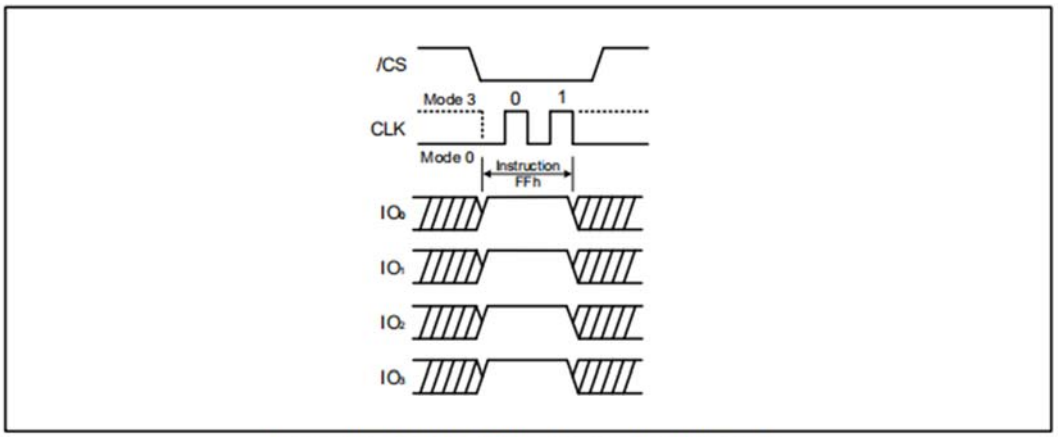


Figure 33. Disable QPI instruction for QPI mode

9.34 Word Read Quad I/O (E7h

The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP directly from the Quad SPI. The Quad Enable bit (QE of Status Register-2 must be set to enable the Word Read Quad I/O instruction. The lowest Address bit (A0 must equal 0 and only two dummy clocks are required prior to the data output.

Continuous Read Mode

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0 after the input Address bits (A23-0, as shown in Figure 34a. The upper nibble of the (M7-4 controls the length of the next Word Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M[3:0] are don't care ("X". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M[7-4]= Ah, then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered does not require the E7h instruction code, as shown in Figure 34b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M[7:4] do not equal to Ah(1,0,1,0 the next instruction (after /CS is raised and then lowered requires the first byte instruction code, thus returning to normal operation.

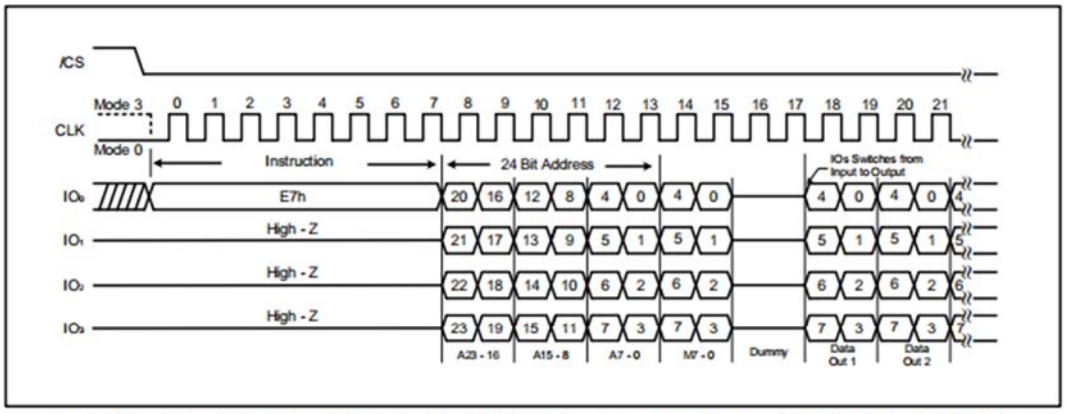


Figure 34a. Word Read Quad I/O instruction (Initial instruction or previous set M7-0 ≠ Axh, SPI Mode)

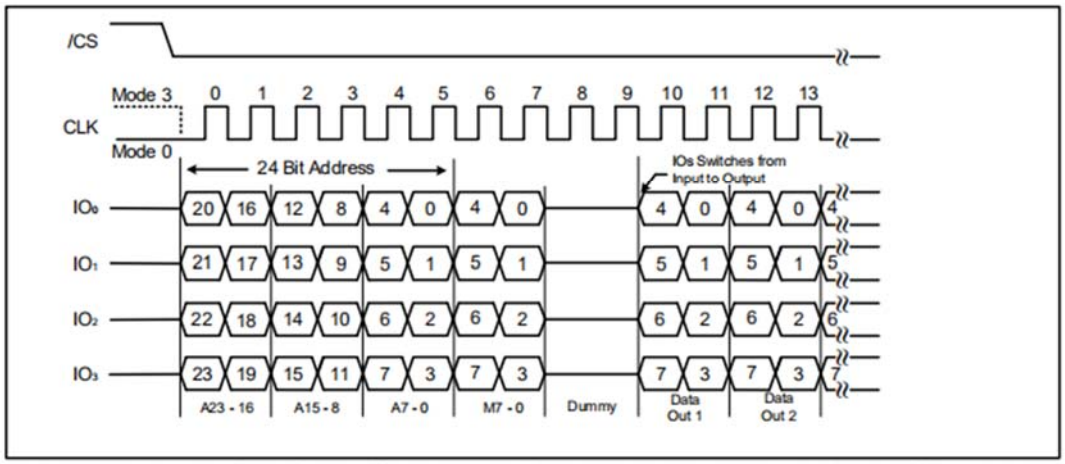


Figure 34b. Word Read Quad I/O instruction (Previous instruction set M7-0= Axh, SPI Mode)

Wrap Around in SPI mode

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a “Set Burst with Wrap” (77h instruction prior to E7h. The “Set Burst with Wrap” (77h instruction can either enable or disable the “Wrap Around” feature for the following E7h commands. When “Wrap Around” is enabled, the output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte of data without issuing read instructions.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 is used to specify the length of the wrap around section within a page. See 10.35 for detail descriptions.

9.35 Set Burst with Wrap (77h

The Set Burst with Wrap (77h instruction is used in conjunction with “Fast Read Quad I/O” and “Word Read Quad I/O” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance. Before the device will accept the Set Burst with Wrap instruction, a Quad enable of Status Register-2 must be executed (Status Register bit QE must equal 1.

The Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Set Burst with Wrap Instruction Sequence. Wrap bit W7 and W3-0 are not used.

W6, W5	W4 = 0		W4 = 1(Default	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O” and Word Read Quad I/O instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction or Reset (99h instruction to reset W4 = 1 prior to any normal Read instructions since ZD25Q64B does not have a hardware Reset Pin.

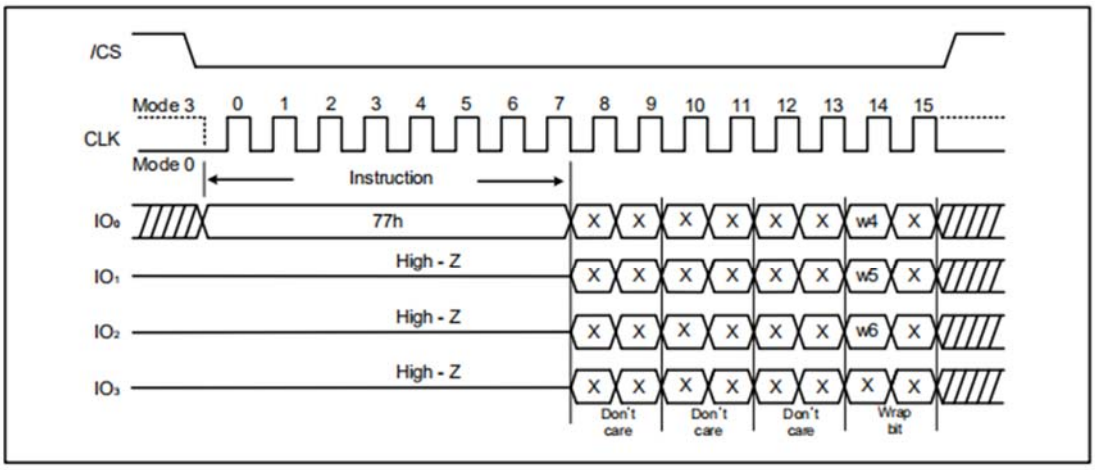


Figure 35. Set Burst with Wrap Instruction Sequence

9.36 Burst Read with Wrap (0Ch

The “Burst Read with Wrap (0Ch” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy of clocks can be configured by the “Set Read Parameters (C0h” instruction.

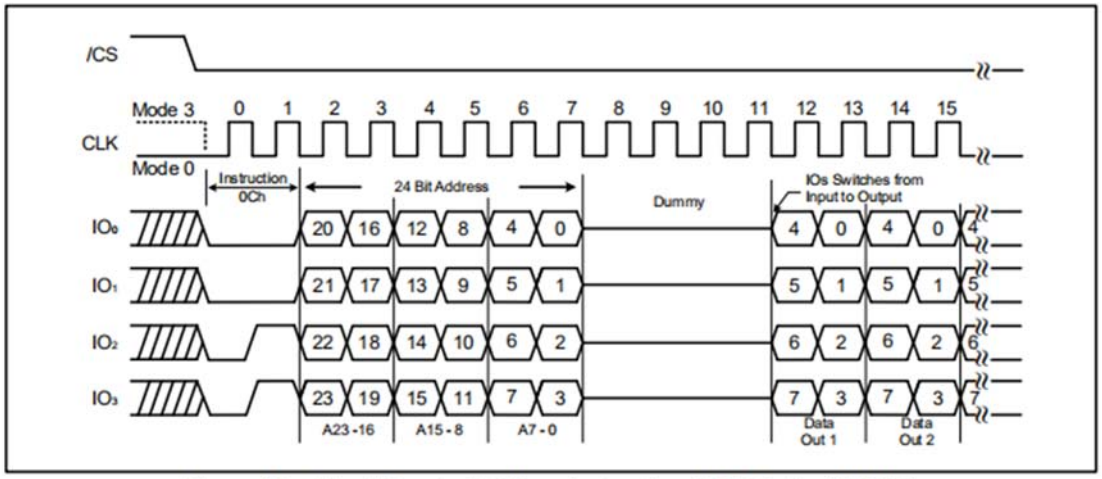


Figure 36a. Burst Read with Wrap instruction (QPI Mode, 80MHz)

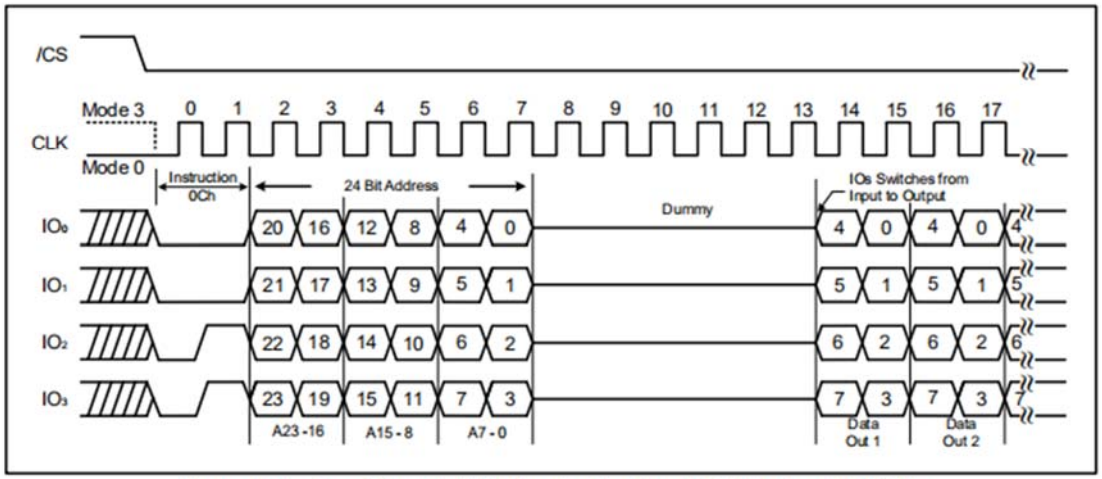


Figure 36b. Burst Read with Wrap instruction (QPI Mode, 108MHz)

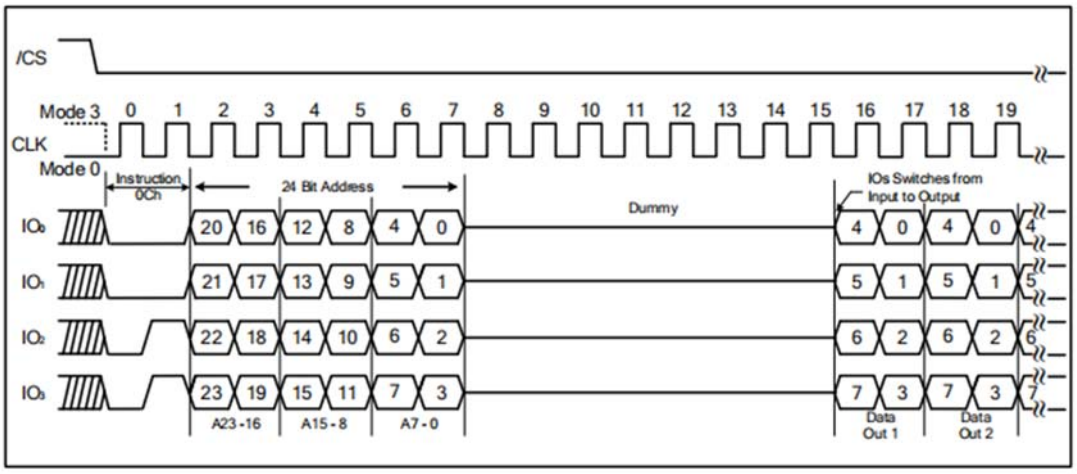


Figure 36c. Burst Read with Wrap instruction (QPI Mode, 133MHz)

9.37 Set Read Parameters (C0h

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h” instruction can be used to configure the number of dummy clocks for “Fast Read (0Bh”, “Fast Read Quad I/O (EBh” & “Burst Read with Wrap (0Ch” instructions, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0Ch” instruction.

In Standard SPI mode, the “Set Read Parameters (C0h” instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer to the instruction. Table 10.2 - 10.5 for details. The “Wrap Length” is set by W6-5 bit in the “Set Burst with Wrap (77h” instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 4.

P5, P4	Dummy Clocks	Maximum Read Freq.		P1, P0	Wrap Length
0 0	4	80MHz		0 0	8-byte
0 1	4	80MHz		0 1	16-byte
1 0	6	108MHz		1 0	32-byte
1 1	8	133MHz		1 1	64-byte

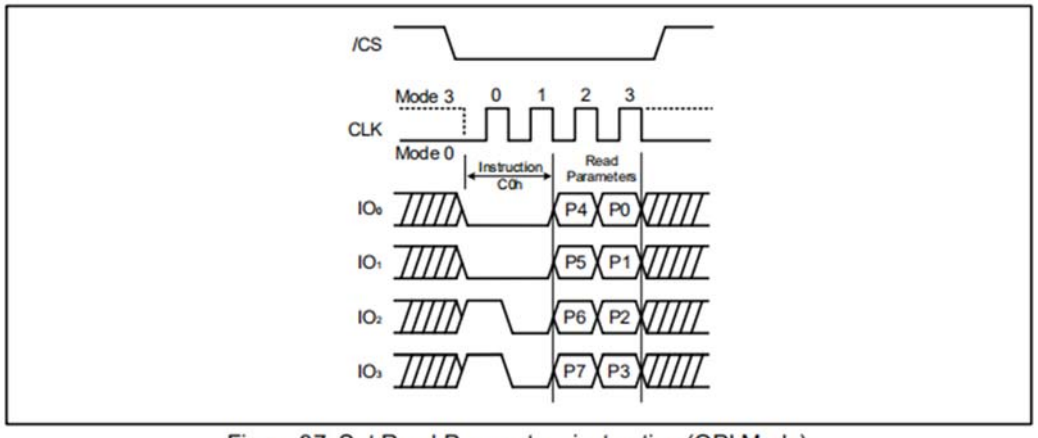


Figure 37. Set Read Parameters instruction (QPI Mode)

9.38 Enable Reset (66h and Reset (99h

Because of the small package and the limitation on the number of pins, the ZD25Q64B provide a software Reset instruction instead of a dedicated RESET pin.

Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL status, Program/Erase Suspend status, Continuous Read Mode bit setting, Read parameter setting and Wrap bit setting.

“Enable Reset (66h” and “Reset (99h” instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other instructions other than “Reset (99h” after the “Enable (66h” instruction will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h” and “Reset (99h” is needed to reset the device. Once the Reset instruction is accepted by the device will take approximately tRST= 30us to reset. During this period, no instruction will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset instruction sequence is accepted by device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset instruction sequence.

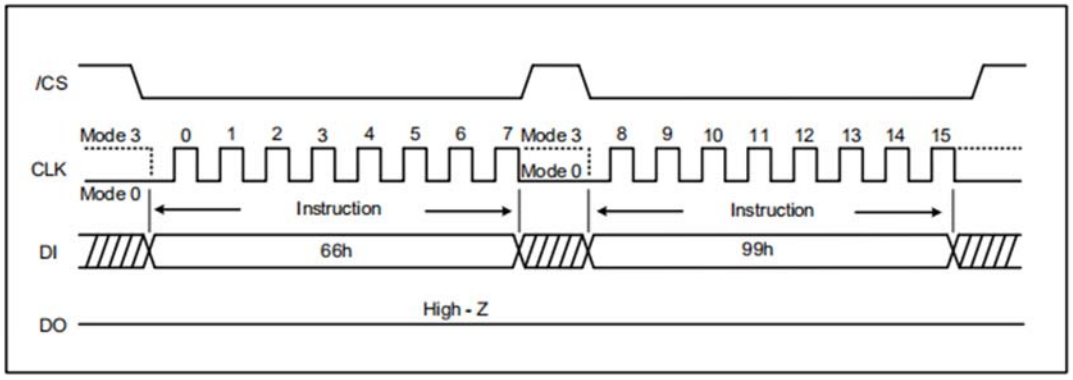


Figure 38a. Enable Reset and Reset Instruction (SPI Mode)

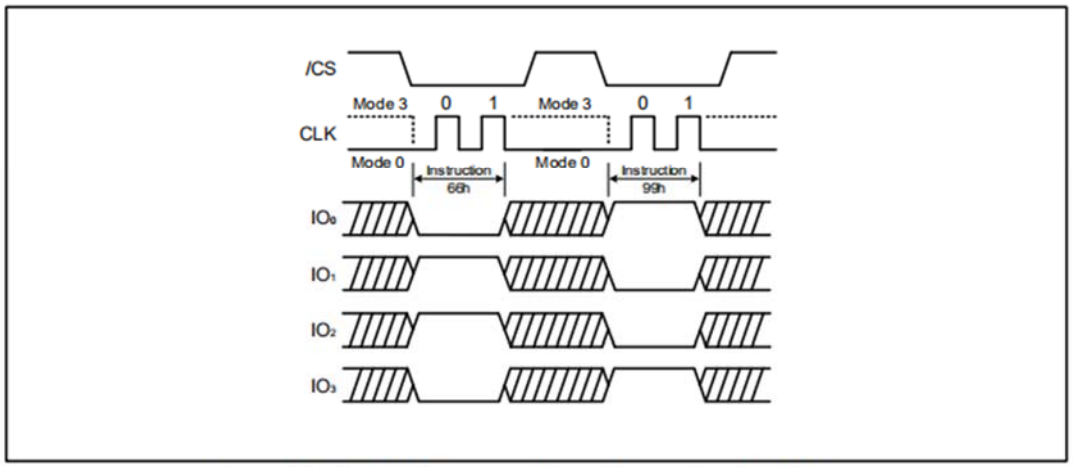


Figure 38b. Enable Reset and Reset Instruction (QPI Mode)

9.39 Read Serial Flash Discovery Parameter (5Ah

The Read Serial Flash Discovery Parameter (SFDP instruction allows reading the Serial Flash Discovery Parameter area (SFDP. This SFDP area is composed of 2048 read-only bytes containing operating characteristics and vendor specific information. The SFDP area is factory programmed. If the SFDP area is blank, the device is shipped with all the SFDP bytes at FFh. If only a portion of the SFDP area is written to, the portion not used is shipped with bytes in erased state (FFh. The instruction sequence for the read SFDP has the same structure as that of a Fast Read instruction. First, the device is selected by driving Chip Select (/CS Low. Next, the 8-bit instruction code (5Ah and the 24-bit address are shifted in, followed by 8 dummy clock cycles. The bytes of SFDP content are shifted out on the Serial Data Output (DO starting from the specified address. Each bit is shifted out during the falling edge of Serial Clock (CLK. The instruction sequence is shown here. The Read SFDP instruction is terminated by driving Chip Select (/CS High at any time during data output.

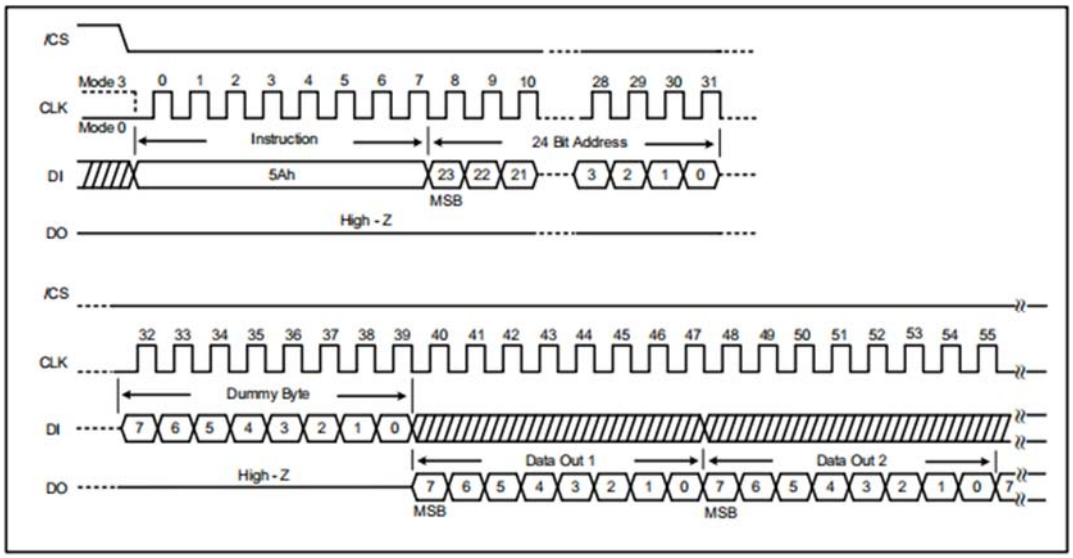


Figure 39. Read SFDP Register Instruction

Read Serial Flash Discovery Parameter (SFDP

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
00h	53h	SFDP Signature	SFDP Signature =50444653h
01h	46h	SFDP Signature	
02h	44h	SFDP Signature	
03h	50h	SFDP Signature	
04h	01h	SFDP Minor Revisions	SFDP revision 1.1
05h	01h	SFDP Major Revisions	
06h	00h	Number of Parameter Header(NPH	1 Parameter Header
07h	FFh	Reserved	
08h	BAh	PID(0(3 : Manufacture JEDEC ID	BAh
09h	00h	PID(0 : Serial Flash Basics Minor Revisions	Serial Flash Basics Revision 1.0
0Ah	01h	PID(0 : Serial Flash Basics Major Revisions	
0Bh	04h	PID(0 : Serial Flash Basics Length	4 Dwords (2
0Ch	80h	PID(0 : Address of Parameter ID(0 Table (A7-A0	PID(0 Table Address = 000080h
0Dh	00h	PID(0 : Address of Parameter ID(0 Table (A15-A8	
0Eh	00h	PID(0 : Address of Parameter ID(0 Table (A23-A16	
0Fh	FFh	Reserved	
... (1	FFh	Reserved	
80h	E5h	Bit[7:5] = 111 Reserved	
		Bit[4:3] = 00 Non-volatile Status Register	
		Bit[2] = 1 Page Programmable	
		Bit[1:0] = 01 Support 4KB Erase	

Read Serial Flash Discovery Parameter (SFDP (cont'd

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
81h	20h	Opcode for 4K-Byte Erase	
82h	F1h	Bit[7] = 1 Reserved	
		Bit[6] = 1 Supports Single Input Quad Output	
		Bit[5] = 1 Supports Quad Input Quad Output	
		Bit[4] = 1 Supports Dual Input Dual Output	
		Bit[3] = 0 Dual Transfer Rate not Supported	
		Bit[2:1] = 00 3-Byte/24-Bit Addressing	
		Bit[0] = 1 Supports Single Input Dual Output	
83h	FFh	Reserved	
84h	FFh	Flash Size in Bits	64 Mega Bits = 03FFFFFFh
85h	FFh	Flash Size in Bits	
86h	FFh	Flash Size in Bits	
87h	03h	Flash Size in Bits	
88h	44h	Bit[7:5] = 010 8 Mode Bits are needed	Fast Read Quad I/O Setting
		Bit[4:0] = 00100 16 Dummy Bits are needed	
89h	EBh	Opcode for Quad Input Quad Output Fast Read	
8Ah	08h	Bit[7:5] = 000 No Mode Bits are needed	Fast Read Quad Output Setting
		Bit[4:0] = 01000 8 Dummy Bits are needed	
8Bh	6Bh	Opcode for Single Input Quad Output Fast Read	
8Ch	08h	Bit[7:5] = 000 No Mode Bits are needed	Fast Read Dual Output Setting
		Bit[4:0] = 01000 8 Dummy Bits are needed	
8Dh	3Bh	Opcode for Single Input Dual Output Fast Read	
8Eh	80h	Bit[7:5] = 100 8 Mode Bits are needed	Fast Read Dual I/O Setting
		Bit[4:0] = 00000 No Dummy Bits are needed	
8Fh	BBh	Opcode for Dual Input Dual Output Fast Read	
90h	FEh	Bit[7:5]= 111 Reserved	Fast Read in QPI mode
		Bit[4]=1 Supports Quad input opcode & address and quad output data Fast Read	
		Bit[3:1]=111 Reserved	
		Bit[0]=0 Not support Dual Input opcode & address	

		and dual output data Fast Read	
91h	FFh	Reserved	
92h	FFh	Reserved	
93h	FFh	Reserved	
94h	FFh	Reserved	Fast Read Dual I/O in QPI Setting
95h	FFh	Reserved	
96h	00h	Bit[7:5]=000 No Mode Bits are needed	
		Bit[4:0]=00000 No Dummy Bits are needed	
97h	FFh	Reserved. Opcode Not to be supported.	
98h	FFh	Reserved	Fast Read Quad I/O in QPI Setting
99h	FFh	Reserved	
9Ah	44h	Bit[7:5]=010 8 Mode Bits are needed	
		Bit[4:0]=00100 8 Dummy Bits are needed(≤80Mhz	
9Bh	EBh	Opcode for Quad Input Quad Output Fast Read in QPI mode	
9Ch	0Ch	Sector type 1 size= 4Kbytes	Erase for Sector Type 1/2
9Dh	20h	Opcode for Erase of Sector Type 1	
9Eh	0Fh	Sector type 2 size= 32Kbytes	
9Fh	52h	Opcode for Erase of Sector Type 2	
A0h	10h	Sector type 3 size= 64Kbytes	Erase for Sector Type 3/4
A1h	D8h	Opcode for Erase of Sector Type 3	
A2h	00h	Sector type 4 size not to exist	
A3h	FFh	Reserved. Opcode Not to be supported.	
...(1	FFh	Reserved	
E8h-EFh	xxh	Reserved	
F0h-FFh	xxh	Reserved	

Notes:

1. Data stored in Byte Address 10h to 7Fh & A4 to 90h to FFh are reserved, the value isFFh.
2. 1 Dword = 4 Bytes.
3. PID(x = Parameter Identification Table(x

10. 40 Enter Secured OTP (B1h

The Enter Secured OTP instruction is for entering the additional 4K-bit secured OTP mode. The additional 4K-bit secured OTP is independent from main array, which may be used to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down

Please note that Write Status Register-1, Write Status Register-2 and Write Security Register instructions are not acceptable during the access of secure OTP region. Once security OTP is lock down, only commands related with read are valid.
The Enter Secured OTP instruction sequence is shown in figure 40.

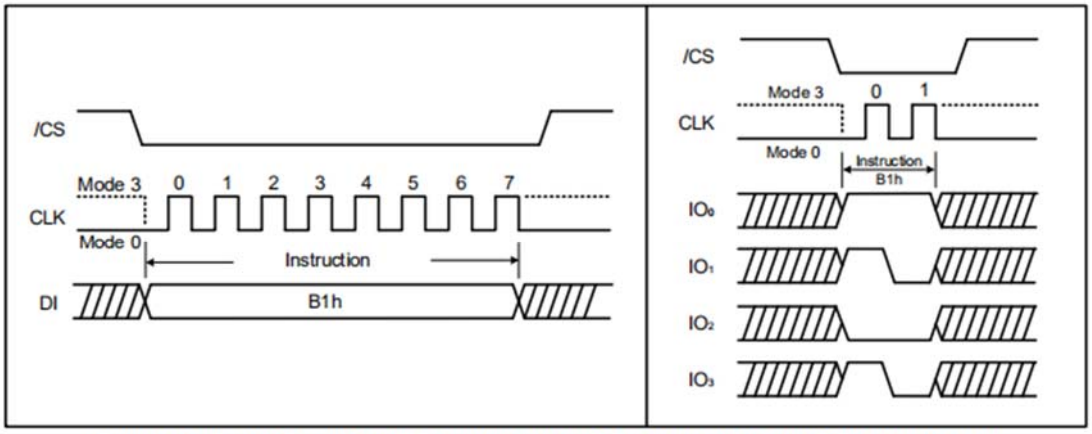


Figure 40. Enter Secured OTP instruction for SPI Mode (left) and QPI Mode (right)

10.41 Exit Secured OTP (C1h

The Exit Secured OTP instruction is for exiting the additional 4K-bit secured OTP mode.
(Please refer to figure 41.

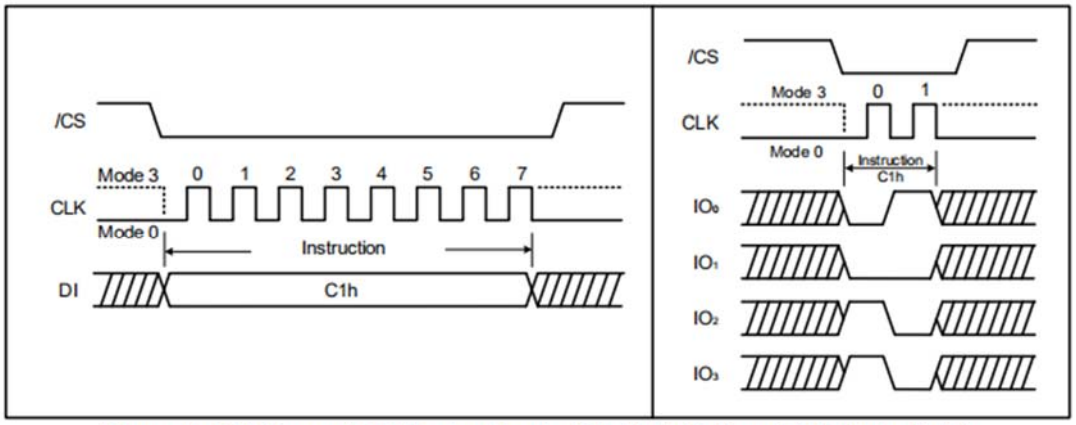


Figure 41. Exit Secured OTP instruction for SPI Mode (left) and QPI Mode (right)

10.42 Read Security Register (2Bh

The Read Security Register can be read the value of Security Register bits at any time (even in program/erase/write status register-1 and write status register-2 condition and continuously.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex-factory or not. When it is “0”, it indicates non-factory lock, “1” indicates factory-lock.

Lock-down Secured OTP (LDSO bit. By writing Write Security Register instruction, the LDSO bit may be set to “1” for customer lock-down purpose. However, once the bit it set to “1” (Lock-down, the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more. While it is in 4K-bit Secured OTP mode, array access is not allowed to write.

Security Register Definition

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x	x	x	x	x	x	LDSO (indicate if lock-down	Secured OTP indicator bit
reserved	reserved	reserved	reserved	reserved	reserved	0 = not lock-down 1 = lock-down(can not program/erase OTP	0 = non factory lock 1 = factory lock
Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non-Volatile bit	Non-Volatile bit

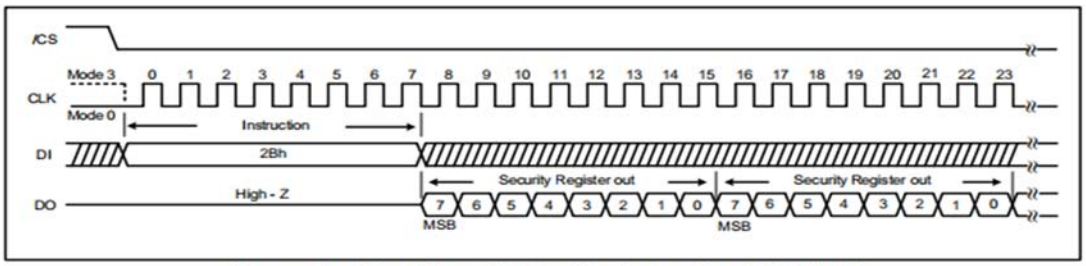


Figure 42a. Read Security Register instruction (SPI Mode)

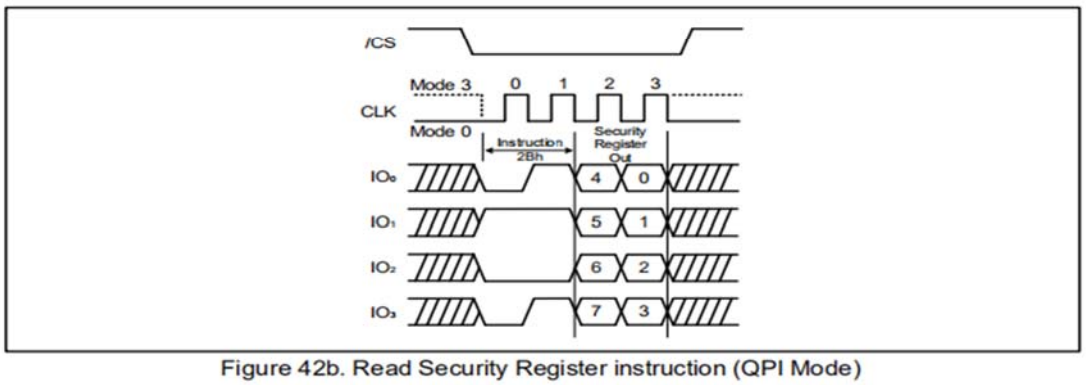


Figure 42b. Read Security Register instruction (QPI Mode)

10.43 Write Security Register (2Fh

The Write Security Register instruction is for changing the values of Security Register bits. Unlike Write Status Register, the Write Enable instruction is not required before writing Write Security Register instruction. The Write Security Register instruction may change the value of bit1 (LDSO bit for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to “1”, the Secured OTP area cannot be updated any more.

The /CS must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

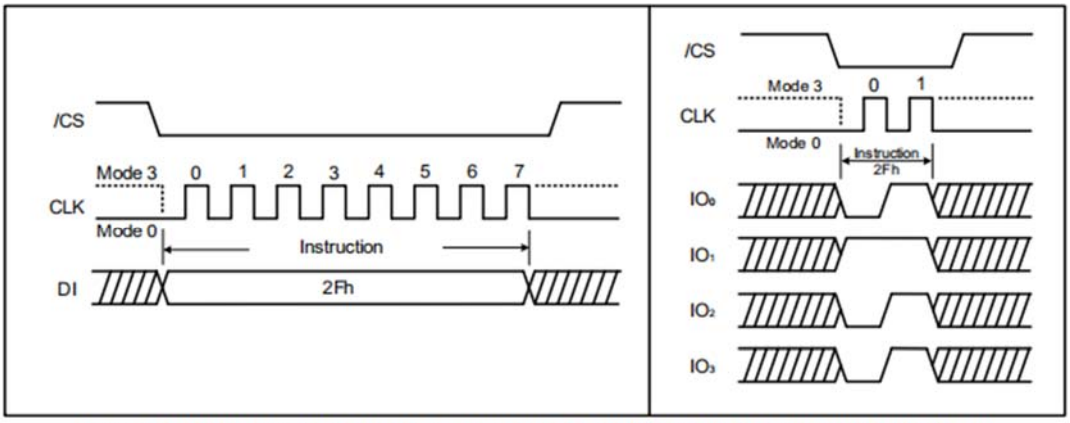


Figure 43. Write Security Register instruction for SPI Mode (left) and QPI Mode (right)

11. 4K-bit Secured OTP

It's for unique identifier to provide 4K-bit one-time-program area for setting device unique serial number which may be set by factory or system customer. Please refer to table of "4K-bit secured OTP definition".

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command
- Customer may lock-down bit1 as "1". Please refer to "table of security register definition" for security register bit definition and table of "4K-bit secured OTP definition" for address range definition.
- Note. Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed to write.

4K-bit secured OTP definition

Address range	Size	Standard Factory Lock	Customer Lock
000000 ~ 00000F	128-bit	ESN (Electrical Serial Number	Determined by customer
000010 ~ 0001FF	3968-bit	N/A	

12. ELECTRICAL CHARACTERISTICS

12.1 Absolute Maximum Ratings (1

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		-0.6 to VCC+0.4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	-0.6 to VCC +0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	-2.0V to VCC +2.0V	V
Storage Temperature	TSTG		-65 to +150	˚C
Lead Temperature	TLEAD		See Note(2	˚C
Electrostatic Discharge Voltage	VESD	Human Body Model(3	-2000 to +2000	V

Notes:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green assembly and the European directive on restrictions on hazardous substances (RoHS 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms.

12.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Erase/Program Cycles	VCC	FR = 133MHz (Single/Dual/Quad SPI fR = 50MHz (Read Data 03h	2.7	3.6	V
Temperature,Operating	T_A	Industrial	-40	+85	˚C

12.3 Endurance and Data Retention

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Erase/Program Cycles	4KB sector, 32/64KB block or full chip.	100,000		Cycles
Data Retention	Full Temperature Range		20	years

12.4 Power-up Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC(min to /CS Low	tVSL(1	10		μs
Time Delay Before Write Instruction	tPUW(1	1	10	ms
Write Inhibit Threshold Voltage	VWI(1	1	2	V

Note:

1. These parameters are characterized only.

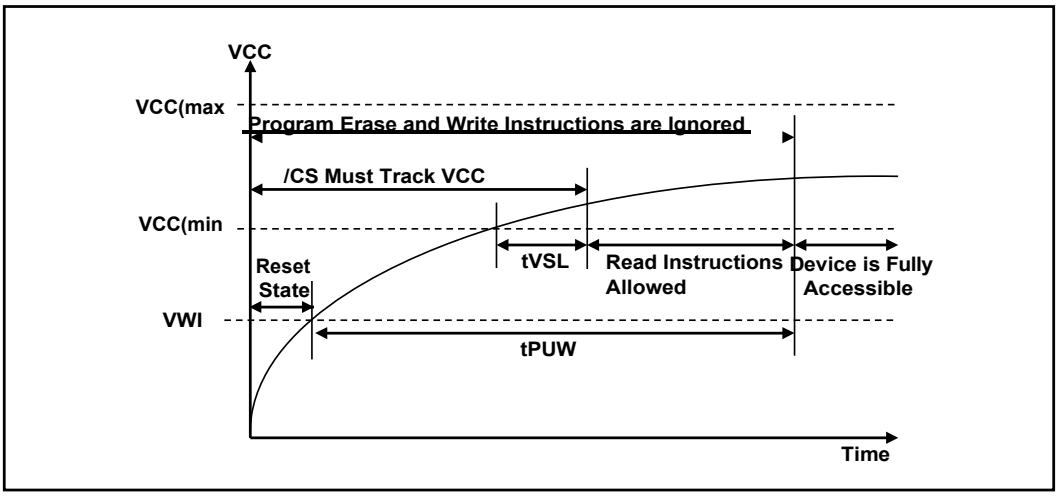


Figure 44. Power-up Timing and Voltage Levels

12.5 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITION	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	CIN(1	VIN=0V(2			6	pF
Output Capacitance	COUT(1	VOUT=0V(2			8	pF
Input Leakage	ILI				±2	μA
I/O Leakage	ILO				±2	μA
Standby Current	ICC1	/CS=VCC VIN=GND or VCC		10	50	μA
Power-down Current	ICC2	/CS=VCC VIN=GND or VCC		2	20	μA
Current Read Data/ Dual/Quad 1MHz(2	ICC3	C=0.1 VCC / 0.9VCC IO=Open			7	mA
Current Read Data/ Dual/Quad 50MHz(2	ICC3	C=0.1 VCC / 0.9VCC IO=Open			15	mA
Current Read Data/ Dual/Quad 80MHz(2	ICC3	C=0.1 VCC / 0.9VCC IO=Open			18	mA
Current Read Data/ Dual/Quad 104MHz(2	ICC3	C=0.1 VCC / 0.9VCC IO=Open			20	mA
Current Read Data/ Dual/Quad 133MHz(2	ICC3	C=0.1 VCC / 0.9VCC IO=Open			27	mA
Current Write Status Register	ICC4	/CS=VCC		10	20	mA
Current page Program	ICC5	/CS=VCC		15	25	mA
Current Sector/Block Erase	ICC6	/CS=VCC		15	25	mA
Current Chip Erase	ICC7	/CS=VCC		15	25	mA
Input Low Voltages	VIL		-0.5		VCC x0.2	V
Input High Voltages	VIH		VCC x0.8		VCC +0.4	V
Output Low Voltages	VOL	IOL= 100μA			0.2	V
Output High Voltages	VOH	IOH=-100μA	VCC -0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data, TA = 25°C, VCC = 3V.
2. Checked Board Pattern.

12.6 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.2 VCC to 0.8 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

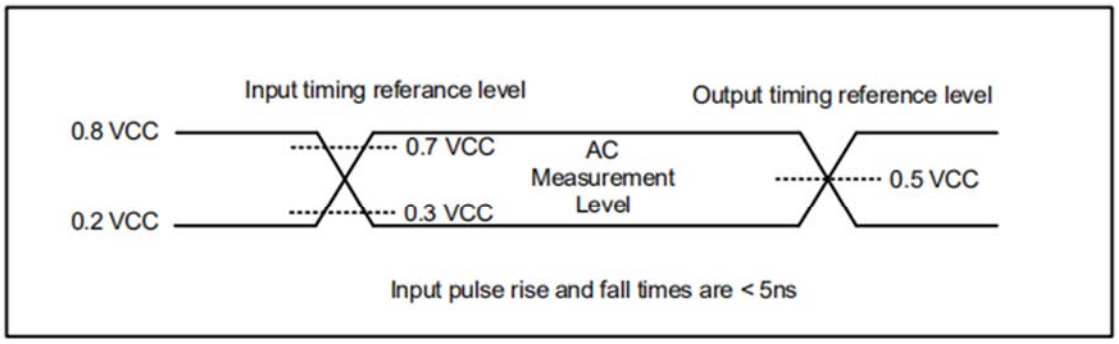


Figure 45. AC Measurement I/O Waveform

12.7 AC Electrical Characteristics

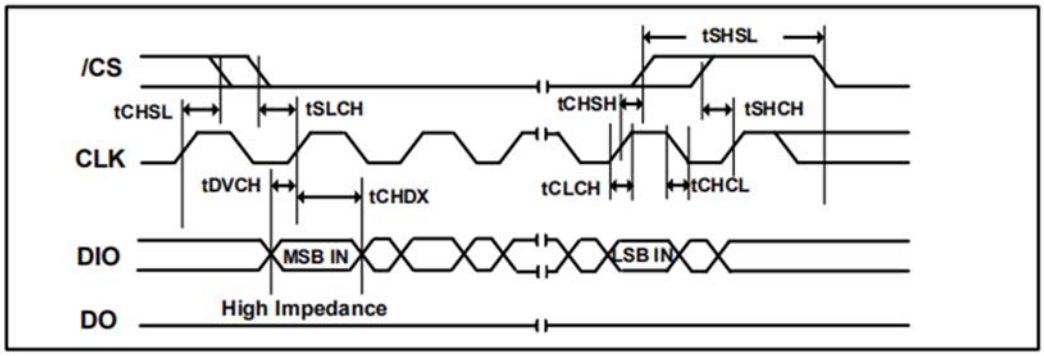
DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency For all instructions, except Read Data (03h 2.7V-3.6V VCC & Industrial Temperature	F_R	f_c	D.C.		133	MHz
Clock freq. Read Data instruction (03h	f_R		D.C.		50	MHz
Clock High, Low Time except Read Data (03h	tCLH, tCLL(1		3.5			ns
Clock High, Low Time for Read Data (03h instructions	tCRLH, tCRLL(1		8			ns
Clock Rise Time peak to peak	tCLCH(2		0.1			V/ns
Clock Fall Time peak to peak	tCHCL(2		0.1			V/ns
/CS Active Setup Time relative to CLK	tSLCH	tCSS	5			ns
/CS Not Active Hold Time relative to CLK	tCHSL		5			ns
Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	3			ns
/CS Active Hold Time relative to CLK	tCHSH		5			ns
/CS Not Active Setup Time relative to CLK	tSHCH		5			ns
/CS Deselect Time (for Read instructions/ Write, Erase and Program instructions	tSHSL	tCSH	30			ns
Output Disable Time	tSHQZ(2	tDIS			7	ns
Clock Low to Output Valid	tCLQV	tV1			6	ns
Clock Low to Output Valid (Except Main Read (3	tCLQV	tV2			7	ns
Output Hold Time	tCLQX	tHO	0			ns
/Hold Active Setup Time relative to CLK	tHLCH		5			ns

12.8 AC Electrical Characteristics (cont'd

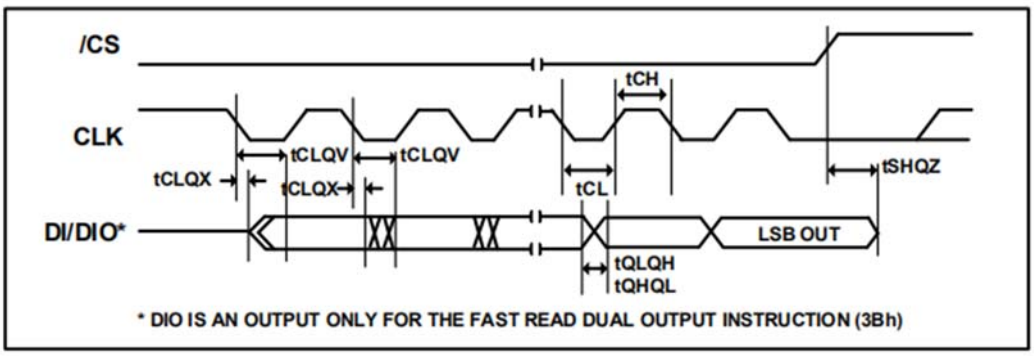
DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Active Hold Time relative to CLK	tCHHH		5			ns
/HOLD Not Active Setup Time relative to CLK	tHHCH		5			ns
/HOLD Not Active Hold Time relative to CLK	tCHHL		5			ns
/HOLD to Output Low-Z	tHHQX(2	t_{LZ}			7	ns
/HOLD to Output High-Z	tHLQZ(2	t_{HZ}			12	ns
Write Protect Setup Time Before /CS Low	tWHSL(4		20			ns
Write Protect Setup Time After /CS High	tSHWL(4		100			ns
/CS High to Power-down Mode	tDP(2				3	μs
/CS High to Standby Mode without Electronic Signature Read	tRES1(2				3	μs
/CS High to Standby Mode with Electronic Signature Read	tRES2(2				1.8	μs
/CS High to next Instruction after Suspend	tSUS(2				20	μs
CS High to next Instruction after Reset	tRST(2				30	μs
Write Status Register Time	tw			5	15	ms
Byte Program Time	t_{BP}			5	150	μs
Page Program Time	t_{PP}			0.6	5	ms
Sector Erase Time(4KB	t_{SE}			0.06	0.4	s
Block Erase Time(32KB	t_{BE1}			0.2	1.5	s
Block Erase Time(64KB	t_{BE2}			0.3	2	s
Chip Erase Time	t_{CE}			30	150	s

Notes:
1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Contains: Read Status Register-1,2/ Read Manufacturer/Device ID, Dual, Quad/ Read JEDEC ID/ Read Security Register/ Read Serial Flash Discovery Parameter.
4. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1.
5. Commercial temperature only applies to Fast Read (F_R. Industrial temperature applies to all other parameters.

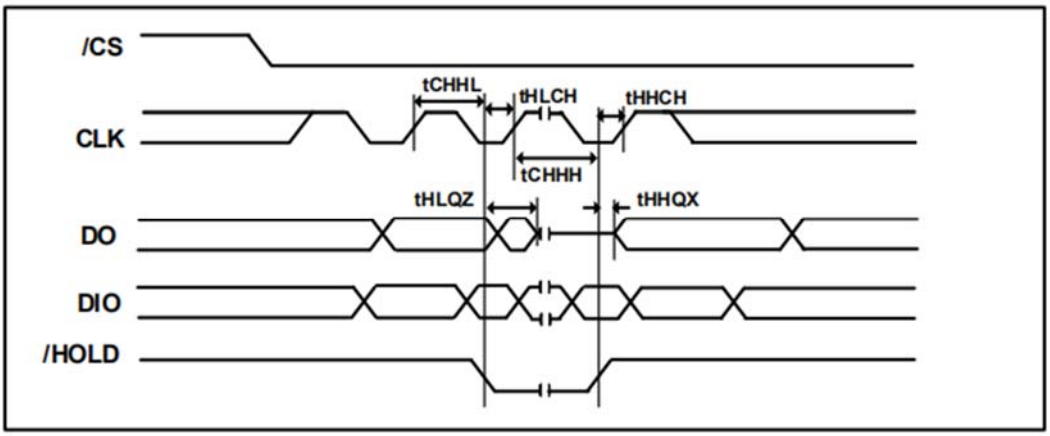
12.9 Input Timing



12.10 Output Timing

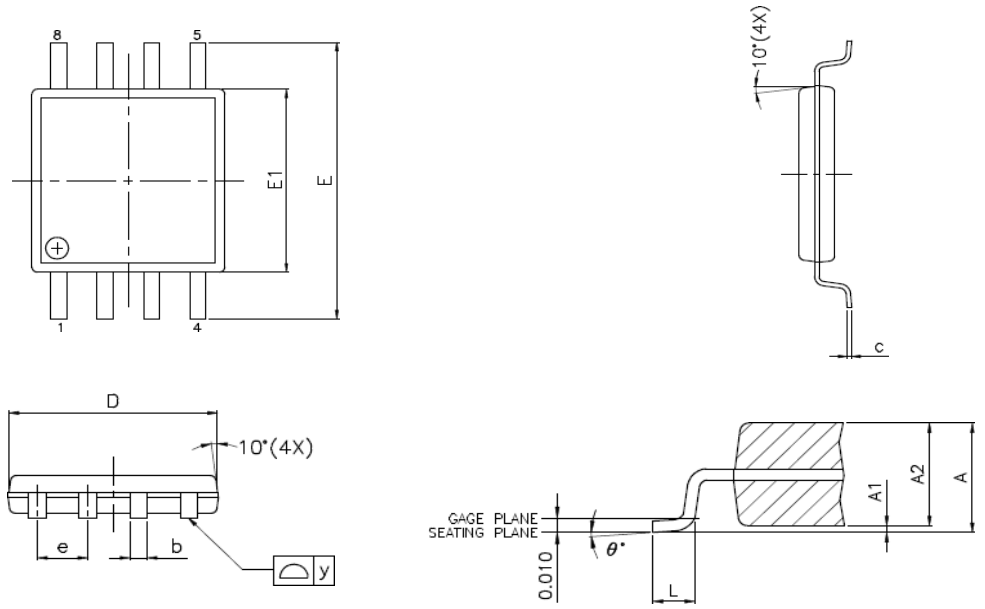


12.11 Hold Timing



13. PACKAGE SPECIFICATION

13.1 8-Pin VSOP 208-mil

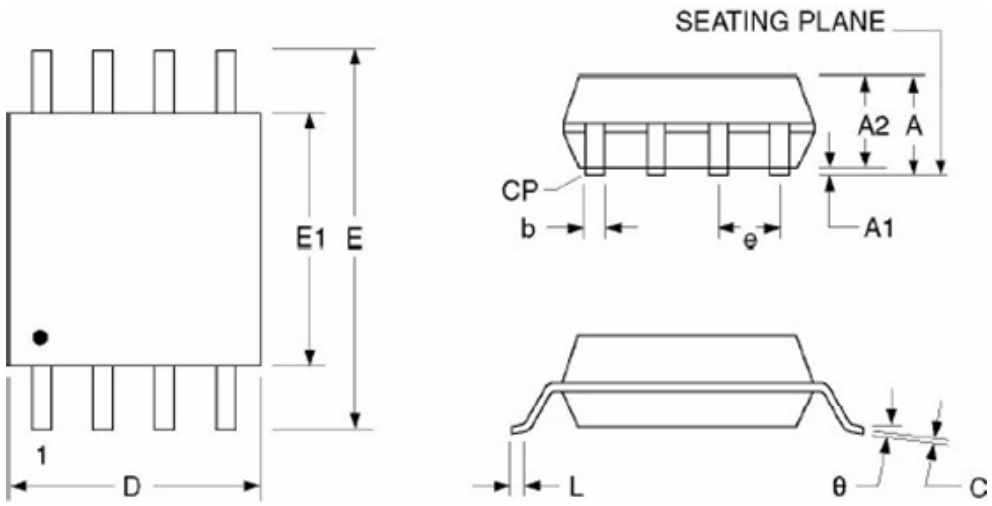


SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	---	---	1.00	---	---	0.039
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.75	0.80	0.85	0.030	0.031	0.033
b	0.35	0.42	0.48	0.014	0.017	0.019
c		0.127 REF.			0.005 REF.	
D	5.18	5.28	5.38	0.204	0.208	0.212
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e	---	1.27	---	---	0.050	---
L	0.50	0.65	0.80	0.020	0.026	0.031
y	---	---	0.10	---	---	0.004
θ	0 °	---	8 °	0 °	---	8 °

Notes:

1. JEDEC outline: N/A.
2. Dimension “D”, “D1” does not include mold flash, mold flash shall not exceed 0.006 [0.15mm] per end. Dimension “E”, “E1” does not include inter lead flash. Inter lead flash shall notexceed 0.010 [0.25mm] per side.
3. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.003 [0.08mm].

13.2 8-Pin SOP 208-mil

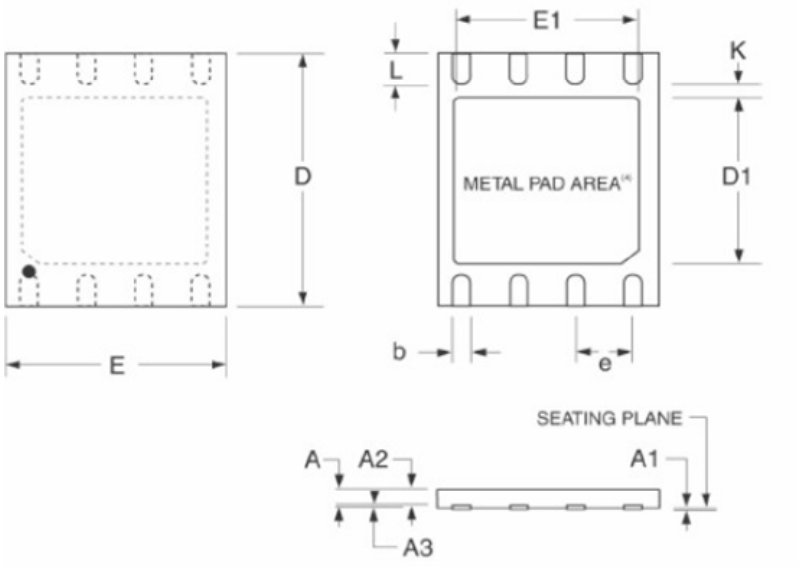


SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.75	2.16	0.069	0.085
A1	0.05	0.25	0.002	0.010
A2	1.70	1.91	0.067	0.075
b	0.35	0.48	0.014	0.019
C	0.19	0.25	0.007	0.010
D	5.18	5.38	0.204	0.212
E	7.70	8.10	0.303	0.319
E1	5.18	5.38	0.204	0.212
e	1.27 BSC		0.050 BSC	
L	0.50	0.80	0.020	0.031
θ	0°	8°	0°	8°
y	---	0.10	---	0.004

Notes:

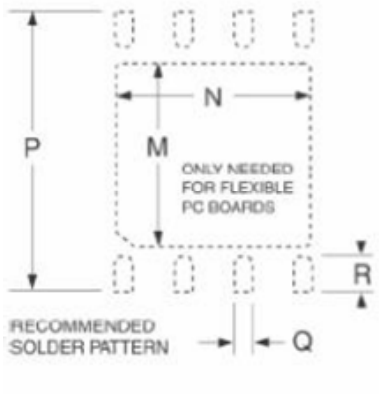
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within. 0004 inches at the seating plane.

13.3 8-contact 6x5 WSON



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	0.02	0.05	0.0000	0.0008	0.0019
A2		0.55			0.0126	
A3	0.19	0.20	0.25	0.0075	0.0080	0.0098
b	0.36	0.40	0.48	0.0138	0.0157	0.0190
D(3	5.90	6.00	6.10	0.2320	0.2360	0.2400
D1	3.30	3.40	3.50	0.1299	0.1338	0.1377
E	4.90	5.00	5.10	0.1930	0.1970	0.2010
E1(3	3.90	4.00	4.05	0.1535	0.1575	0.1594
e(2	1.27 BSC			0.0500 BSC		
K	0.20			0.0080		
L	0.50	0.60	0.75	0.0197	0.0236	0.0295

13.4 8-contact 6x5 WSON (cont'd

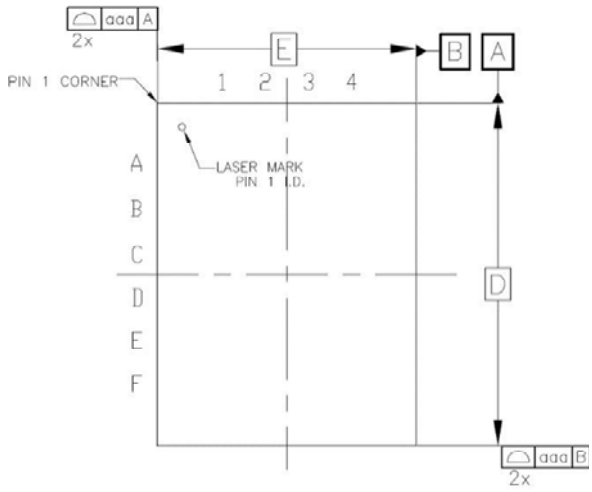


SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
SOLDER PATTERN						
M		3.40			0.1338	
N		4.00			0.1575	
P		6.00			0.2360	
Q		0.50			0.0196	
R		0.65			0.0255	

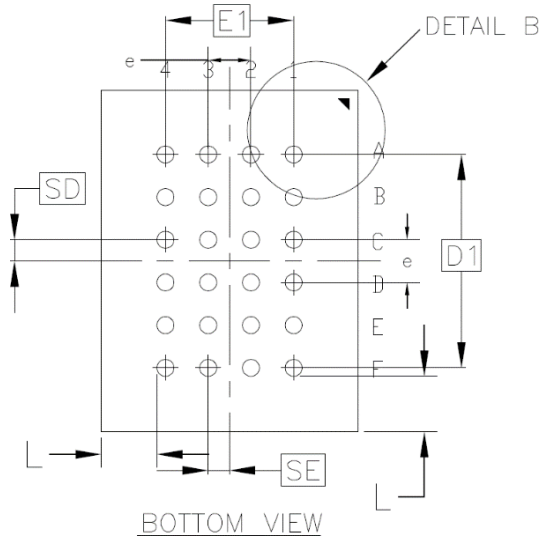
Notes:

1. Advanced Packaging Information; please contact Zetta Co., Ltd. for the latest minimum and maximum specifications.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. The metal pad area on the bottom center of the package is connected to the device ground (GND pin. Avoid placement of exposed PCB bias under the pad.

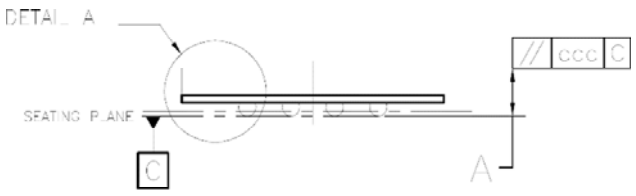
13.5 24-Ball TFBGA



TOP VIEW

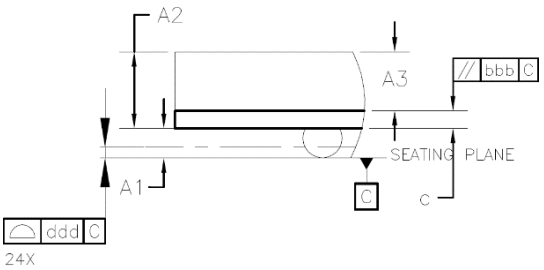


BOTTOM VIEW

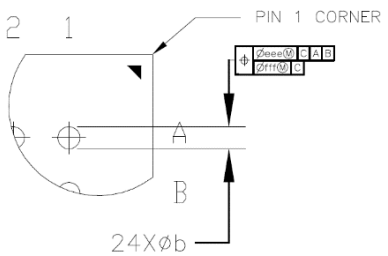


SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.20
A1	0.25	0.30	0.35
A2	0.73	0.78	0.83
A3	0.60 BASIC		
c	0.15	0.18	0.21
D	7.90	8.00	8.10
D1	5.00 BASIC		
E	5.90	6.00	6.10
E1	3.00 BASIC		
e	1.00 BASIC		
b	0.35	0.40	0.45
L	1.30 TYP		
SD	0.50 TYP		
SE	0.50 TYP		
aaa	0.10		
bbb	0.10		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		



DETAIL A(2:1)



DETAIL B(1:1)

14. ORDERING INFORMATION