# Differential Input, 555 kSPS 12-Bit ADC in an 8-Lead SOT-23

Data Sheet

# AD7452

## FEATURES

- **Specified for $V_{DD}$ of 3 V and 5 V**
- **Low power at max throughput rate**
  - **3.3 mW max at 555 kSPS with 3 V supplies**
  - **7.25 mW max at 555 kSPS with 5 V supplies**
- **Fully differential analog input**
- **Wide input bandwidth**
  - **70 dB SINAD at 100 kHz input frequency**
- **Flexible power/serial clock speed management**
- **No pipeline delays**
- **High speed serial interface**
  - **SPI/QSPI™/MICROWIRE™/DSP compatible**
- **Power-down mode: 1 µA max**
- **8-lead SOT-23 package**

## APPLICATIONS

- **Transducer interface**
- **Battery-powered systems**
- **Data acquisition systems**
- **Portable instrumentation**
- **Motor control**

## GENERAL DESCRIPTION

The AD7452[1] is a 12-bit, high speed, low power, successive approximation (SAR) analog-to-digital converter that features a fully differential analog input. This part operates from a single 3 V or 5 V power supply and features throughput rates up to 555 kSPS.

The part contains a low noise, wide bandwidth, differential track-and-hold amplifier (T/H) that can handle input frequencies up to 3.5 MHz. The reference voltage is applied externally to the $V_{REF}$ pin and can be varied from 100 mV to 3.5 V depending on the power supply and what suits the application. The value of the reference voltage determines the common-mode voltage range of the part. With this truly differential input structure and variable reference input, the user can select a variety of input ranges and bias points.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the device to interface with microprocessors or DSPs. The input signals are sampled on the falling edge of $\overline{CS}$, and the conversion is also initiated at this point.

## FUNCTIONAL BLOCK DIAGRAM

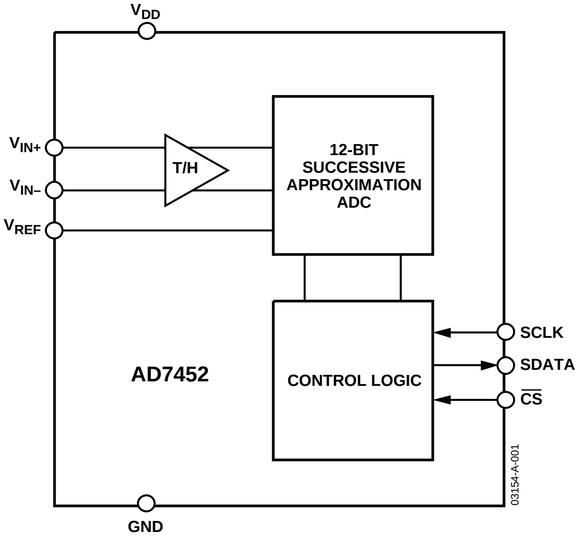


*Figure 1.*

The SAR architecture of this part ensures that there are no pipeline delays.

The AD7452 uses advanced design techniques to achieve very low power dissipation.

## PRODUCT HIGHLIGHTS

1. Operation with Either 3 V or 5 V Power Supplies.
2. High Throughput with Low Power Consumption. With a 3 V supply, the AD7452 offers 3.3 mW max power consumption for 555 kSPS throughput.
3. Fully Differential Analog Input.
4. Flexible Power/Serial Clock Speed Management. The conversion rate is determined by the serial clock, allowing the power to be reduced as the conversion time is reduced through the serial clock speed increase. This part also features a shutdown mode to maximize power efficiency at lower throughput rates.
5. Variable Voltage Reference Input.
6. No Pipeline Delay.
7. Accurate Control of the Sampling Instant via a $\overline{CS}$ Input and Once-Off Conversion Control.
8. ENOB > 8 Bits Typically with 100 mV Reference.

---

[1] Protected by U.S. Patent Number 6,681,332.

**Rev. C** **Document Feedback**

**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700**

**Technical Support** **www.analog.com**

# TABLE OF CONTENTS

## REVISION HISTORY

**7/15—Rev. B to Rev. C**

Changed $F_{SCLK}$ to $f_{SCLK}$ ... Throughout
Changes to Figure 29 ... 16
Changes to Power vs. Throughput Rate Section ... 22
Deleted Microprocessor and DSP Interfacing Section and AD7452 to ADSP-21xx Section ... 22
Deleted Figure 40, Figure 41, and Figure 42; Renumbered Sequentially ... 23
Deleted AD7452 to TMS320C5x/C54x Section and AD7452 to DSP56xxx Section ... 23
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 24

**2/04—Rev. A to Rev. B**

Added Patent Note ... 1

**2/04—Rev. 0 to Rev. A**

Updated Formatting ... Universal
Changes to Applications section ... 1
Changes to General Description ... 1
Changes to Specifications ... 4
Changes to Timing Specifications ... 5
Changes to Timing Example ... 19

**9/03—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 2.7 V to 3.6 V, $f_{SCLK}$ = 10 MHz, $f_S$ = 555 kSPS, $V_{REF}$ = 2.0 V; $V_{DD}$ = 4.75 V to 5.25 V, $f_{SCLK}$ = 10 MHz, $f_S$ = 555 kSPS, $V_{REF}$ = 2.5 V; $V_{CM}$[1] = $V_{REF}$; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions/Comments | B Version[2] | Unit |
|---|---|---|---|
| DYNAMIC PERFORMANCE | $f_{IN}$ = 100 kHz | | |
| Signal-to-(Noise + Distortion) (SINAD)[3] | | 70 | dB min |
| Total Harmonic Distortion (THD)[3] | $V_{DD}$ = 4.75 V to 5.25 V, −86 dB typ | −76 | dB max |
| | $V_{DD}$ = 2.7 V to 3.6 V, −84 dB typ | −74 | dB max |
| Peak Harmonic or Spurious Noise[3] | $V_{DD}$ = 4.75 V to 5.25 V, −86 dB typ | −76 | dB max |
| | $V_{DD}$ = 2.7 V to 3.6 V, −84 dB typ | −74 | dB max |
| Intermodulation Distortion (IMD)[3] | fa = 90 kHz, fb = 110 kHz | | |
| Second-Order Terms | | −89 | dB typ |
| Third-Order Terms | | −89 | dB typ |
| Aperture Delay[3] | | 5 | ns typ |
| Aperture Jitter[3] | | 50 | ps typ |
| Full Power Bandwidth[3, 4] | @ −3 dB | 20 | MHz typ |
| | @ −0.1 dB | 2.5 | MHz typ |
| DC ACCURACY | | | |
| Resolution | | 12 | Bits |
| Integral Nonlinearity (INL) [3] | | ±1 | LSB max |
| Differential Nonlinearity (DNL) [3] | Guaranteed no missed codes to 12 bits | ± 0.95 | LSB max |
| Zero-Code Error[3] | | ±6 | LSB max |
| Positive Gain Error[3] | | ±2 | LSB max |
| Negative Gain Error[3] | | ±2 | LSB max |
| ANALOG INPUT | | | |
| Full-Scale Input Span | 2 × $V_{REF}$[5] | $V_{IN+} - V_{IN-}$ | V |
| Absolute Input Voltage | | | |
| $V_{IN+}$ | $V_{CM} = V_{REF}$ | $V_{CM}$[1] ± $V_{REF}/2$ | V |
| $V_{IN-}$ | $V_{CM} = V_{REF}$ | $V_{CM}$[1] ± $V_{REF}/2$ | V |
| DC Leakage Current | | ±1 | µA max |
| Input Capacitance | When in track/hold | 30/10 | pF typ |
| REFERENCE INPUT | | | |
| $V_{REF}$ Input Voltage | $V_{DD}$ = 4.75 V to 5.25 V (±1% tolerance for specified performance) | 2.5[6] | V |
| | $V_{DD}$ = 2.7 V to 3.6 V (±1% tolerance for specified performance) | 2.0[7] | V |
| DC Leakage Current | | ±1 | µA max |
| $V_{REF}$ Input Capacitance | When in track/hold | 10/30 | pF typ |
| LOGIC INPUTS | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | V min |
| Input Low Voltage, $V_{INL}$ | | 0.8 | V max |
| Input Current, $I_{IN}$ | Typically 10 nA, $V_{IN}$ = 0 V or $V_{DD}$ | ±1 | µA max |
| Input Capacitance, $C_{IN}$ [8] | | 10 | pF max |
| LOGIC OUTPUTS | | | |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ = 4.75 V to 5.25 V, $I_{SOURCE}$ = 200 µA | 2.8 | V min |
| | $V_{DD}$ = 2.7 V to 3.6 V, $I_{SOURCE}$ = 200 µA | 2.4 | V min |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 200 µA | 0.4 | V max |
| Floating-State Leakage Current | | ±1 | µA max |
| Floating-State Output Capacitance[8] | | 10 | pF max |
| Output Coding | | Twos Complement | |

| Parameter | Test Conditions/Comments | B Version[2] | Unit |
|---|---|---|---|
| CONVERSION RATE | | | |
| Conversion Time | 1.6 µs with a 10 MHz SCLK | 16 | SCLK cycles |
| Track-and-Hold Acquisition Time[3] | Sine wave input | 200 | ns max |
| | Step input | 290 | ns max |
| Throughput Rate | | 555 | kSPS max |
| POWER REQUIREMENTS | | | |
| $V_{DD}$ | Range: 3 V + 20%/−10%;<br>5 V ± 5% | 2.7/5.25 | V min/V max |
| $I_{DD}$[9, 10] | | | |
| Normal Mode (Static) | SCLK on or off | 0.5 | mA typ |
| Normal Mode (Operational) | $V_{DD}$ = 4.75 V to 5.25 V | 1.5 | mA max |
| | $V_{DD}$ = 2.7 V to 3.6 V | 1.2 | mA max |
| Full Power-Down Mode | SCLK on or off | 1 | µA max |
| Power Dissipation | | | |
| Normal Mode (Operational) | $V_{DD}$ = 5 V, 1.55 mW typ for 100 kSPS[9] | 7.25 | mW max |
| | $V_{DD}$ = 3 V, 0.64 mW typ for 100 kSPS[9] | 3.3 | mW max |
| Full Power-Down | $V_{DD}$ = 5 V, SCLK on or off | 5 | µW max |
| | $V_{DD}$ = 3 V, SCLK on or off | 3 | µW max |

---

[1] Common-mode voltage. The input signal can be centered on a dc common-mode voltage in the range specified in Figure 23 and Figure 24.

[2] Temperature ranges as follows: B Version: −40°C to +85°C.

[3] See Terminology section.

[4] Analog inputs with slew rates exceeding 27 V/µs (full-scale input sine wave > 3.5 MHz) within the acquisition time may cause an incorrect result to be returned by the converter.

[5] Because the input spans of $V_{IN+}$ and $V_{IN-}$ are both $V_{REF}$ and are 180° out of phase, the differential voltage is $2 \times V_{REF.}$

[6] The AD7452 is functional with a reference input from 100 mV; for $V_{DD}$ = 5 V, the reference can range up to 3.5 V.

[7] The AD7452 is functional with a reference input from 100 mV; for $V_{DD}$ = 3 V, the reference can range up to 2.2 V.

[8] Guaranteed by characterization.

[9] See Power VS. Throughput Rate section.

[10] Measured with a midscale dc input.

## TIMING SPECIFICATIONS

Guaranteed by characterization. All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DD}$) and timed from a 1.6 V voltage level. See Figure 2 and the Serial Interface section.

$V_{DD}$ = 2.7 V to 3.6 V, $f_{SCLK}$ = 10 MHz, $f_S$ = 555 kSPS, $V_{REF}$ = 2.0 V; $V_{DD}$ = 4.75 V to 5.25 V, $f_{SCLK}$ = 10 MHz, $f_S$ = 555 kSPS, $V_{REF}$ = 2.5 V; $V_{CM}$[1] = $V_{REF}$; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Description |
|---|---|---|---|
| $f_{SCLK}$[2] | 10 | kHz min | |
| | 10 | MHz max | |
| $t_{CONVERT}$ | 16 × $t_{SCLK}$ | | $t_{SCLK} = 1/f_{SCLK}$ |
| | 1.6 | µs max | |
| $t_{QUIET}$ | 60 | ns min | Minimum quiet time between the end of a serial read and the next falling edge of $\overline{CS}$ |
| $t_1$ | 10 | ns min | Minimum $\overline{CS}$ pulse width |
| $t_2$ | 10 | ns min | $\overline{CS}$ falling edge to SCLK falling edge setup time |
| $t_3$[3] | 20 | ns max | Delay from $\overline{CS}$ falling edge until SDATA three-state disabled |
| $t_4$[3] | 40 | ns max | Data access time after SCLK falling edge |
| $t_5$ | 0.4 $t_{SCLK}$ | ns min | SCLK high pulse width |
| $t_6$ | 0.4 $t_{SCLK}$ | ns min | SCLK low pulse width |
| $t_7$ | 10 | ns min | SCLK edge to data valid hold time |
| $t_8$[4] | 10 | ns min | SCLK falling edge to SDATA three-state enabled |
| | 35 | ns max | SCLK falling edge to SDATA three-state enabled |
| $t_{POWER-UP}$[5] | 1 | µs max | Power-up time from full power-down |

---

[1] Common-mode voltage.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.8 V or 2.4 V with $V_{DD}$ = 5 V, or 0.4 V or 2.0 V for $V_{DD}$ = 3 V.
[4] $t_8$ is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, $t_8$, quoted in the Timing Specifications is the true bus relinquish time of the part and is independent of the bus loading.
[5] See Power-Up Time section.

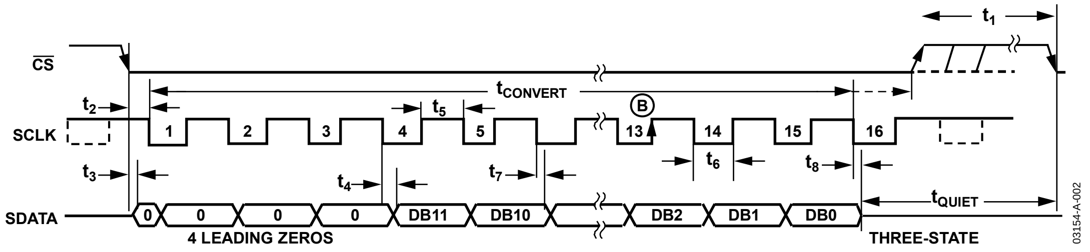


*Figure 2. Serial Interface Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| $V_{IN+}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| $V_{IN-}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to +7 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| $V_{REF}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Input Current to Any Pin Except Supplies[1] | ±10 mA |
| Operating Temperature Range | |
| Commercial (B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| $\theta_{JA}$ Thermal Impedance | 211.5°C/W |
| $\theta_{JC}$ Thermal Impedance | 91.99°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| ESD | 1 kV |

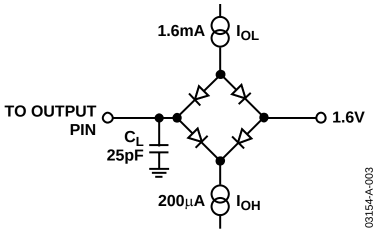


*Figure 3. Load Circuit for Digital Output Timing Specifications*

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

---

[1] Transient currents of up to 100 mA will not cause SCR latch-up.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

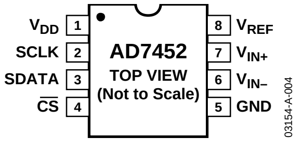


*Figure 4. 8-Lead SOT-23 Pin Configuration*

**Table 4. Pin Function Descriptions**

| Mnemonic | Function |
|---|---|
| $V_{REF}$ | Reference Input for the AD7452. An external reference must be applied to this input. For a 5 V power supply, the reference is 2.5 V (± 1%) for specified performance. For a 3 V power supply, the reference is 2 V (± 1%) for specified performance. This pin should be decoupled to GND with a capacitor of at least 0.1 µF. See the Reference section for more details. |
| $V_{IN+}$ | Positive Terminal for Differential Analog Input. |
| $V_{IN-}$ | Negative Terminal for Differential Analog Input. |
| GND | Analog Ground. Ground reference point for all circuitry on the AD7452. All analog input signals and any external reference signal should be referred to this GND voltage. |
| $\overline{CS}$ | Chip Select. Active low logic input. This input provides the dual function of initiating a conversion on the AD7452 and framing the serial data transfer. |
| SDATA | Serial Data. Logic output. The conversion result from the AD7452 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four leading zeros followed by the 12 bits of conversion data, which are provided MSB first. The output coding is twos complement. |
| SCLK | Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process. |
| $V_{DD}$ | Power Supply Input. $V_{DD}$ is 3 V (+20%/−10%) or 5 V (± 5%). This supply should be decoupled to GND with a 0.1 µF capacitor and a 10 µF tantalum capacitor in parallel. |

# TERMINOLOGY

**Signal-to-(Noise + Distortion) Ratio**

The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to-}(\textit{Noise} + \textit{Distortion}) = (6.02N + 1.76)\ \text{dB}$$

Thus, for a 12-bit converter, this is 74 dB.

**Total Harmonic Distortion (THD)**

Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7452, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where $V_1$ is the rms amplitude of the fundamental and $V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second to the sixth harmonics.

**Peak Harmonic or Spurious Noise**

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

**Intermodulation Distortion**

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at the sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7452 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB.

**Aperture Delay**

The amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

**Aperture Jitter**

The sample-to-sample variation in the effective point in time at which the actual sample is taken.

**Full Power Bandwidth**

The full power bandwidth of an ADC is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

**Common-Mode Rejection Ratio (CMRR)**

This is the ratio of the power in the ADC output at full-scale frequency, $f$, to the power of a 100 mV p-p sine wave applied to the common-mode voltage of $V_{IN+}$ and $V_{IN-}$ of frequency $f_S$

$$CMRR(\text{dB}) = 10\log(Pf/Pf_S)$$

$Pf$ is the power at the frequency $f$ in the ADC output; $Pf_S$ is the power at frequency $f_S$ in the ADC output.

**Integral Nonlinearity (INL)**

The maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

**Differential Nonlinearity (DNL)**

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Zero Code Error**

The deviation of the midscale code transition (111…111 to 000...000) from the ideal $V_{IN+} - V_{IN-}$ (that is, 0 LSB)

**Positive Gain Error**

This is the deviation of the last code transition (011...110 to 011...111) from the ideal $V_{IN+} - V_{IN-}$ (that is, $V_{REF}$ − 1 LSB), after the zero code error has been adjusted out.

### Negative Gain Error

This is the deviation of the first code transition (100...000 to 100...001) from the ideal $V_{IN+} - V_{IN-}$ (that is, $-V_{REF} + 1$ LSB), after the zero code error has been adjusted out.

### Track-and-Hold Acquisition Time

The minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

### Power Supply Rejection Ratio (PSRR)

The ratio of the power in the ADC output at full-scale frequency, $f$, to the power of a 100 mV p-p sine wave applied to the ADC $V_{DD}$ supply of frequency $f_S$. The frequency of this input varies from 1 kHz to 1 MHz.

$$PSRR(\text{dB}) = 10\log(Pf/Pf_S)$$

$Pf$ is the power at frequency $f$ in the ADC output; $Pfs$ is the power at frequency $f_S$ in the ADC output.

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $f_S = 555$ kSPS, $f_{SCLK} = 10$ MHz, unless otherwise noted.

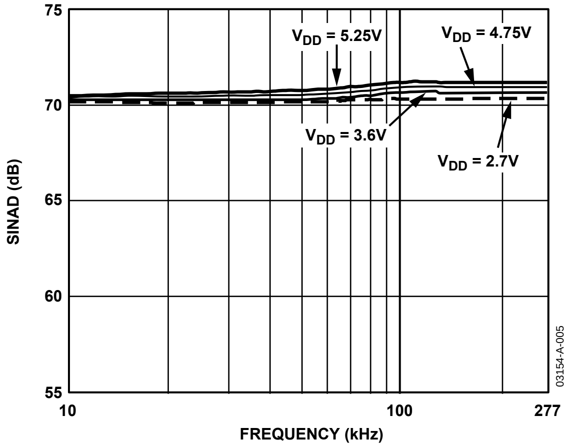


Figure 5. SINAD vs. Analog Input Frequency for Various Supply Voltages

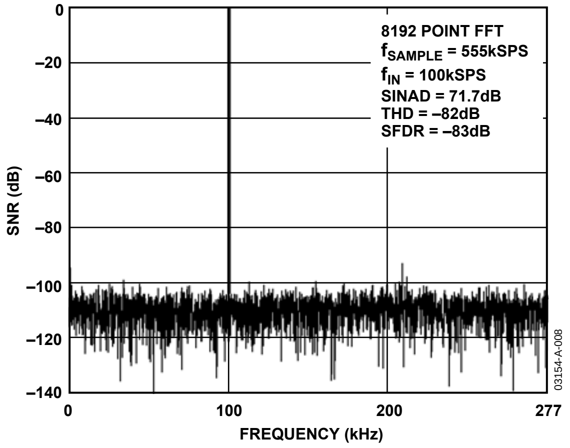


Figure 8. Dynamic Performance with $V_{DD} = 5$ V

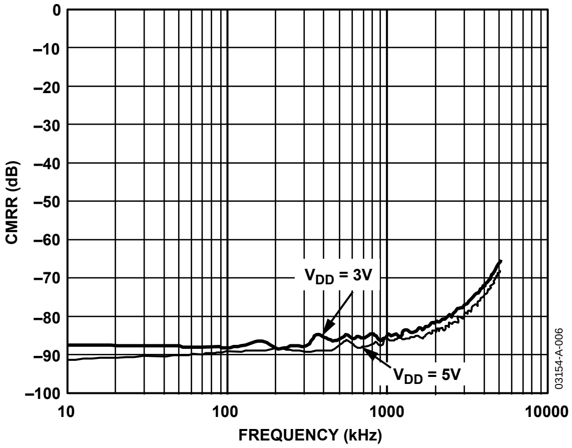


Figure 6. CMRR vs. Frequency for $V_{DD} = 5$ V and 3 V

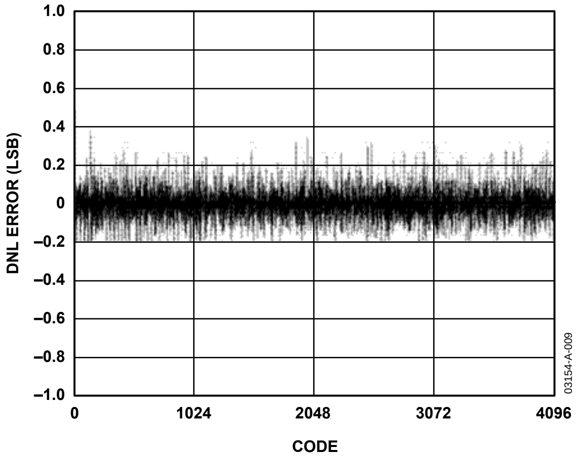


Figure 9. Typical DNL for $V_{DD} = 5$ V

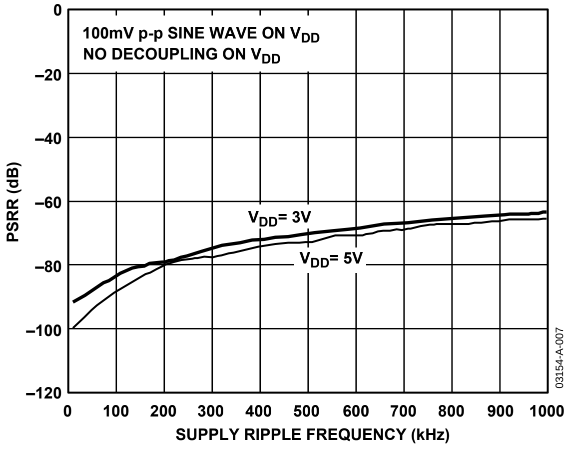


Figure 7. PSRR vs. Supply Ripple Frequency without Supply Decoupling

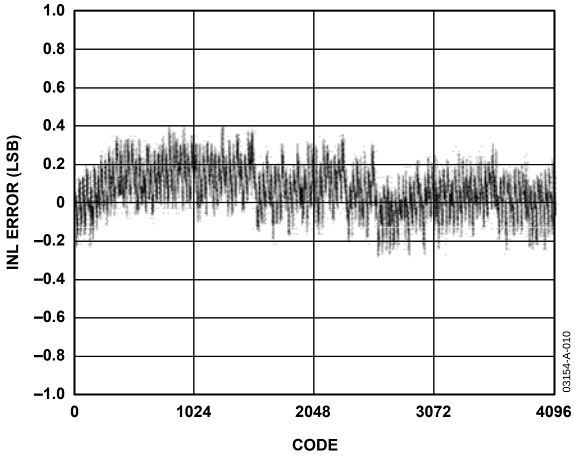


Figure 10. Typical INL for $V_{DD} = 5$ V

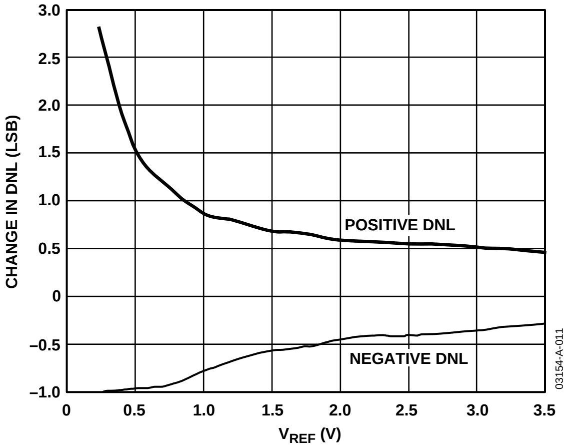


*Figure 11. Change in DNL vs. $V_{REF}$ for $V_{DD}$ = 5 V*

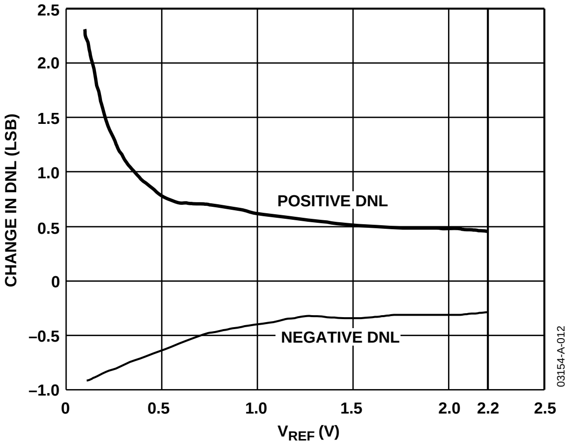


*Figure 12. Change in DNL vs. $V_{REF}$ for $V_{DD}$ = 3 V*

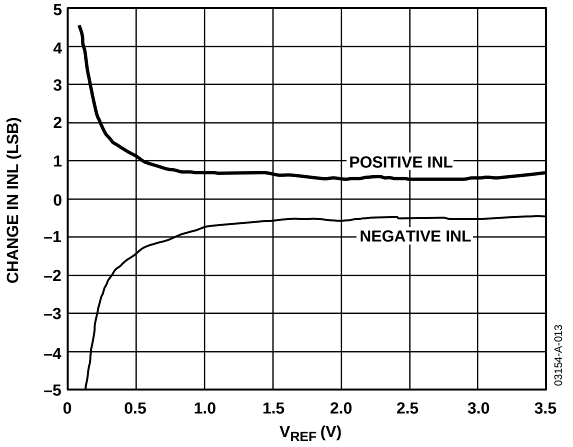


*Figure 13. Change in INL vs. $V_{REF}$ for $V_{DD}$ = 5 V*

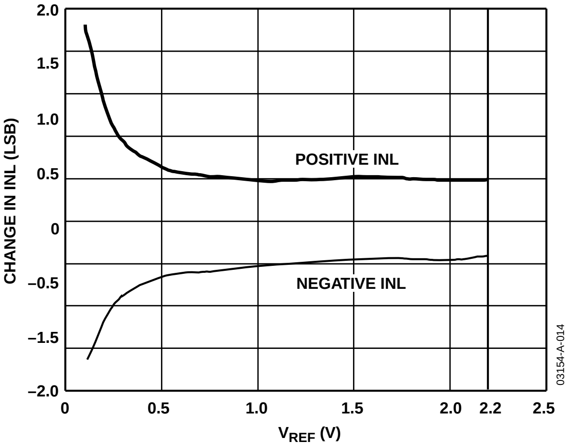


*Figure 14. Change in INL vs. $V_{REF}$ for $V_{DD}$ = 3 V*

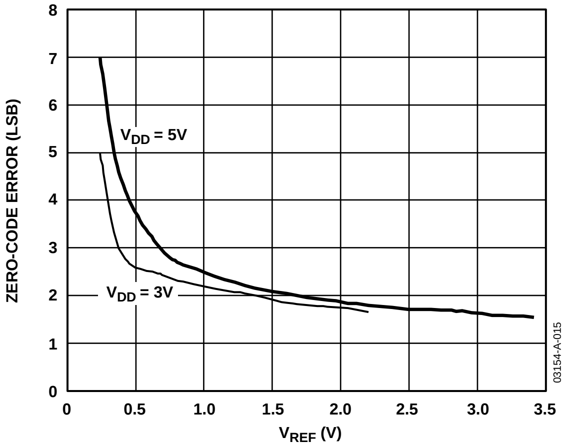


*Figure 15. Change in Zero-Code Error vs. Reference Voltage $V_{DD}$ = 5 V and 3 V*

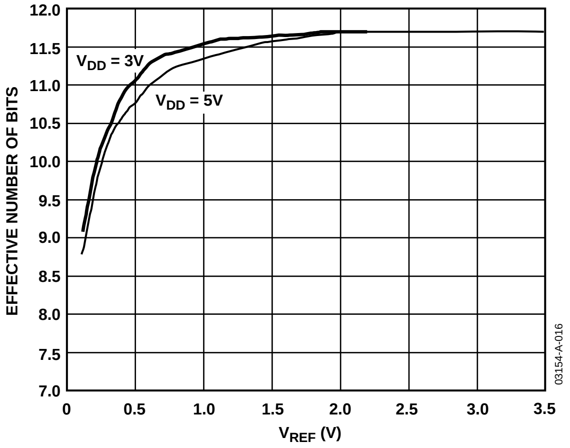


*Figure 16. Change in ENOB vs. Reference Voltage $V_{DD}$ = 5 V and 3 V*

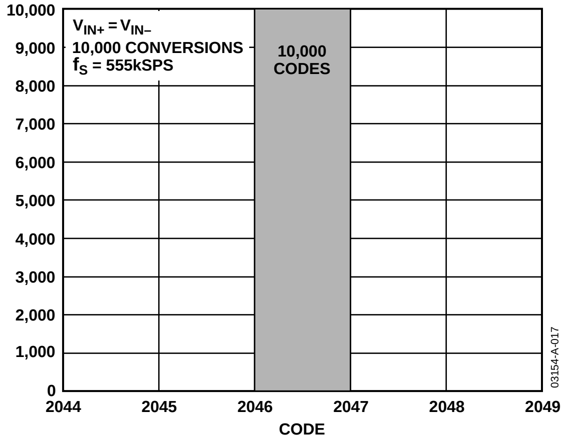


*Figure 17. Histogram of 10,000 Conversions of a DC Input with $V_{DD}$ = 5 V*

# CIRCUIT INFORMATION

The AD7452 is a 12-bit, low power, single-supply, successive approximation analog-to-digital converter (ADC). It can operate with a 5 V or 3 V power supply, and is capable of throughput rates up to 555 kSPS when supplied with a 10 MHz SCLK. It requires an external reference to be applied to the $V_{REF}$ pin, with the value of the reference chosen depending on the power supply and what suits the application.

When operated with a 5 V supply, the maximum reference that can be applied is 3.5 V. When operated with a 3 V supply, the maximum reference that can be applied is 2.2 V (see the Reference section).

The AD7452 has an on-chip differential track-and-hold amplifier, a successive approximation (SAR) ADC, and a serial interface, housed in an 8-lead SOT-23 package. The serial clock input accesses data from the part and provides the clock source for the successive approximation ADC. The AD7452 features a power-down option for reduced power consumption between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

## CONVERTER OPERATION

The AD7452 is a successive approximation ADC based around two capacitive DACs. Figure 18 and Figure 19 show simplified schematics of the ADC in the acquisition and conversion phase, respectively. The ADC is comprised of control logic, an SAR, and two capacitive DACs. In Figure 18 (acquisition phase), SW3 is closed and SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

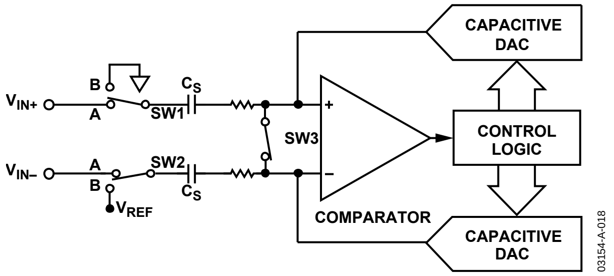


*Figure 18. ADC Acquisition Phase*

When the ADC starts a conversion (Figure 19), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC's output code. The output impedances of the sources driving the $V_{IN+}$ and the $V_{IN-}$ pins must be matched; otherwise, the two inputs will have different settling times, resulting in errors.

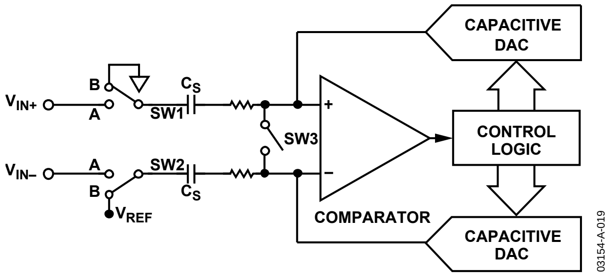


*Figure 19. ADC Conversion Phase*

## ADC TRANSFER FUNCTION

The output coding for the AD7452 is twos complement. The designed code transitions occur at successive LSB values (that is, 1 LSB, 2 LSBs, and so on). The LSB size is 2 × $V_{REF}/4096$. The ideal transfer characteristic of the AD7452 is shown in Figure 20.

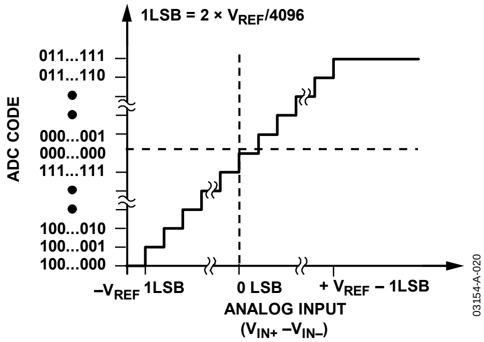


*Figure 20. Ideal Transfer Characteristic*

## TYPICAL CONNECTION DIAGRAM

Figure 21 shows a typical connection diagram for the AD7452 for both 5 V and 3 V supplies. In this setup, the GND pin is connected to the analog ground plane of the system. The $V_{REF}$ pin is connected to either a 2.5 V or a 2 V decoupled reference source, depending on the power supply, to set up the analog input range. The common-mode voltage has to be set up externally and is the value on which the two inputs are centered. The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit result. For more details on driving the differential inputs and setting up the common mode, refer to the Driving Differential Inputs section.

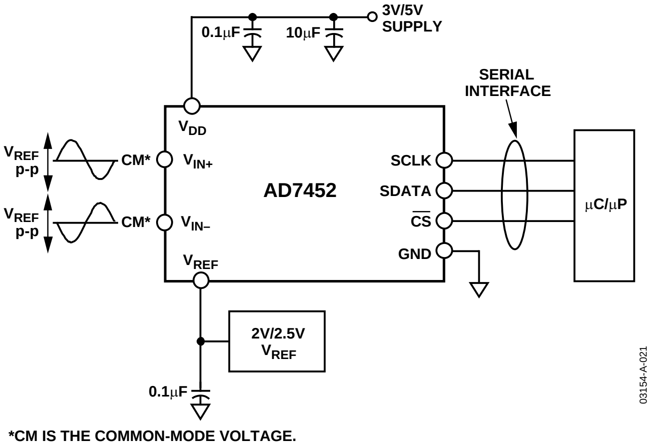


*Figure 21. Typical Connection Diagram*

## ANALOG INPUT

The analog input of the AD7452 is fully differential. Differential signals have a number of benefits over single-ended signals, including noise immunity based on the device's common-mode rejection, improvements in distortion performance, doubling of the device's available dynamic range, and flexibility in input ranges and bias points. Figure 22 defines the fully differential analog input of the AD7452.

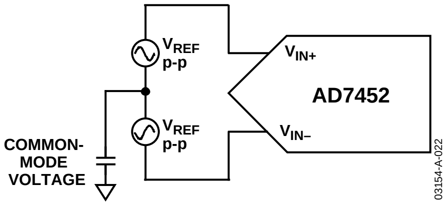


*Figure 22. Differential Input Definition*

The amplitude of the differential signal is the difference between the signals applied to the $V_{IN+}$ and $V_{IN-}$ pins (that is, $V_{IN+} - V_{IN-}$). $V_{IN+}$ and $V_{IN-}$ are simultaneously driven by two signals, each of amplitude $V_{REF}$, that are 180° out of phase. The amplitude of the differential signal is therefore $-V_{REF}$ to $+V_{REF}$ peak-to-peak (that is, $2 \times V_{REF}$). This is true regardless of the common mode (CM).

The common mode is the average of the two signals, that is, $(V_{IN+} + V_{IN-})/2$, and is therefore the voltage upon which the two inputs are centered. This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally, and its range varies with $V_{REF}$. As the value of $V_{REF}$ increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the amplifier's output voltage swing.

Figure 23 and Figure 24 show how the common-mode range typically varies with $V_{REF}$ for both 5 V and 3 V power supplies. The common mode must be in this range to guarantee the functionality of the AD7452.

For ease of use, the common mode can be set up to equal $V_{REF}$, resulting in the differential signal being $\pm V_{REF}$ centered on $V_{REF}$. When a conversion takes place, the common mode is rejected, resulting in a virtually noise-free signal of amplitude, $-V_{REF}$ to $+V_{REF}$, corresponding to the digital codes of 0 to 4096.

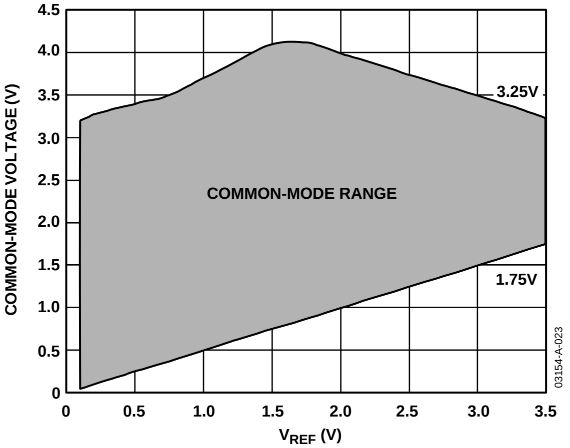


*Figure 23. Input Common-Mode Range vs. $V_{REF}$ ($V_{DD}$ = 5 V and $V_{REF}$ (Max) = 3.5 V)*

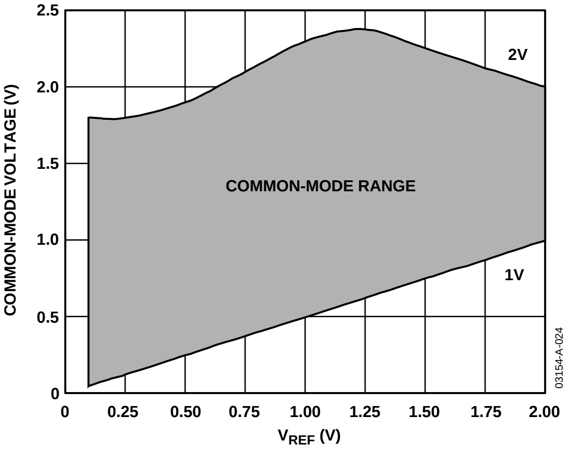


*Figure 24. Input Common-Mode Range vs. $V_{REF}$ ($V_{DD}$ = 3 V and $V_{REF}$ (Max) = 2 V)*

Figure 25 shows examples of the inputs to $V_{IN+}$ and $V_{IN-}$ for different values of $V_{REF}$ for $V_{DD}$ = 5 V. It also gives the maximum and minimum common-mode voltages for each reference value according to Figure 23.

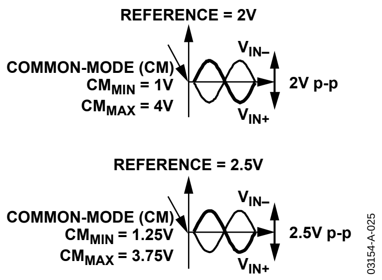


*Figure 25. Examples of the Analog Inputs to $V_{IN+}$ and $V_{IN-}$ for Different Values of $V_{REF}$ for $V_{DD}$ = 5 V*

### *Analog Input Structure*

Figure 26 shows the equivalent circuit of the analog input structure of the AD7452. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part. The capacitors, C1 in Figure 26, are typically 4 pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The capacitors C2 are the ADC's sampling capacitors and have a typical capacitance of 16 pF.

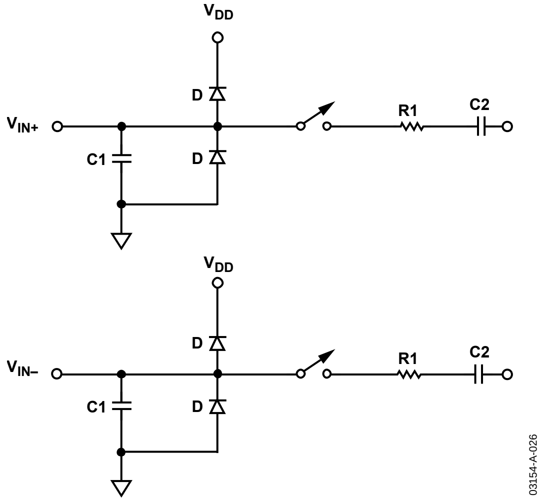


*Figure 26. Equivalent Analog Input Circuit Conversion Phase—Switches Open; Track Phase—Switches Closed*

For ac applications, removing high frequency components from the analog input signal through the use of an RC low-pass filter on the relevant analog input pins is recommended. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases, and performance degrades. Figure 27 shows a graph of the THD versus the analog input signal frequency for different source impedances for $V_{DD}$ = 5 V.

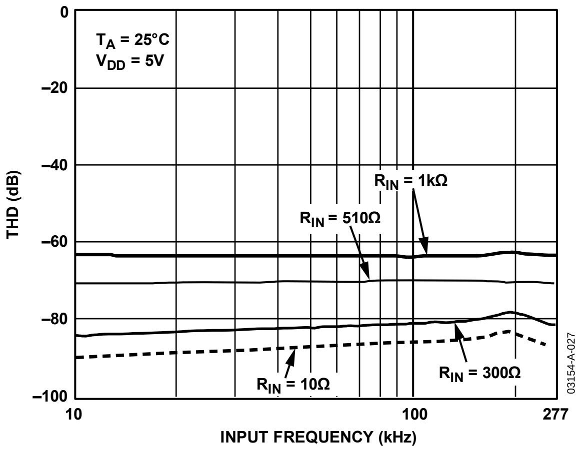


*Figure 27. THD vs. Analog Input Frequency for Various Source Impedances for $V_{DD}$ = 5 V*

Figure 28 shows a graph of the THD vs. the analog input frequency for $V_{DD}$ of 5 V ± 5% and 3 V + 20%/−10%, while sampling at 555 kSPS with an SCLK of 10 MHz. In this case, the source impedance is 10 Ω.

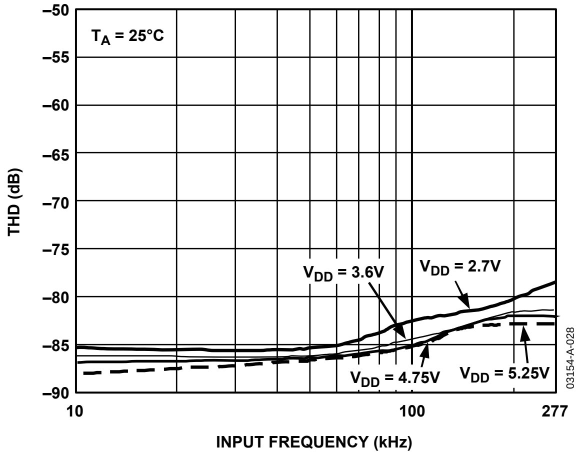


*Figure 28. THD vs. Analog Input Frequency for 3 V and 5 V Supply Voltages*

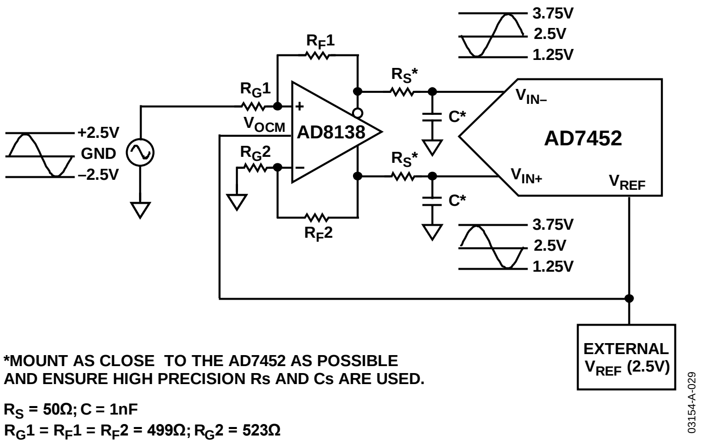
## DRIVING DIFFERENTIAL INPUTS

Differential operation requires that $V_{IN+}$ and $V_{IN-}$ be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally and has a range determined by $V_{REF}$, the power supply, and the particular amplifier used to drive the analog inputs (see Figure 23 and Figure 24). Differential modes of operation with either an ac or a dc input provide the best THD performance over a wide frequency range. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion.

### *Differential Amplifier*

An ideal method of applying differential drive to the AD7452 is to use a differential amplifier such as the AD8138. This part can be used as a single-ended-to-differential amplifier or as a differential-to-differential amplifier. In both cases, the analog input needs to be bipolar. It also provides common-mode level shifting and buffering of the bipolar input signal. Figure 29 shows how the AD8138 can be used as a single-ended-to-differential amplifier. The positive and negative outputs of the AD8138 are connected to the respective inputs on the ADC via a pair of series resistors to minimize the effects of switched capacitance on the front end of the ADCs. The RC low-pass filter on each analog input is recommended in ac applications to remove high frequency components of the analog input. The architecture of the AD8138 results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components. If the analog input source being used has zero impedance, all four resistors ($R_G1$, $R_G2$, $R_F1$, $R_F2$) should be the same. If, for example, the source has a 50 Ω impedance and a 50 Ω termination, the value of $R_G2$ should be increased by 25 Ω to balance this parallel impedance on the input and thus ensure that both the positive and negative analog inputs have the same gain (see Figure 29). The outputs of the amplifier are perfectly matched, balanced differential outputs of identical amplitude, and are exactly 180° out of phase.

The AD8138 is specified with +3 V, +5 V, and ±5 V power supplies, but the best results are obtained when it is supplied by ±5 V. The AD8132 is a lower cost device that could also be used in this configuration with slight differences in characteristics to the AD8138 but with similar performance and operation.



*MOUNT AS CLOSE TO THE AD7452 AS POSSIBLE
AND ENSURE HIGH PRECISION Rs AND Cs ARE USED.

$R_S$ = 50Ω; C = 1nF
$R_G1 = R_F1 = R_F2 = 499Ω$; $R_G2 = 523Ω$

*Figure 29. Using the AD8138 as a Single-Ended-to-Differential Amplifier*

### Op Amp Pair

An op amp pair can be used to directly couple a differential signal to the AD7452. The circuit configurations shown in Figure 30 and Figure 31 show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, it is connected in some way to the reference, but any value in the common-mode range can be input here to set up the common mode. The AD8022 is a suitable dual op amp that could be used in this configuration to provide differential drive to the AD7452.

Care must be taken when choosing the op amp because the selection depends on the required power supply and the system performance objectives. The driver circuits in Figure 30 and Figure 31 are optimized for dc coupling applications that require optimum distortion performance.

The differential op amp driver circuit in Figure 30 is configured to convert and level shift a single-ended, ground-referenced (bipolar) signal to a differential signal centered at the $V_{REF}$ level of the ADC.

The circuit configuration shown in Figure 31 converts a unipolar, single-ended signal into a differential signal.

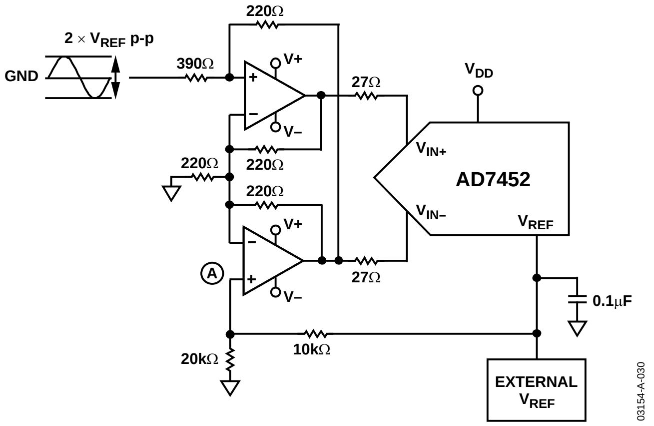


*Figure 30. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Signal*

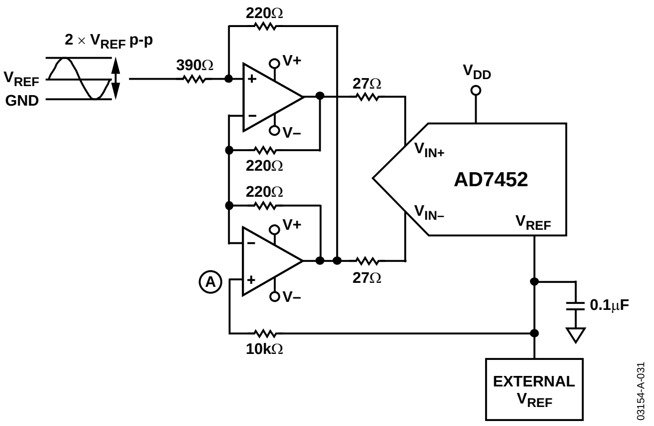


*Figure 31. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal*

### RF Transformer

In systems that do not need to be dc-coupled, an RF transformer with a center tap offers a good solution for generating differential inputs. Figure 32 shows how a transformer is used for single-ended-to-differential conversion. It provides the benefits of operating the ADC in the differential mode without contributing additional noise and distortion. An RF transformer also has the benefit of providing electrical isolation between the signal source and the ADC. A transformer can be used for most ac applications. The center tap is used to shift the differential signal to the common-mode level required; in this case, it is connected to the reference so the common-mode level is the value of the reference.

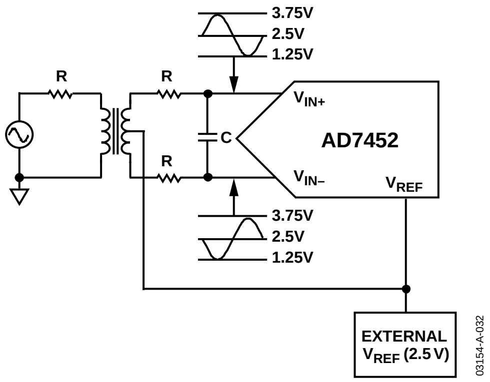


*Figure 32. Using an RF Transformer to Generate Differential Inputs*

## DIGITAL INPUTS

The digital inputs applied to the AD7452 are not limited by the maximum ratings, which limit the analog limits. Instead the digital inputs applied, that is, $\overline{CS}$ and SCLK, can go to 7 V and are not restricted by the $V_{DD}$ + 0.3 V limits as on the analog input.

The main advantage of the inputs being unrestricted to the $V_{DD}$ + 0.3 V limit is that power supply sequencing issues are avoided. If $\overline{CS}$ and SCLK are applied before $V_{DD}$, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to $V_{DD}$.

## REFERENCE

An external reference source is required to supply the reference to the AD7452. This reference input can range from 100 mV to 3.5 V. With a 5 V power supply, the specified reference is 2.5 V and the maximum reference is 3.5 V. With a 3 V power supply, the specified reference is 2 V and the maximum reference is 2.2 V. In both cases, the reference is functional from 100 mV.

It is important to ensure that when choosing the reference value for a particular application, the maximum analog input range ($V_{IN}$ *max*) is never greater than $V_{DD}$ + 0.3 V to comply with the maximum ratings of the device. The following two examples calculate the maximum $V_{REF}$ input that can be used when operating the AD7452 at a $V_{DD}$ of 5 V and 3 V, respectively.

### *Example 1*

$V_{IN}\ max = V_{DD} + 0.3$
$V_{IN}\ max = V_{REF} + V_{REF}/2$

If $V_{DD} = 5$ V, then $V_{IN}\ max = 5.3$ V.

Therefore
$3 \times V_{REF}/2 = 5.3$ V
$V_{REF}\ max = 3.5$ V

Thus, when operating at $V_{DD} = 5$ V, the value of $V_{REF}$ can range from 100 mV to a maximum value of 3.5 V. When $V_{DD} = 4.75$ V, $V_{REF}\ max = 3.17$ V.

### *Example 2*

$V_{IN}\ max = V_{DD} + 0.3$
$V_{IN}\ max = V_{REF} + V_{REF}/2$

If $V_{DD} = 3$ V, then $V_{IN}\ max = 3.3$ V.

Therefore
$3 \times V_{REF}/2 = 3.3$ V
$V_{REF}\ max = 2.2$ V

Thus, when operating at $V_{DD} = 3$ V, the value of $V_{REF}$ can range from 100 mV to a maximum value of 2.2 V. When $V_{DD} = 2.7$ V, $V_{REF}\ max = 2$ V.

These examples show that the maximum reference applied to the AD7452 is directly dependent on the value applied to $V_{DD}$. The value of the reference sets the analog input span and the common-mode voltage range. Errors in the reference source result in gain errors in the AD7452 transfer function and add to specified full-scale errors on the part. A 0.1 µF capacitor should be used to decouple the $V_{REF}$ pin to GND.

Figure 33 shows a typical connection diagram for the $V_{REF}$ pin.

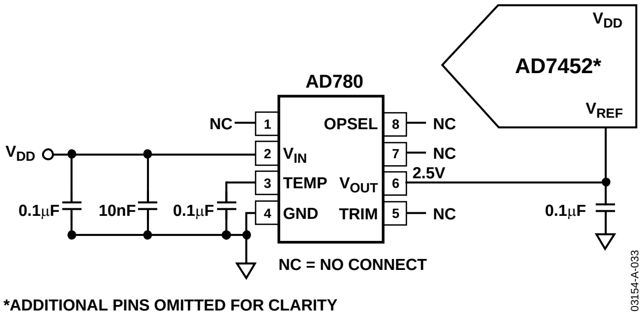


*Figure 33. Typical $V_{REF}$ Connection Diagram for $V_{DD}$ = 5 V*

**Table 5. Examples of Suitable Voltage References**

| Reference | Output Voltage (V) | Initial Accuracy (%) | Operating Current (µA) |
|---|---|---|---|
| AD780 | 2.5/3 | 0.04 | 1000 |
| ADR421 | 2.5 | 0.04 | 500 |
| ADR420 | 2.048 | 0.05 | 500 |

## SINGLE-ENDED OPERATION

When supplied with a 5 V power supply, the AD7452 can handle a single-ended input. The design of this part is optimized for differential operation, so with a single-ended input, performance degrades. Linearity degrades by 0.2 LSB typically, the full-scale errors degrade by 1 LSB typically, and ac performance is not guaranteed.

To operate the AD7452 in single-ended mode, the $V_{IN+}$ input is coupled to the signal source, while the $V_{IN-}$ input is biased to the appropriate voltage corresponding to the midscale code transition. This voltage is the common mode, which is a fixed dc voltage (usually the reference). The $V_{IN+}$ input swings around this value and should have a voltage span of 2 × $V_{REF}$ to make use of the full dynamic range of the part. The input signal therefore has peak-to-peak values of common mode ± $V_{REF}$. If the analog input is unipolar, an op amp in a noninverting unity gain configuration can be used to drive the $V_{IN+}$ pin. Because the ADC operates from a single supply, it is necessary to level shift ground-based bipolar signals to comply with the input requirements. An op amp can be configured to rescale and level shift the ground-based bipolar signal so it is compatible with the selected input range of the AD7452 (see Figure 34).

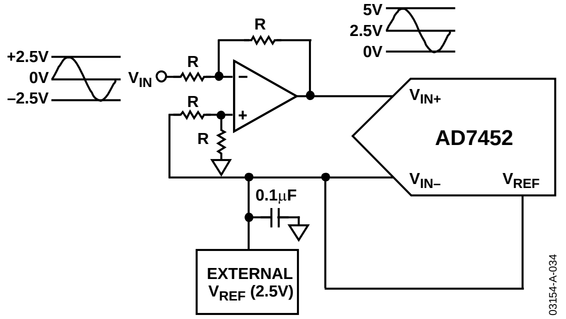


*Figure 34. Applying a Bipolar Single-Ended Input to the AD7452*

## SERIAL INTERFACE

Figure 2 shows a detailed timing diagram for the serial interface of the AD7452. The serial clock provides the conversion clock and also controls the transfer of data from the device during conversion. $\overline{CS}$ initiates the conversion process and frames the data transfer. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state. The analog input is sampled and the conversion is initiated at this point. The conversion requires 16 SCLK cycles to complete.

Once 13 SCLK falling edges have occurred, the track-and-hold goes back into track on the next SCLK rising edge, as shown at Point B in Figure 2. On the 16th SCLK falling edge, the SDATA line goes back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion is terminated and the SDATA line goes back into three-state.

The conversion result from the AD7452 is provided on the SDATA output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7452 consists of four leading zeros followed by 12 bits of conversion data provided MSB first. The output coding is twos complement.

Sixteen serial clock cycles are required to perform a conversion and access data from the AD7452. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out on the subsequent SCLK falling edges beginning with the second leading zero. Thus, the first falling clock edge on the serial clock provides the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge. Once the conversion is complete and the data has been accessed after the 16 clock cycles, it is important to ensure that before the next conversion is initiated, enough time is left to meet the acquisition, and quiet time specifications (see the Timing Example).

In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge, that is, the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the leading zero provided and the 15th SCLK edge would have DB0 provided.

### *Timing Example*

Having $f_{SCLK}$ = 10 MHz and a throughput rate of 555 kSPS gives a cycle time of

$$1/Throughput = 1/555{,}000 = 1.8\ \mu s$$

A cycle consists of

$$t_2 + 12.5(1/f_{SCLK}) + t_{ACQ} = 1.8\ \mu s$$

Therefore, if $t_2$ = 10 ns

$$10\ ns + 12.5(1/10\ MHz) + t_{ACQ} = 1.8\ \mu s$$

$$t_{ACQ} = 540\ ns$$

This 540 ns satisfies the requirement of 290 ns for $t_{ACQ}$.

From Figure 35, $t_{ACQ}$ comprises

$$2.5(1/f_{SCLK}) + t_8 + t_{QUIET}$$

where $t_8$ = 35 ns. This allows a value of 255 ns for $t_{QUIET}$, satisfying the minimum requirement of 60 ns.

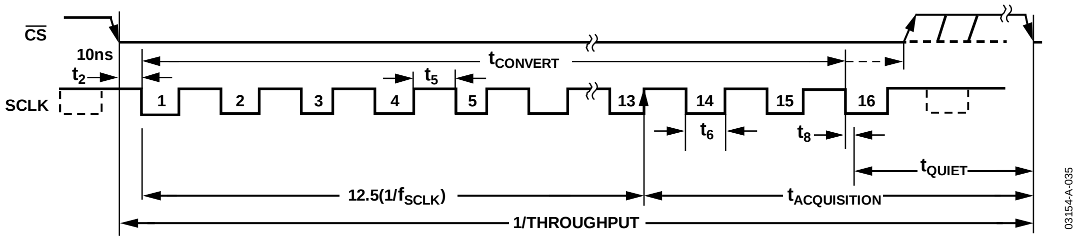


*Figure 35. Serial Interface Timing Example*

# MODES OF OPERATION

The mode of operation of the AD7452 is selected by controlling the logic state of the $\overline{\text{CS}}$ signal during a conversion. There are two possible modes of operation, normal and power-down. The point at which $\overline{\text{CS}}$ is pulled high after the conversion has been initiated determines whether or not the AD7452 enters the power-down mode. Similarly, if already in power-down, $\overline{\text{CS}}$ controls whether the device returns to normal operation or remains in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

## NORMAL MODE

This mode is intended for fastest throughput rate performance. The user does not have to worry about any power-up times with the AD7452 remaining fully powered up all the time. Figure 36 shows the general diagram of the AD7452's operation in this mode. The conversion is initiated on the falling edge of $\overline{\text{CS}}$, as described in the Serial Interface section. To ensure that the part remains fully powered up, $\overline{\text{CS}}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{\text{CS}}$.

If $\overline{\text{CS}}$ is brought high any time after the 10th SCLK falling edge, but before the 16th SCLK falling edge, the part remains powered up but the conversion is terminated and SDATA goes back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{\text{CS}}$ may idle high until the next conversion or may idle low until sometime prior to the next conversion. Once a data transfer is complete, that is, when SDATA has returned to three-state, another conversion can be initiated after the quiet time, $t_{QUIET}$, has elapsed by again bringing $\overline{\text{CS}}$ low.

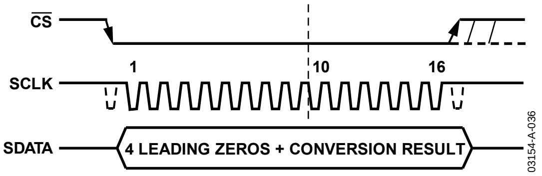


*Figure 36. Normal Mode Operation*

## POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7452 is in power-down mode, all analog circuitry is powered down. To enter power-down mode, the conversion process must be interrupted by bringing $\overline{\text{CS}}$ high anywhere after the second falling edge of SCLK, and before the 10th falling edge of SCLK, as shown in Figure 37.

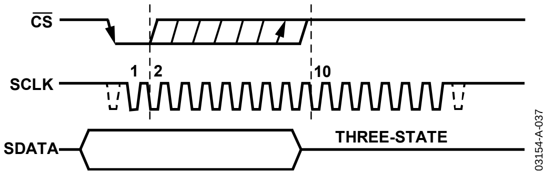


*Figure 37. Entering Power-Down Mode*

Once $\overline{\text{CS}}$ has been brought high in this window of SCLKs, the part enters power-down, the conversion that was initiated by the falling edge of $\overline{\text{CS}}$ is terminated, and SDATA goes back into three-state. The time from the rising edge of $\overline{\text{CS}}$ to SDATA three-state enabled is never greater than $t_8$ (refer to the Timing Specifications). If $\overline{\text{CS}}$ is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the $\overline{\text{CS}}$ line.

In order to exit this mode of operation and power up the AD7452 again, a dummy conversion is performed. On the falling edge of $\overline{\text{CS}}$, the device begins to power up and continues to power up as long as $\overline{\text{CS}}$ is held low until after the falling edge of the 10th SCLK. The device is fully powered up after 1 μs has elapsed and, as shown in Figure 38, valid data results from the next conversion.

If $\overline{\text{CS}}$ is brought high before the 10th falling edge of SCLK, the AD7452 again goes back into power-down. This avoids accidental power-up due to glitches on the $\overline{\text{CS}}$ line or an inadvertent burst of eight SCLK cycles while $\overline{\text{CS}}$ is low. So although the device may begin to power up on the falling edge of $\overline{\text{CS}}$, it again powers down on the rising edge of $\overline{\text{CS}}$ as long as it occurs before the 10th SCLK falling edge.

## POWER-UP TIME

The power-up time of the AD7452 is typically 1 µs, which means that with any SCLK frequency up to 10 MHz, one dummy cycle is always sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC is fully powered up and the input signal will be acquired properly. The quiet time, $t_{QUIET}$, must still be allowed from the point at which the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{\text{CS}}$.

When running at the maximum throughput rate of 555 kSPS, the AD7452 powers up and acquires a signal within ±0.5 LSB in one dummy cycle. When powering up from the power-down mode with a dummy cycle, as in Figure 38, the track-and-hold, which was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{\text{CS}}$. This is shown as Point A in Figure 38.

Although at any SCLK frequency one dummy cycle is sufficient to power up the device and acquire $V_{IN}$, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire $V_{IN}$ fully; 1 µs is sufficient to power up the device and acquire the input signal.

For example, if a 5 MHz SCLK frequency is applied to the ADC, the cycle time is 3.2 µs (that is, 1/(5 MHz) × 16). In one dummy cycle, 3.2 µs, the part is powered up and $V_{IN}$ fully acquired. However, after 1 µs with a 5 MHz SCLK, only five SCLK cycles would have elapsed. At this stage, the ADC is fully powered up and the signal acquired. So in this case, $\overline{\text{CS}}$ can be brought high after the 10th SCLK falling edge and brought low again after a time, $t_{QUIET}$, to initiate the conversion.

When power supplies are first applied to the AD7452, the ADC may power up either in power-down mode or in normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if the user wants the part to power up in power-down mode, the dummy cycle may be used to ensure the device is in power-down by executing a cycle such as the one shown in Figure 37.

Once supplies are applied to the AD7452, the power-up time is the same as that when powering up from power-down mode. It takes approximately 1 µs to power up fully if the part powers up in normal mode. It is not necessary to wait 1 µs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed.

As mentioned earlier, when powering up from the power-down mode, the part returns to track mode upon the first SCLK edge applied after the falling edge of $\overline{\text{CS}}$. However, when the ADC powers up initially after supplies are applied, the track-and-hold is already in track mode. This means if (assuming one has the facility to monitor the ADC supply current) the ADC powers up in the desired mode of operation, and thus a dummy cycle is not required to change the mode, and a dummy cycle is not required to place the track-and-hold into track mode.

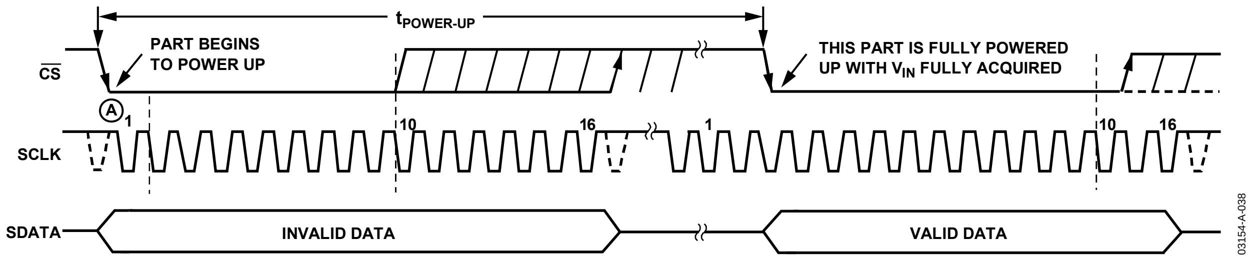


Figure 38. Exiting Power-Down Mode

## POWER vs. THROUGHPUT RATE

By using the power-down mode on the AD7452 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 39 shows how, as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption is reduced accordingly. It shows this for both 5 V and 3 V power supplies.

For example, if the AD7452 is operated in continuous sampling mode with a throughput rate of 100 kSPS and an SCLK of 10 MHz, and the device is placed in power-down mode between conversions, the power consumption is calculated as follows:

*Power Dissipation during Normal Operation* = 7.25 mW *max* (*for* $V_{DD}$ = 5 V)

If the power-up time is one dummy cycle (1.06 µs if $\overline{CS}$ is brought high after the 10th SCLK falling edge and then brought low after the quiet time) and the remaining conversion time is another cycle, that is, 1.6 µs, the AD7452 can be said to dissipate 7.25 mW for 2.66 µs during each conversion cycle. This 2.66 µs figure assumes a very short time to enter power-down mode. This increases as the burst of clocks used to enter the power-down mode is increased.

If the throughput rate = 100 kSPS, the cycle time = 10 µs and the average power dissipated during each cycle is

$(2.66/10) \times 7.25$ mW = 1.92 mW

For the same scenario, if $V_{DD}$ = 3 V, the power dissipation during normal operation is 3.3 mW max.

The AD7452 can now be said to dissipate 3.3 mW for 2.66 µs during each conversion cycle. This 2.66 µs figure assumes a very short time to enter power-down mode. This increases as the burst of clocks used to enter the power-down mode is increased.

The average power dissipated during each cycle with a throughput rate of 100 kSPS is therefore

$(2.66/10) \times 3.3$ mW = 0.88 mW

This is how the power numbers in Figure 39 are calculated.

For throughput rates above 320 kSPS, it is recommended that the serial clock frequency be reduced for optimum power performance.

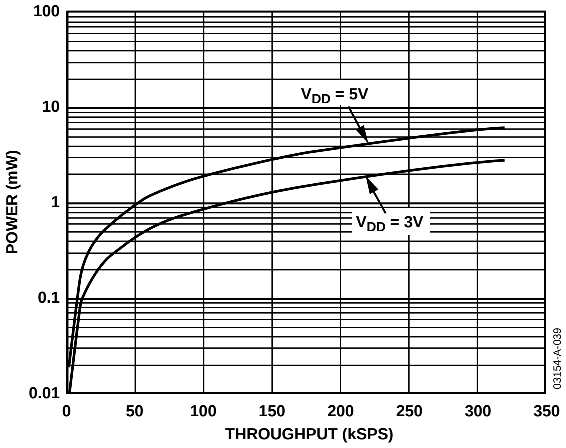


*Figure 39. Power vs. Throughput Rate for Power-Down Mode*

## APPLICATION HINTS

### *Grounding and Layout*

The printed circuit board that houses the AD7452 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place, a star ground point established as close as possible to the GND pin on the AD7452. Avoid running digital lines under the device because this couples noise onto the die. The analog ground plane should be allowed to run under the AD7452 to avoid noise coupling. The power supply lines to the AD7452 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A micro-strip technique is by far the best but is not always possible with a double-sided board.

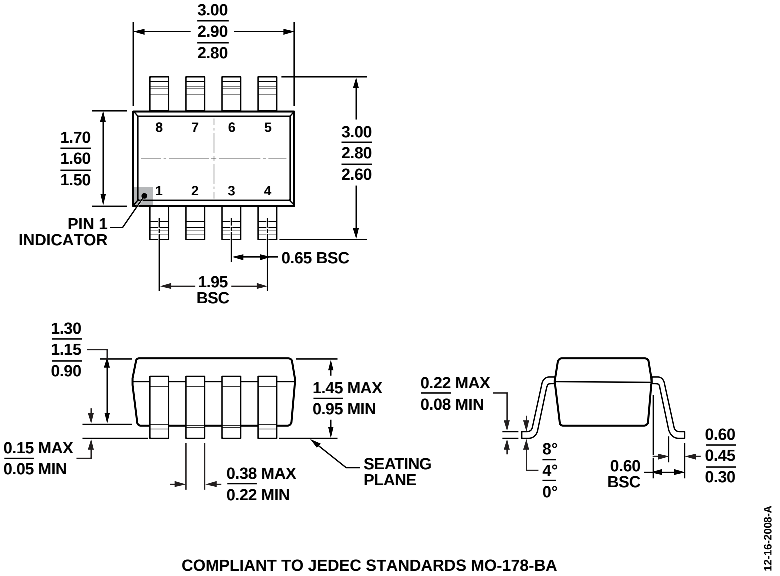
In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side. Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best from these decoupling components, place them as close to the device as possible.

## EVALUATING THE AD7452'S PERFORMANCE

The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the evaluation board controller. The evaluation board controller can be used in conjunction with the AD7452 evaluation board, as well as many other Analog Devices evaluation boards ending with the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7452.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7452. For more information, see the AD7452 application note that accompanies the evaluation kit.

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

*Figure 40. 8-Lead Small Outline Transistor Package [SOT-23]*
*(RJ-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Linearity Error (LSB)[2] | Package Description | Package Option | Branding |
|---|---|---|---|---|---|
| AD7452BRTZ-R2 | −40°C to +85°C | ±1 | 8-Lead SOT-23 | RJ-8 | C4P |
| AD7452BRTZ-REEL7 | −40°C to +85°C | ±1 | 8-Lead SOT-23 | RJ-8 | C4P |

---

[1] Z = RoHS Compliant Part.
[2] Linearity error here refers to integral nonlinearity error.