# 1 A/1.5 A/2 A Synchronous, Step-Down DC-to-DC Converters

Data Sheet

# ADP2105/ADP2106/ADP2107

## FEATURES

- Extremely high 97% efficiency
- Ultralow quiescent current: 20 µA
- 1.2 MHz switching frequency
- 0.1 µA shutdown supply current
- Maximum load current
  - ADP2105: 1 A
  - ADP2106: 1.5 A
  - ADP2107: 2 A
- Input voltage: 2.7 V to 5.5 V
- Output voltage: 0.8 V to $V_{IN}$
- Maximum duty cycle: 100%
- Smoothly transitions into low dropout (LDO) mode
- Internal synchronous rectifier
- Small 16-lead 4 mm × 4 mm LFCSP package
- Optimized for small ceramic output capacitors
- Enable/shutdown logic input
- Undervoltage lockout
- Soft start
- Supported by ADIsimPower™ design tool

## APPLICATIONS

- Mobile handsets
- PDAs and palmtop computers
- Telecommunication/networking equipment
- Set top boxes
- Audio/video consumer electronics

## TYPICAL OPERATING CIRCUIT

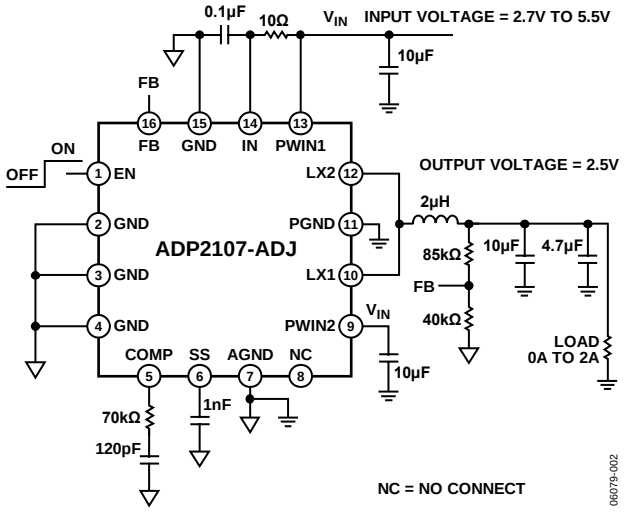


*Figure 1. Circuit Configuration of ADP2107 with $V_{OUT}$ = 2.5 V*

## GENERAL DESCRIPTION

The ADP2105/ADP2106/ADP2107 are low quiescent current, synchronous, step-down dc-to-dc converters in a compact 4 mm × 4 mm LFCSP package. At medium to high load currents, these devices use a current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient response. To ensure the longest battery life in portable applications, the ADP2105/ADP2106/ADP2107 use a pulse frequency modulation (PFM) control scheme under light load conditions that reduces switching frequency to save power.

The ADP2105/ADP2106/ADP2107 run from input voltages of 2.7 V to 5.5 V, allowing single Li+/Li− polymer cell, multiple alkaline/NiMH cells, PCMCIA, and other standard power sources. The output voltage of ADP2105/ADP2106/ADP2107 is adjustable from 0.8 V to the input voltage (indicated by ADJ), whereas the ADP2105/ADP2106/ADP2107 are available in preset output voltage options of 3.3 V, 1.8 V, 1.5 V, and 1.2 V (indicated by x.x V). Each of these variations is available in three maximum current levels: 1 A (ADP2105), 1.5 A (ADP2106), and 2 A (ADP2107). The power switch and synchronous rectifier are integrated for minimal external part count and high efficiency. During logic controlled shutdown, the input is disconnected from the output, and it draws less than 0.1 µA from the input source. Other key features include undervoltage lockout to prevent deep battery discharge and programmable soft start to limit inrush current at startup.

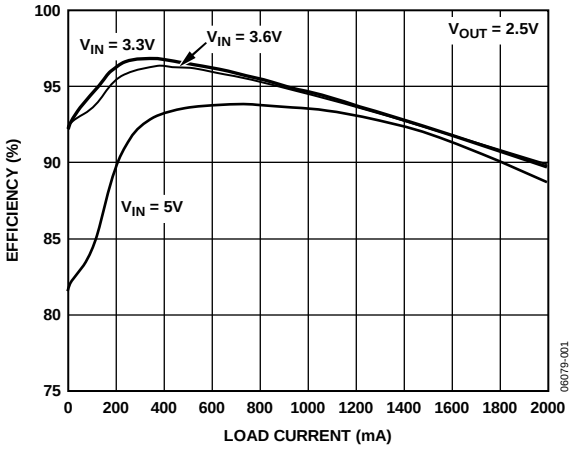


*Figure 2. Efficiency vs. Load Current for the ADP2107 with $V_{OUT}$ = 2.5 V*

Rev. E

Document Feedback



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**8/12—Rev. C to Rev. D**

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**7/06—Revision 0: Initial Version**

# FUNCTIONAL BLOCK DIAGRAM

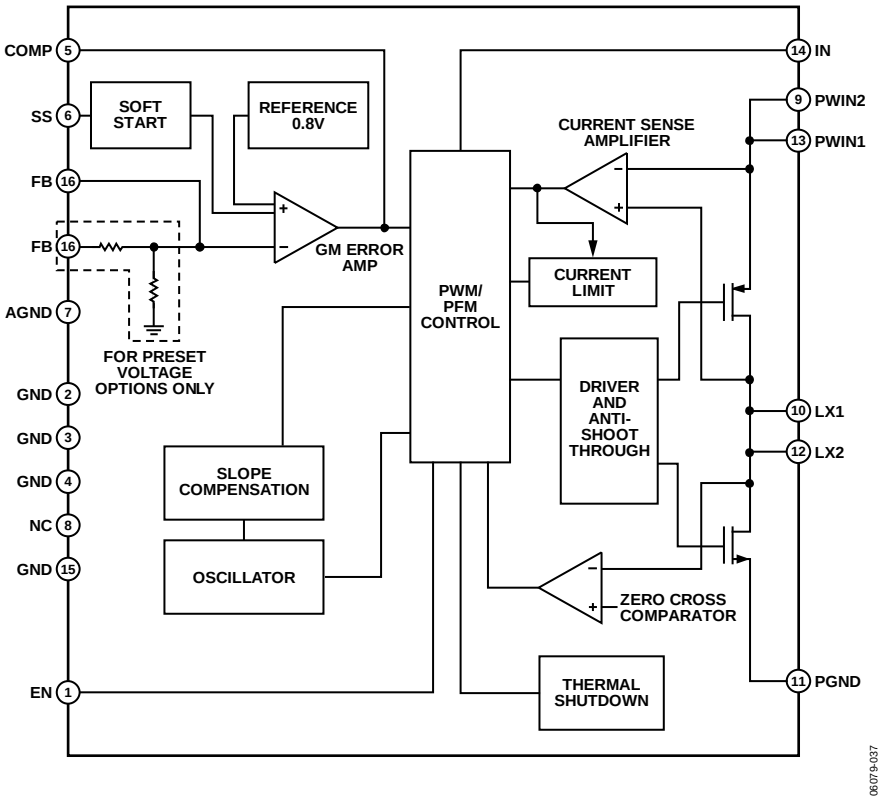



*Figure 3.*

# SPECIFICATIONS

$V_{IN}$ = 3.6 V at $T_A$ = 25°C, unless otherwise noted.[1]

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | |
| Input Voltage Range | 2.7 | | 5.5 | V | −40°C ≤ $T_J$ ≤ +125°C |
| Undervoltage Lockout Threshold | | 2.4 | | V | $V_{IN}$ rising |
| | 2.2 | | 2.6 | V | $V_{IN}$ rising, −40°C ≤ $T_J$ ≤ +125°C |
| | | 2.2 | | V | $V_{IN}$ falling |
| | 2.0 | | 2.5 | V | $V_{IN}$ falling, −40°C ≤ $T_J$ ≤ +125°C |
| Undervoltage Lockout Hysteresis[2] | | 200 | | mV | $V_{IN}$ falling |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Regulation Voltage | 3.267 | 3.3 | 3.333 | V | 3.3 V, load = 10 mA |
| | | 3.3 | | V | 3.3 V, VIN = 3.6 V to 5.5 V, no load to full load |
| | 3.201 | | 3.399 | V | 3.3 V, $V_{IN}$ = 3.6 V to 5.5 V, no load to full load, −40°C ≤ $T_J$ ≤ +125°C |
| | 1.782 | 1.8 | 1.818 | V | 1.8 V, load = 10 mA |
| | | 1.8 | | V | 1.8 V, $V_{IN}$ = 2.7 V to 5.5 V, no load to full load |
| | 1.746 | | 1.854 | V | 1.8 V, $V_{IN}$ = 2.7 V to 5.5 V, no load to full load, −40°C ≤ $T_J$ ≤ +125°C |
| | 1.485 | 1.5 | 1.515 | V | 1.5, load = 10 mA |
| | | 1.5 | | V | ADP210x-1.5 V, VIN = 2.7 V to 5.5 V, no load to full load |
| | 1.455 | | 1.545 | V | ADP210x-1.5 V, $V_{IN}$ = 2.7 V to 5.5 V, no load to full load, −40°C ≤ $T_J$ ≤ +125°C |
| | 1.188 | 1.2 | 1.212 | V | 1.2 V, load = 10 mA |
| | | 1.2 | | V | 1.2 V, $V_{IN}$ = 2.7 V to 5.5 V, no load to full load |
| | 1.164 | | 1.236 | V | 1.2 V, $V_{IN}$ = 2.7 V to 5.5 V, no load to full load, −40°C ≤ $T_J$ ≤ +125°C |
| Load Regulation | | 0.4 | | %/A | ADP2105 |
| | | 0.5 | | %/A | ADP2106 |
| | | 0.6 | | %/A | ADP2107 |
| Line Regulation[3] | | 0.1 | 0.33 | %/V | ADP2105, measured in servo loop |
| | | 0.1 | 0.3 | %/V | ADP2106 and ADP2107, measured in servo loop |
| Output Voltage Range | 0.8 | | $V_{IN}$ | V | ADJ |
| FEEDBACK CHARACTERISTICS | | | | | |
| FB Regulation Voltage | | 0.8 | | V | ADJ |
| | 0.784 | | 0.816 | V | ADJ, −40°C ≤ $T_J$ ≤ +125°C |
| FB Bias Current | −0.1 | | +0.1 | µA | ADJ, −40°C ≤ $T_J$ ≤ +125°C |
| | | 3 | | µA | 1.2 V output voltage |
| | | | 6 | µA | 1.2 V output voltage, −40°C ≤ $T_J$ ≤ +125°C |
| | | 4 | | µA | 1.5 V output voltage |
| | | | 8 | µA | 1.5 V output voltage, −40°C ≤ $T_J$ ≤ +125°C |
| | | 5 | | µA | 1.8 V output voltage |
| | | | 10 | µA | 1.8 V output voltage, −40°C ≤ $T_J$ ≤ +125°C |
| | | 10 | | µA | 3.3 V output voltage |
| | | | 20 | µA | 3.3 V output voltage, −40°C ≤ $T_J$ ≤ +125°C |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| INPUT CURRENT CHARACTERISTICS | | | | | |
| IN Operating Current | | 20 | | µA | ADP2105/ADP2106/ADP2107 (ADJ), $V_{FB}$ = 0.9 V |
| | | | 30 | µA | ADP2105/ADP2106/ADP2107 (ADJ), $V_{FB}$ = 0.9 V, −40°C ≤ $T_J$ ≤ +125°C |
| | | 20 | | µA | ADP2105/ADP2106/ADP2107 (x.x V) output voltage 10% above regulation voltage |
| | | | 30 | µA | ADP2105/ADP2106/ADP2107 (x.x V) output voltage 10% above regulation voltage, −40°C ≤ $T_J$ ≤ +125°C |
| IN Shutdown Current[4] | | 0.1 | 1 | µA | $V_{EN}$ = 0 V |
| LX (SWITCH) NODE CHARACTERISTICS | | | | | |
| LX On Resistance[4] | | 190 | | mΩ | P-channel switch, ADP2105 |
| | | | 270 | mΩ | P-channel switch, ADP2105, −40°C ≤ $T_J$ ≤ +125°C |
| | | 100 | | mΩ | P-channel switch, ADP2106 and ADP2107 |
| | | | 165 | mΩ | P-channel switch, ADP2106 and ADP2107, −40°C ≤ $T_J$ ≤ +125°C |
| | | 160 | | mΩ | N-channel synchronous rectifier, ADP2105 |
| | | | 230 | mΩ | N-channel synchronous rectifier, ADP2105, −40°C ≤ $T_J$ ≤ +125°C |
| | | 90 | | mΩ | N-channel synchronous rectifier, ADP2106 and ADP2107 |
| | | | 140 | mΩ | N-channel synchronous rectifier, ADP2106 and ADP2107, −40°C ≤ $T_J$ ≤ +125°C |
| LX Leakage Current[4, 5] | | 0.1 | 1 | µA | $V_{IN}$ = 5.5 V, $V_{LX}$ = 0 V, 5.5 V |
| LX Peak Current Limit[5] | | 2.9 | | A | P-channel switch, ADP2107 |
| | 2.6 | | 3.3 | A | P-channel switch, ADP2107, −40°C ≤ $T_J$ ≤ +125°C |
| | | 2.25 | | A | P-channel switch, ADP2106 |
| | 2.0 | | 2.6 | A | P-channel switch, ADP2106, −40°C ≤ $T_J$ ≤ +125°C |
| | | 1.5 | | A | P-channel switch, ADP2105 |
| | 1.3 | | 1.8 | A | P-channel switch, ADP2105, −40°C ≤ $T_J$ ≤ +125°C |
| LX Minimum On-Time | | | 110 | ns | In PWM mode of operation, −40°C ≤ $T_J$ ≤ +125°C |
| ENABLE CHARACTERISTICS | | | | | |
| EN Input High Voltage | 2 | | | V | $V_{IN}$ = 2.7 V to 5.5 V, −40°C ≤ $T_J$ ≤ +125°C |
| EN Input Low Voltage | | | 0.4 | V | $V_{IN}$ = 2.7 V to 5.5 V, −40°C ≤ $T_J$ ≤ +125°C |
| EN Input Leakage Current | | −0.1 | | µA | $V_{IN}$ = 5.5 V, $V_{EN}$ = 0 V, 5.5 V |
| | −1 | | +1 | µA | $V_{IN}$ = 5.5 V, $V_{EN}$ = 0 V, 5.5 V, −40°C ≤ $T_J$ ≤ +125°C |
| OSCILLATOR FREQUENCY | | 1.2 | | MHz | $V_{IN}$ = 2.7 V to 5.5 V |
| | 1 | | 1.4 | MHz | $V_{IN}$ = 2.7 V to 5.5 V, −40°C ≤ $T_J$ ≤ +125°C |
| SOFT START PERIOD | 750 | 1000 | 1200 | µs | $C_{SS}$ = 1 nF |
| THERMAL CHARACTERISTICS | | | | | |
| Thermal Shutdown Threshold | | 140 | | °C | |
| Thermal Shutdown Hysteresis | | 40 | | °C | |
| COMPENSATOR TRANSCONDUCTANCE ($g_m$) | | 50 | | µA/V | |
| CURRENT SENSE AMPLIFIER GAIN ($G_{CS}$)[2] | | 1.875 | | A/V | ADP2105 |
| | | 2.8125 | | A/V | ADP2106 |
| | | 3.625 | | A/V | ADP2107 |

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). Typical values are at $T_A$ = 25°C.
[2] Guaranteed by design.
[3] The ADP2105/ADP2106/ADP2107 line regulation was measured in a servo loop on the automated test equipment that adjusts the feedback voltage to achieve a specific COMP voltage.
[4] All LX (switch) node characteristics are guaranteed only when the LX1 pin and LX2 pin are tied together.
[5] These specifications are guaranteed from −40°C to +85°C.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| IN, EN, SS, COMP, FB to AGND | −0.3 V to +6 V |
| LX1, LX2 to PGND | −0.3 V to ($V_{IN}$ + 0.3 V) |
| PWIN1, PWIN2 to PGND | −0.3 V to +6 V |
| PGND to AGND | −0.3 V to +0.3 V |
| GND to AGND | −0.3 V to +0.3 V |
| PWIN1, PWIN2 to IN | −0.3 V to +0.3 V |
| Operating Junction Temperature Range | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Soldering Conditions | JEDEC J-STD-020 |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 16-Lead LFCSP | 40 | °C/W |
| Maximum Power Dissipation | 1 | W |

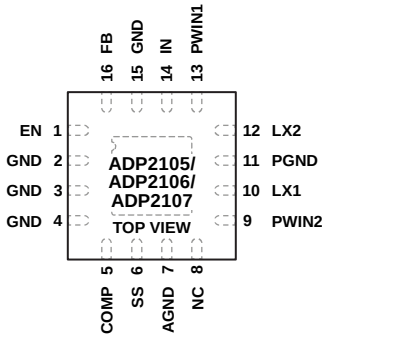
## BOUNDARY CONDITION

Natural convection, 4-layer board, exposed pad soldered to the PCB.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS




NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD SHOULD BE SOLDERED TO AN EXTERNAL GROUND PLANE UNDERNEATH THE IC FOR THERMAL DISSIPATION.

06079-003

*Figure 4. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | EN | Enable Input. Drive EN high to turn on the device. Drive EN low to turn off the device and reduce the input current to 0.1 µA. |
| 2, 3, 4, 15 | GND | Test Pins. These pins are used for internal testing and are not ground return pins. These pins are to be tied to the AGND plane as close as possible to the ADP2105/ADP2106/ADP2107. |
| 5 | COMP | Feedback Loop Compensation Node. COMP is the output of the internal transconductance error amplifier. Place a series RC network from COMP to AGND to compensate the converter. See the Loop Compensation section. |
| 6 | SS | Soft Start Input. Place a capacitor from SS to AGND to set the soft start period. A 1 nF capacitor sets a 1 ms soft start period. |
| 7 | AGND | Analog Ground. Connect the ground of the compensation components, the soft start capacitor, and the voltage divider on the FB pin to the AGND pin as close as possible to the ADP2105/ ADP2106/ADP2107. The AGND is also to be connected to the exposed pad of ADP2105/ADP2106/ADP2107. |
| 8 | NC | No Connect. This is not internally connected and can be connected to other pins or left unconnected. |
| 9, 13 | PWIN2, PWIN1 | Power Source Inputs. The source of the PFET high-side switch. Bypass each PWIN pin to the nearest PGND plane with a 4.7 µF or greater capacitor as close as possible to the ADP2105/ADP2106/ ADP2107. See the Input Capacitor Selection section. |
| 10, 12 | LX1, LX2 | Switch Outputs. The drain of the P-channel power switch and N-channel synchronous rectifier. These pins are to be tied together and connected to the output LC filter between LX and the output voltage. |
| 11 | PGND | Power Ground. Connect the ground return of all input and output capacitors to the PGND pin using a power ground plane as close as possible to the ADP2105/ADP2106/ADP2107. The PGND is then to be connected to the exposed pad of the ADP2105/ADP2106/ADP2107. |
| 14 | IN | Power Input. The power source for the ADP2105/ADP2106/ADP2107 internal circuitry. Connect IN and PWIN1 with a 10 Ω resistor as close as possible to the ADP2105/ADP2106/ADP2107. Bypass IN to AGND with a 0.1 µF or greater capacitor. See the Input Filter section. |
| 16 | FB | Output Voltage Sense or Feedback Input. For fixed output versions, connect to the output voltage. For adjustable versions, FB is the input to the error amplifier. Drive FB through a resistive voltage divider to set the output voltage. The FB regulation voltage is 0.8 V. |
| | EP | Exposed Pad. The exposed pad should be soldered to an external ground plane underneath the IC for thermal dissipation. |

# TYPICAL PERFORMANCE CHARACTERISTICS

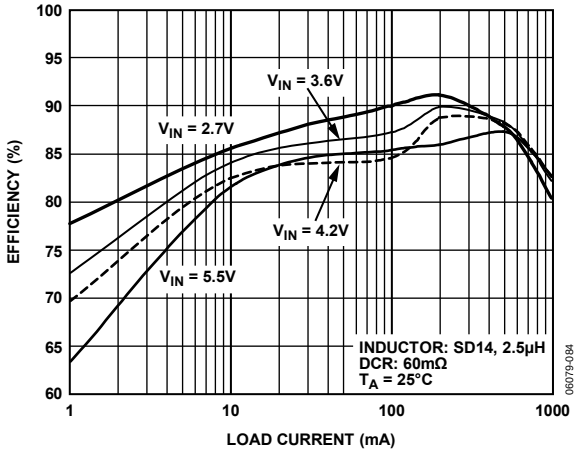



Figure 5. Efficiency—ADP2105 (1.2 V Output)

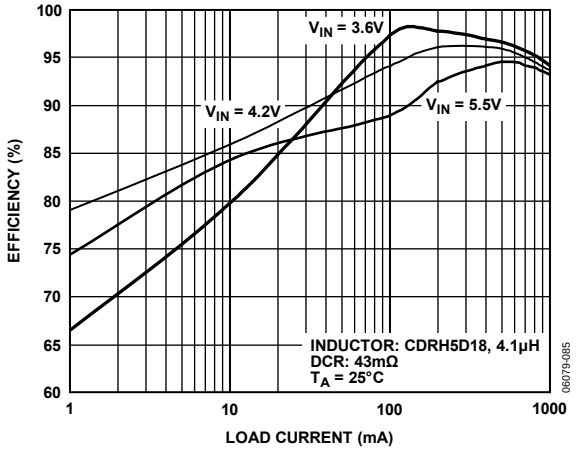



Figure 6. Efficiency—ADP2105 (3.3 V Output)

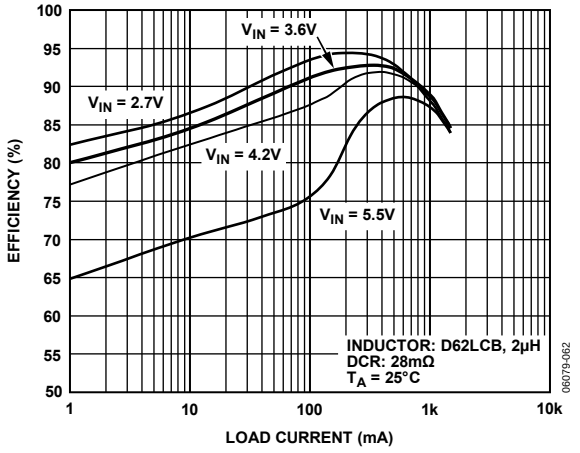



Figure 7. Efficiency—ADP2106 (1.8 V Output)

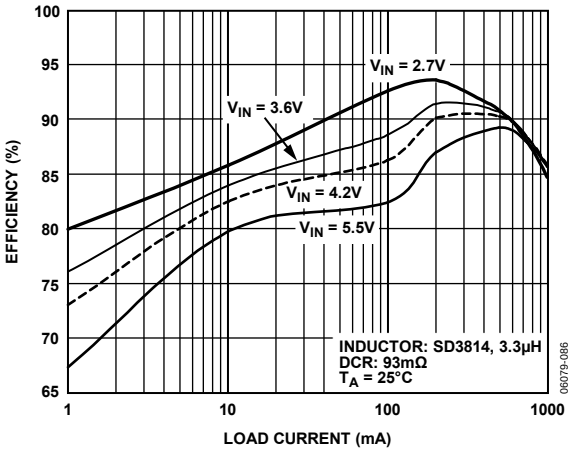



Figure 8. Efficiency—ADP2105 (1.8 V Output)

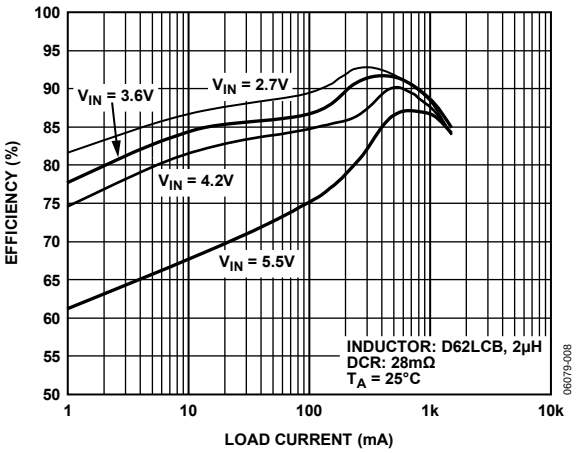



Figure 9. Efficiency—ADP2106 (1.2 V Output)

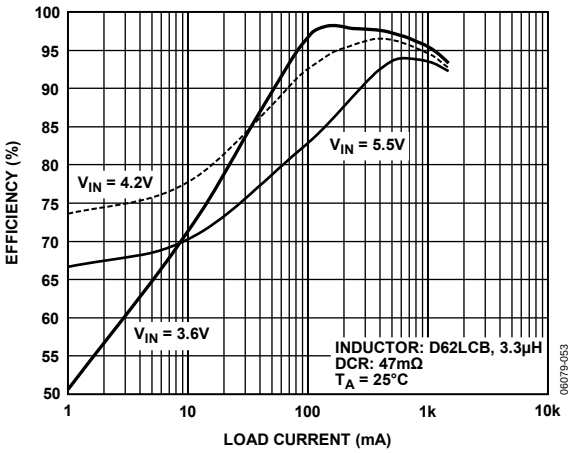



Figure 10. Efficiency—ADP2106 (3.3 V Output)

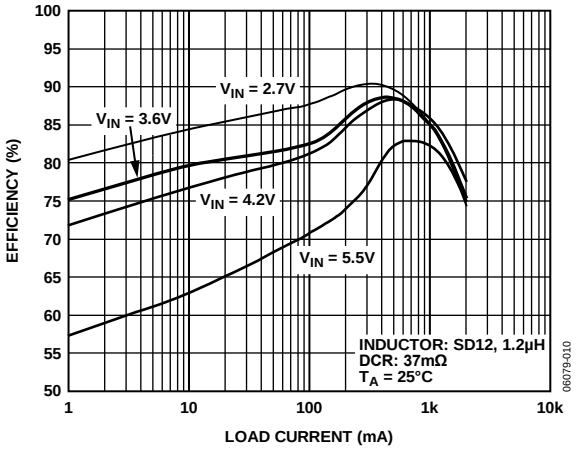



Figure 11. Efficiency—ADP2107 (1.2 V)

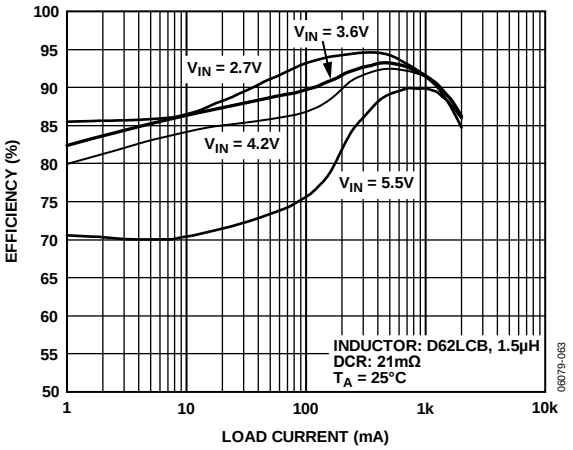



Figure 14. Efficiency—ADP2107 (1.8 V)

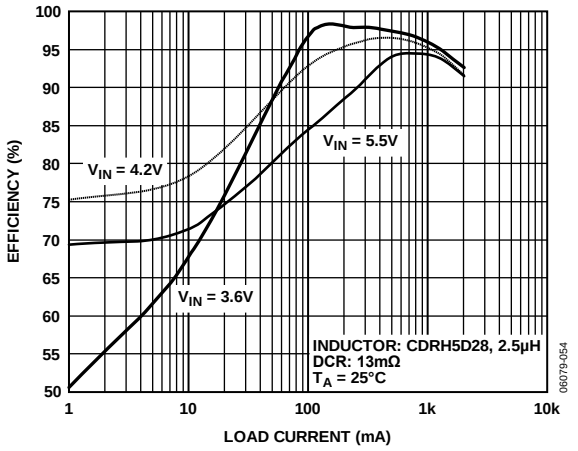



Figure 12. Efficiency—ADP2107 (3.3 V)

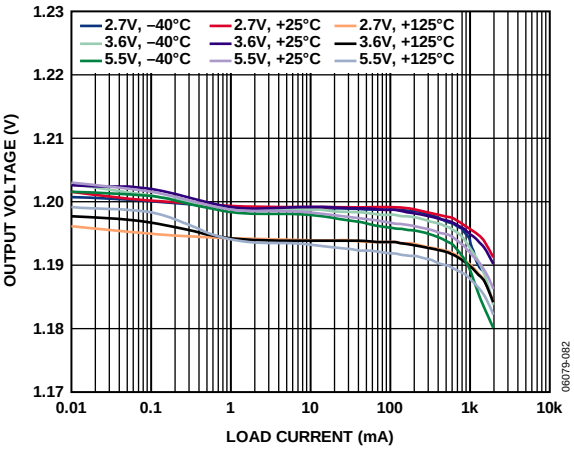



Figure 15. Output Voltage Accuracy—ADP2107 (1.2 V)

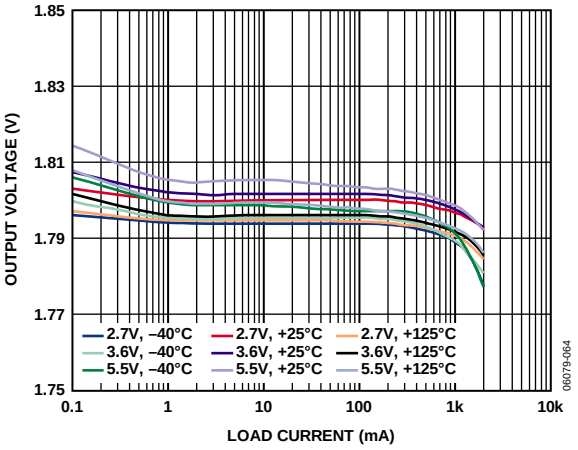



Figure 13. Output Voltage Accuracy—ADP2107 (1.8 V)

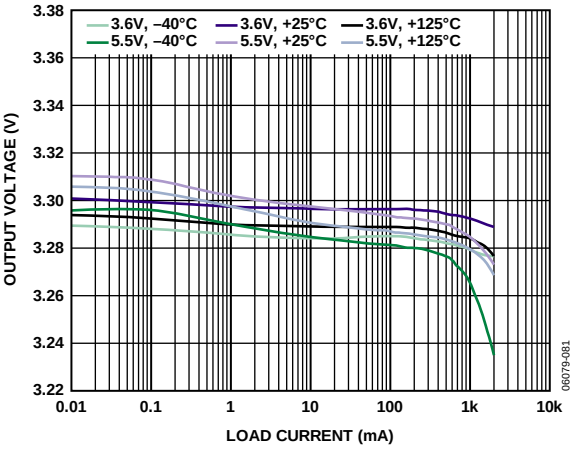



Figure 16. Output Voltage Accuracy—ADP2107 (3.3 V)

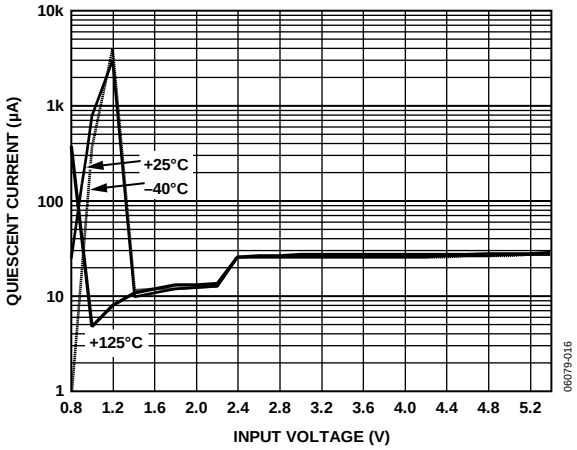



Figure 17. Quiescent Current vs. Input Voltage

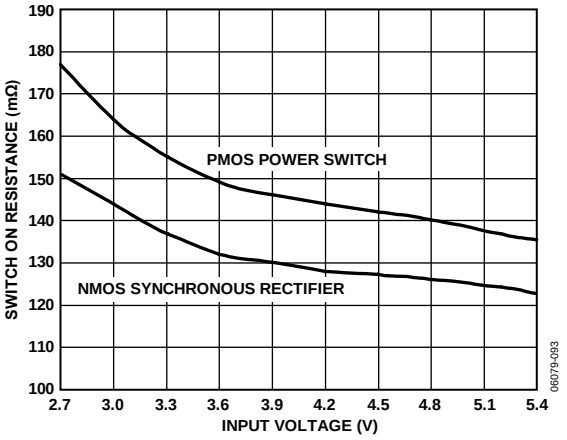



Figure 20. Switch On Resistance vs. Input Voltage—ADP2105

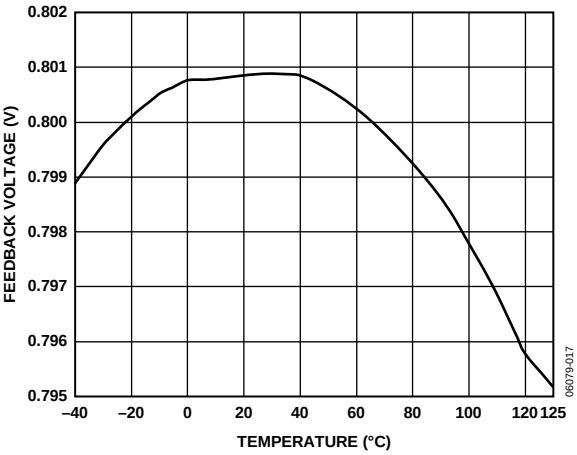



Figure 18. Feedback Voltage vs. Temperature

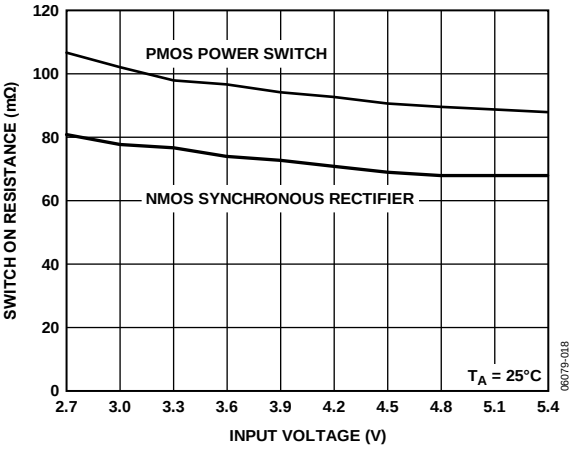



Figure 21. Switch On Resistance vs. Input Voltage—ADP2106 and ADP2107

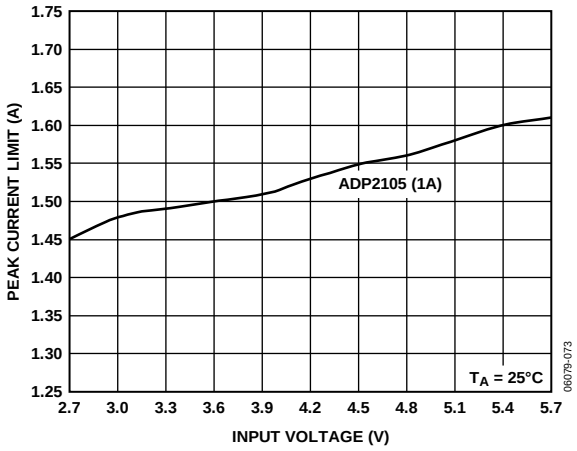



Figure 19. Peak Current Limit of ADP2105

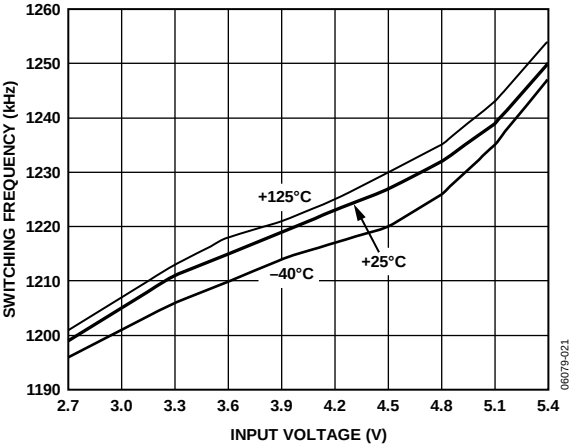



Figure 22. Switching Frequency vs. Input Voltage

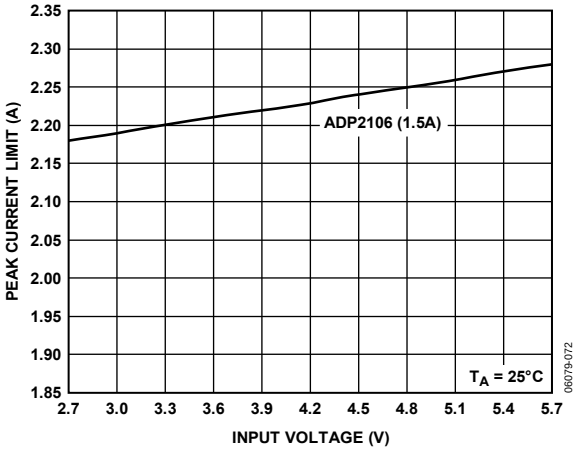



Figure 23. Peak Current Limit of ADP2106

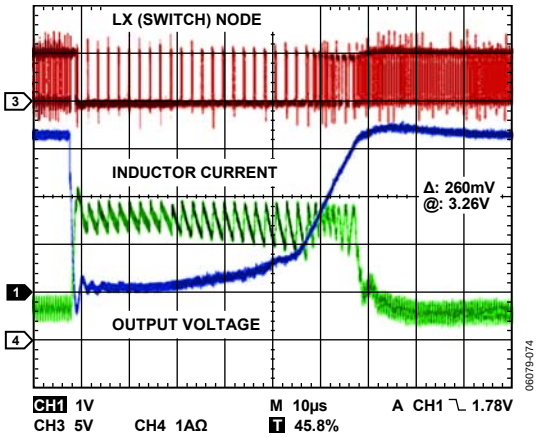



Figure 26. Short-Circuit Response at Output

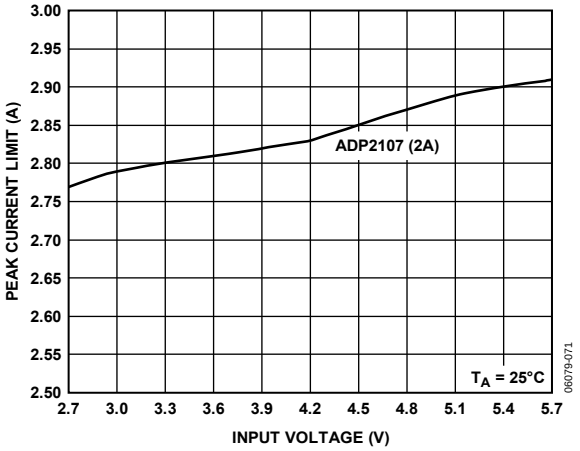



Figure 24. Peak Current Limit of ADP2107

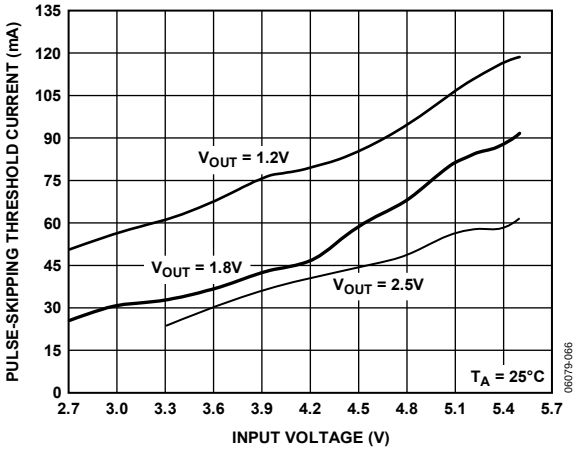



Figure 27. Pulse-Skipping Threshold vs. Input Voltage for ADP2105

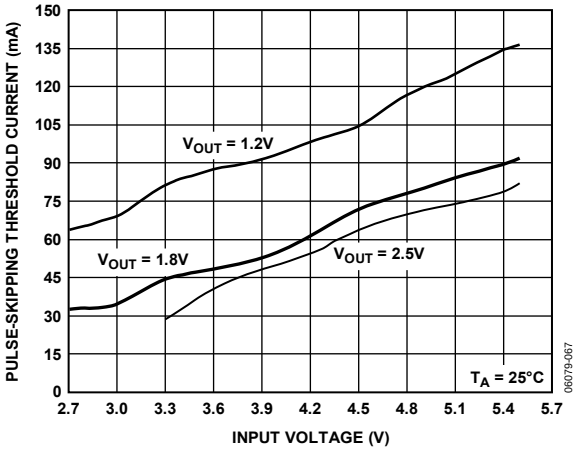



Figure 25. Pulse-Skipping Threshold vs. Input Voltage for ADP2106

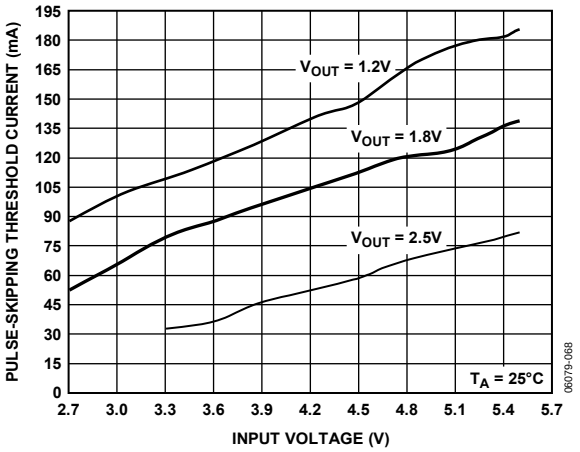



Figure 28. Pulse-Skipping Threshold vs. Input Voltage for ADP2107

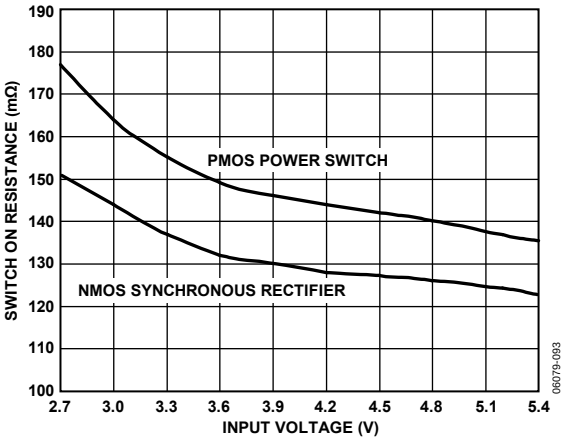



Figure 29. Switch On Resistance vs. Temperature—ADP2105

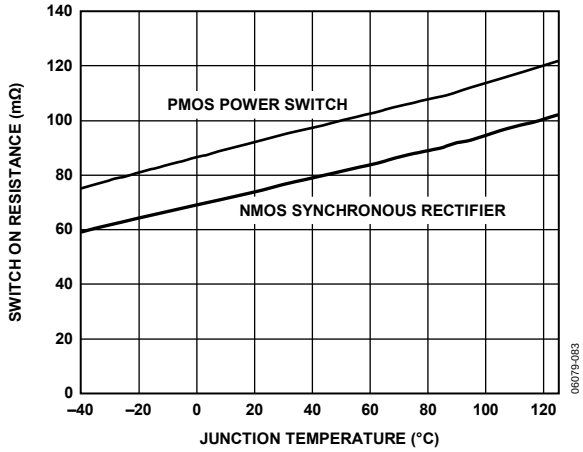



Figure 30. Switch On Resistance vs. Temperature—ADP2106 and ADP2107

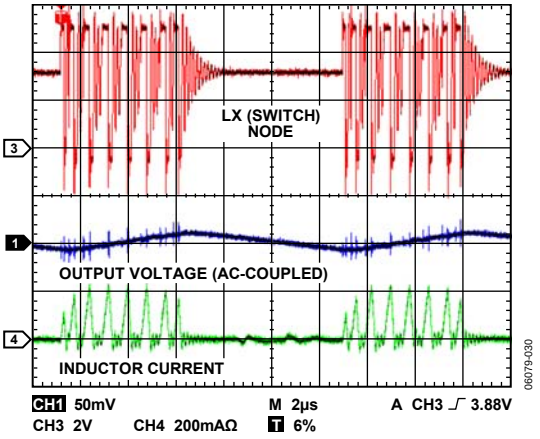



Figure 31. PFM Mode of Operation at Very Light Load (10 mA)

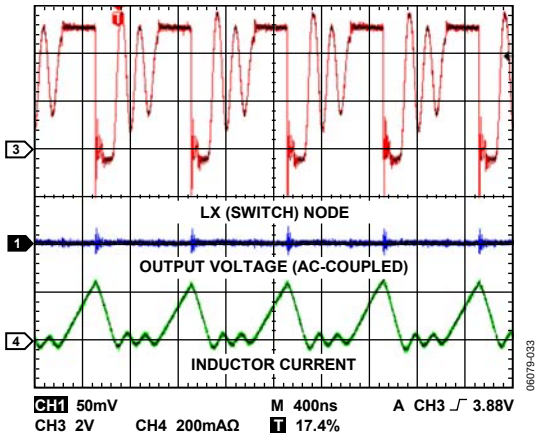



Figure 32. DCM Mode of Operation at Light Load (100 mA)

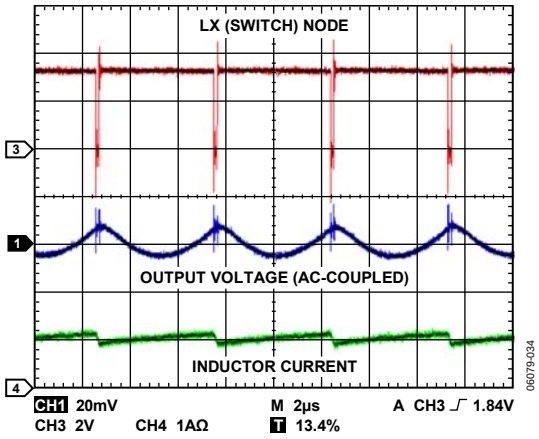



Figure 33. Minimum Off Time Control at Dropout

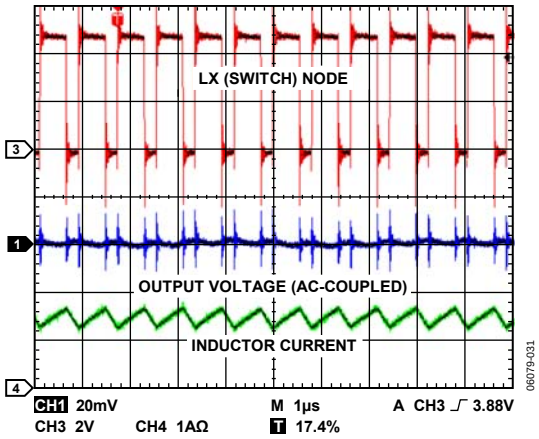



Figure 34. PWM Mode of Operation at Medium/Heavy Load (1.5 A)

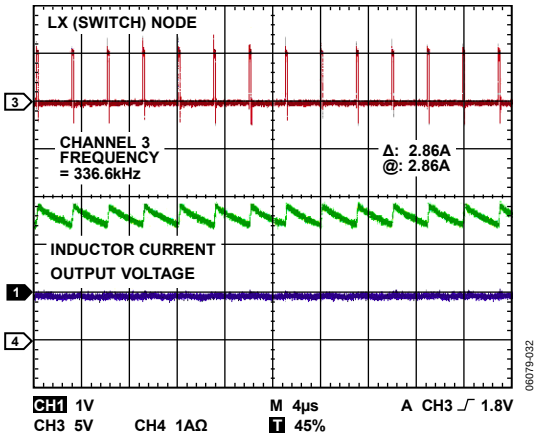



Figure 35. Current Limit Behavior of ADP2107 (Frequency Foldback)

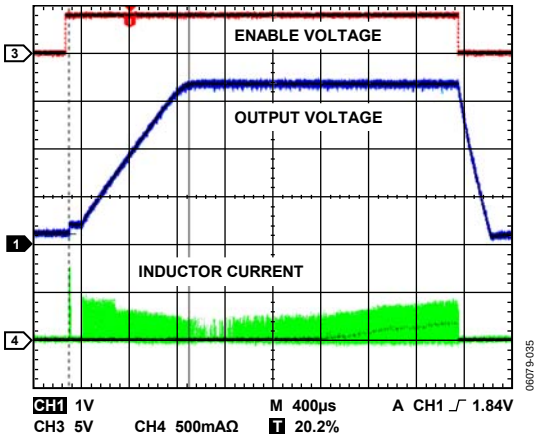



Figure 36. Startup and Shutdown Waveform ($C_{SS}$ = 1 nF → SS Time = 1 ms)

# THEORY OF OPERATION

The ADP2105/ADP2106/ADP2107 are step-down, dc-to-dc converters that use a fixed frequency, peak current mode architecture with an integrated high-side switch and low-side synchronous rectifier. The high 1.2 MHz switching frequency and tiny 16-lead, 4 mm × 4 mm LFCSP package allow for a small step-down dc-to-dc converter solution. The integrated high-side switch (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET) yield high efficiency at medium to heavy loads. Light load efficiency is improved by smoothly transitioning to variable frequency PFM mode.

The ADP2105/ADP2106/ADP2107 (ADJ) operate with an input voltage from 2.7 V to 5.5 V and regulate an output voltage down to 0.8 V. The ADP2105/ADP2106/ADP2107 are also available with preset output voltage options of 3.3 V, 1.8 V, 1.5 V, and 1.2 V.

## CONTROL SCHEME

The ADP2105/ADP2106/ADP2107 operate with a fixed frequency, peak current mode PWM control architecture at medium to high loads for high efficiency, but shift to a variable frequency PFM control scheme at light loads for lower quiescent current. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted to regulate the output voltage, but when operating in PFM mode at light loads, the switching frequency is adjusted to regulate the output voltage.

The ADP2105/ADP2106/ADP2107 operate in the PWM mode only when the load current is greater than the pulse-skipping threshold current. At load currents below this value, the converter smoothly transitions to the PFM mode of operation.

## PWM MODE OPERATION

In PWM mode, the ADP2105/ADP2106/ADP2107 operate at a fixed frequency of 1.2 MHz set by an internal oscillator. At the start of each oscillator cycle, the P-channel MOSFET switch is turned on, putting a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current level that turns off the P-channel MOSFET switch and turns on the N-channel MOSFET synchronous rectifier. This puts a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the remainder of the cycle, unless the inductor current reaches zero, which causes the zero-crossing comparator to turn off the N-channel MOSFET. The peak inductor current is set by the voltage on the COMP pin. The COMP pin is the output of a transconductance error amplifier that compares the feedback voltage with an internal 0.8 V reference.

## PFM MODE OPERATION

The ADP2105/ADP2106/ADP2107 smoothly transition to the variable frequency PFM mode of operation when the load current decreases below the pulse skipping threshold current, switching only as necessary to maintain the output voltage within regulation. When the output voltage dips below regulation, the ADP2105/ADP2106/ADP2107 enter PWM mode for a few oscillator cycles to increase the output voltage back to regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies all the load current. Because the output voltage dips and recovers occasionally, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

## PULSE-SKIPPING THRESHOLD

The output current at which the ADP2105/ADP2106/ADP2107 transition from variable frequency PFM control to fixed frequency PWM control is called the pulse-skipping threshold. The pulse-skipping threshold is optimized for excellent efficiency over all load currents. The variation of pulse-skipping threshold with input voltage and output voltage is shown in Figure 25, Figure 27, and Figure 28.

## 100% DUTY CYCLE OPERATION (LDO MODE)

As the input voltage drops, approaching the output voltage, the ADP2105/ADP2106/ADP2107 smoothly transition to 100% duty cycle, maintaining the P-channel MOSFET switch-on continuously. This allows the ADP2105/ADP2106/ADP2107 to regulate the output voltage until the drop in input voltage forces the P-channel MOSFET switch to enter dropout, as shown in the following equation:

$$V_{IN(MIN)} = I_{OUT} \times (R_{DS(ON)-P} + DCR_{IND}) + V_{OUT(NOM)}$$

The ADP2105/ADP2106/ADP2107 achieve 100% duty cycle operation by stretching the P-channel MOSFET switch-on time if the inductor current does not reach the peak inductor current level by the end of the clock cycle. When this happens, the oscillator remains off until the inductor current reaches the peak inductor current level, at which time the switch is turned off and the synchronous rectifier is turned on for a fixed off time. At the end of the fixed off time, another cycle is initiated. As the ADP2105/ADP2106/ADP2107 approach dropout, the switching frequency decreases gradually to smoothly transition to 100% duty cycle operation.

## SLOPE COMPENSATION

Slope compensation stabilizes the internal current control loop of the ADP2105/ADP2106/ADP2107 when operating beyond 50% duty cycle to prevent subharmonic oscillations. It is implemented by summing a fixed, scaled voltage ramp to the current sense signal during the on-time of the P-channel MOSFET switch.

The slope compensation ramp value determines the minimum inductor that can prevent subharmonic oscillations at a given output voltage. For slope compensation ramp values, see Table 5. For more information see the Inductor Selection section.

**Table 5. Slope Compensation Ramp Values**

| Device | Slope Compensation Ramp Values |
|---|---|
| ADP2105 | 0.72 A/µs |
| ADP2106 | 1.07 A/µs |
| ADP2107 | 1.38 A/µs |

## DESIGN FEATURES

### *Enable/Shutdown*

Drive EN high to turn on the ADP2105/ADP2106/ADP2107. Drive EN low to turn off the ADP2105/ADP2106/ADP2107, reducing the input current below 0.1 µA. To force the ADP2105/ADP2106/ADP2107 to automatically start when input power is applied, connect EN to IN. When shut down, the ADP2105/ADP2106/ADP2107 discharge the soft start capacitor, causing a new soft start cycle every time they are re-enabled.

### *Synchronous Rectification*

In addition to the P-channel MOSFET switch, the ADP2105/ADP2106/ADP2107 include an integrated N-channel MOSFET synchronous rectifier. The synchronous rectifier improves efficiency, especially at low output voltage, and reduces cost and board space by eliminating the need for an external rectifier.

### *Current Limit*

The ADP2105/ADP2106/ADP2107 have protection circuitry to limit the direction and amount of current flowing through the power switch and synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output, and the negative current limit on the synchronous rectifier prevents the inductor current from reversing direction and flowing out of the load.

### *Short-Circuit Protection*

The ADP2105/ADP2106/ADP2107 include frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below 0.3 V, indicating the possibility of a hard short at the output, the switching frequency is reduced to 1/4 of the internal oscillator frequency. The reduction in the switching frequency results in more time for the inductor to discharge, preventing a runaway of output current.

### *Undervoltage Lockout (UVLO)*

To protect against deep battery discharge, UVLO circuitry is integrated on the ADP2105/ADP2106/ADP2107. If the input voltage drops below the 2.2 V UVLO threshold, the ADP2105/ADP2106/ADP2107 shut down, and both the power switch and synchronous rectifier turn off. When the voltage again rises above the UVLO threshold, the soft start period is initiated, and the device is enabled.

### *Thermal Protection*

In the event that the ADP2105/ADP2106/ADP2107 junction temperatures rise above 140°C, the thermal shutdown circuit turns off the converter. Extreme junction temperatures can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 40°C hysteresis is included so that when thermal shutdown occurs, the ADP2105/ADP2106/ ADP2107 do not return to operation until the on-chip temperature drops below 100°C. When coming out of thermal shutdown, soft start is initiated.

### *Soft Start*

The ADP2105/ADP2106/ADP2107 include soft start circuitry to limit the output voltage rise time to reduce inrush current at startup. To set the soft start period, connect the soft start capacitor ($C_{SS}$) from SS to AGND. When the ADP2105/ADP2106/ADP2107 are disabled, or if the input voltage is below the undervoltage lockout threshold, $C_{SS}$ is internally discharged. When the ADP2105/ADP2106/ADP2107 are enabled, $C_{SS}$ is charged through an internal 0.8 µA current source, causing the voltage at SS to rise linearly. The output voltage rises linearly with the voltage at SS.

# APPLICATIONS INFORMATION

## ADIsimPower DESIGN TOOL

The ADP2105/ADP2106/ADP2107 is supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

## EXTERNAL COMPONENT SELECTION

The external component selection for the ADP2105/ADP2106/ADP2107 application circuits shown in Figure 37 and Figure 38 depend on input voltage, output voltage, and load current requirements. Additionally, trade-offs between performance parameters like efficiency and transient response can be made by varying the choice of external components.

## SETTING THE OUTPUT VOLTAGE

The output voltage of ADP2105/ADP2106/ADP2107 (ADJ) is externally set by a resistive voltage divider from the output voltage to FB. The ratio of the resistive voltage divider sets the output voltage, and the absolute value of those resistors sets the divider string current. For lower divider string currents, the small 10 nA (0.1 µA maximum) FB bias current is to be taken into account when calculating resistor values. The FB bias current can be ignored for a higher divider string current, but this degrades efficiency at very light loads.

To limit output voltage accuracy degradation due to FB bias current to less than 0.05% (0.5% maximum), ensure that the divider string current is greater than 20 µA. To calculate the desired resistor values, first determine the value of the bottom divider string resistor ($R_{BOT}$) using the following equation:

$$R_{BOT} = \frac{V_{FB}}{I_{STRING}}$$

where:

$V_{FB}$ = 0.8 V, the internal reference.

$I_{STRING}$ is the resistor divider string current.

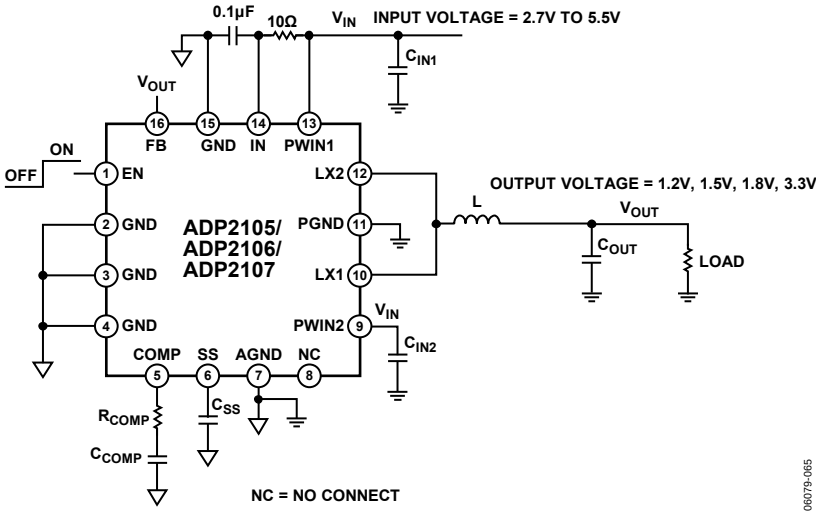



*Figure 37. Typical Applications Circuit for Fixed Output Voltage Options of ADP2105/ADP2106/ADP2107(x.x V)*

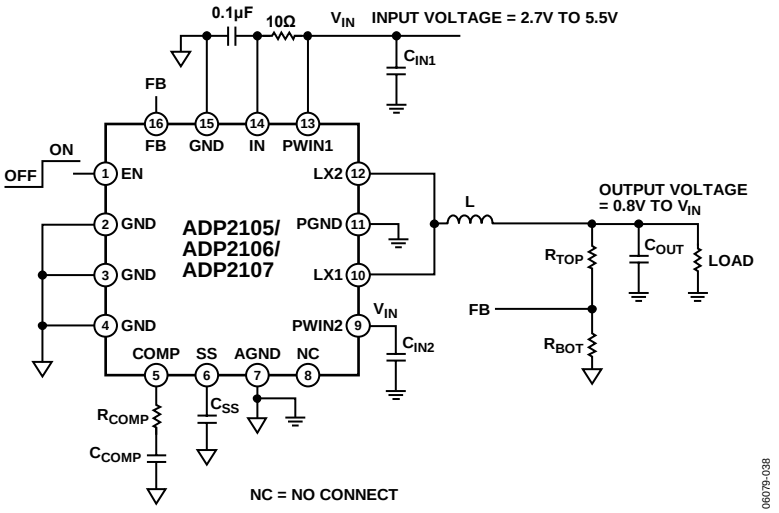



*Figure 38. Typical Applications Circuit for Adjustable Output Voltage Option of ADP2105/ADP2106/ADP2107 (ADJ)*

When $R_{BOT}$ is determined, calculate the value of the top resistor ($R_{TOP}$) by using the following equation:

$$R_{TOP} = R_{BOT}\left[\frac{V_{OUT} - V_{FB}}{V_{FB}}\right]$$

The ADP2105/ADP2106/ADP2107(x.x V) include the resistive voltage divider internally, reducing the external circuitry required. For improved load regulation, connect the FB to the output voltage as close as possible to the load.

## INDUCTOR SELECTION

The high switching frequency of ADP2105/ADP2106/ADP2107 allows minimal output voltage ripple even with small inductors. The sizing of the inductor is a trade-off between efficiency and transient response. A small inductor leads to larger inductor current ripple that provides excellent transient response but degrades efficiency. Due to the high switching frequency of ADP2105/ADP2106/ADP2107, shielded ferrite core inductors are recommended for their low core losses and low electromagnetic interference (EMI).

As a guideline, the inductor peak-to-peak current ripple ($\Delta I_L$) is typically set to 1/3 of the maximum load current for optimal transient response and efficiency, as shown in the following equations:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \approx \frac{I_{LOAD(MAX)}}{3}$$

$$\Rightarrow L_{IDEAL} = \frac{2.5 \times V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times I_{LOAD(MAX)}} \mu H$$

where $f_{SW}$ is the switching frequency (1.2 MHz).

The ADP2105/ADP2106/ADP2107 use slope compensation in the current control loop to prevent subharmonic oscillations when operating beyond 50% duty cycle. The fixed slope compensation limits the minimum inductor value as a function of output voltage.

For the ADP2105

$$L > (1.12\ \mu H/V) \times V_{OUT}$$

For the ADP2106

$$L > (0.83\ \mu H/V) \times V_{OUT}$$

For the ADP2107

$$L > (0.66\ \mu H/V) \times V_{OUT}$$

Inductors 4.7 µH or larger are not recommended because they may cause instability in discontinuous conduction mode under light load conditions. It is also important that the inductor be capable of handling the maximum peak inductor current ($I_{PK}$) determined by the following equation:

$$I_{PK} = I_{LOAD(MAX)} + \left(\frac{\Delta I_L}{2}\right)$$

**Table 6. Minimum Inductor Value for Common Output Voltage Options for the ADP2105 (1 A)**

| | $V_{IN}$ | | | |
|---|---|---|---|---|
| $V_{OUT}$ | 2.7 V | 3.6 V | 4.2 V | 5.5 V |
| 1.2 V | 1.67 µH | 2.00 µH | 2.14 µH | 2.35 µH |
| 1.5 V | 1.68 µH | 2.19 µH | 2.41 µH | 2.73 µH |
| 1.8 V | 2.02 µH | 2.25 µH | 2.57 µH | 3.03 µH |
| 2.5 V | 2.80 µH | 2.80 µH | 2.80 µH | 3.41 µH |
| 3.3 V | 3.70 µH | 3.70 µH | 3.70 µH | 3.70 µH |

**Table 7. Minimum Inductor Value for Common Output Voltage Options for the ADP2106 (1.5 A)**

| | $V_{IN}$ | | | |
|---|---|---|---|---|
| $V_{OUT}$ | 2.7 V | 3.6 V | 4.2 V | 5.5 V |
| 1.2 V | 1.11 µH | 2.33 µH | 2.43 µH | 1.56 µH |
| 1.5 V | 1.25 µH | 1.46 µH | 1.61 µH | 1.82 µH |
| 1.8 V | 1.49 µH | 1.50 µH | 1.71 µH | 2.02 µH |
| 2.5 V | 2.08 µH | 2.08 µH | 2.08 µH | 2.27 µH |
| 3.3 V | 2.74 µH | 2.74 µH | 2.74 µH | 2.74 µH |

**Table 8. Minimum Inductor Value for Common Output Voltage Options for the ADP2107 (2 A)**

| | $V_{IN}$ | | | |
|---|---|---|---|---|
| $V_{OUT}$ | 2.7 V | 3.6 V | 4.2 V | 5.5 V |
| 1.2 V | 0.83 µH | 1.00 µH | 1.07 µH | 1.17 µH |
| 1.5 V | 0.99 µH | 1.09 µH | 1.21 µH | 1.36 µH |
| 1.8 V | 1.19 µH | 1.19 µH | 1.29 µH | 1.51 µH |
| 2.5 V | 1.65 µH | 1.65 µH | 1.65 µH | 1.70 µH |
| 3.3 V | 2.18 µH | 2.18 µH | 2.18 µH | 2.18 µH |

**Table 9. Inductor Recommendations for the ADP2105/ ADP2106/ADP2107**

| Vendor | Small-Sized Inductors (< 5 mm × 5 mm) | Large-Sized Inductors (> 5 mm × 5 mm) |
|---|---|---|
| Sumida | CDRH2D14, 3D16, 3D28 | CDRH4D18, 4D22, 4D28, 5D18, 6D12 |
| Toko | 1069AS-DB3018, 1098AS-DE2812, 1070AS-DB3020 | D52LC, D518LC, D62LCB |
| Coilcraft | LPS3015, LPS4012, DO3314 | DO1605T |
| Cooper Bussmann | SD3110, SD3112, SD3114, SD3118, SD3812, SD3814 | SD10, SD12, SD14, SD52 |

## OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the converter. For a given loop crossover frequency (the frequency at which the loop gain drops to 0 dB), the maximum voltage transient excursion (overshoot) is inversely proportional to the value of the output capacitor. Therefore, larger output capacitors result in improved load transient response. To minimize the effects of the dc-to-dc converter switching, the cross-over frequency of the compensation loop must be less than 1/10 of the switching frequency. Higher crossover frequency leads to faster settling time for a load transient response, but it can also cause ringing due to poor phase margin. Lower crossover frequency helps to provide stable operation but needs large output capacitors to achieve competitive overshoot specifications. Therefore, the optimal crossover frequency for the control loop of ADP2105/ADP2106/ADP2107 is 80 kHz, 1/15 of the switching frequency. For a crossover frequency of 80 kHz, Figure 39 shows the maximum output voltage excursion during a 1 A load transient, as the product of the output voltage and the output capacitor is varied. Choose the output capacitor based on the desired load transient response and target output voltage.

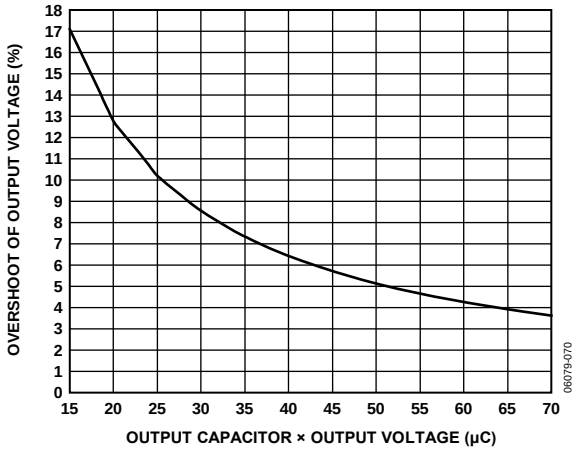



*Figure 39. Percentage Overshoot for a 1 A Load Transient Response vs. Output Capacitor × Output Voltage*

For example, if the desired 1 A load transient response (overshoot) is 5% for an output voltage of 2.5 V, then from Figure 39

Output Capacitor × Output Voltage = 50 µC

$$\Rightarrow Output\ Capacitor = \frac{50\,\mu C}{2.5} \approx 20\,\mu F$$

The ADP2105/ADP2106/ADP2107 have been designed for operation with small ceramic output capacitors that have low ESR and ESL. Therefore, they are comfortably able to meet tight output voltage ripple specifications. X5R or X7R dielectrics are recommended with a voltage rating of 6.3 V or 10 V. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics. Table 10 shows a list of recommended MLCC capacitors from Murata and Taiyo Yuden.

When choosing output capacitors, it is also important to account for the loss of capacitance due to output voltage dc bias. Figure 40 shows the loss of capacitance due to output voltage dc bias for three X5R MLCC capacitors from Murata.

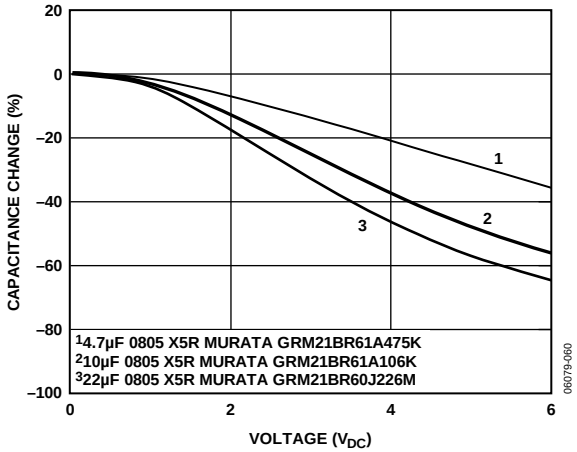



*Figure 40. Percentage Drop-In Capacitance vs. DC Bias for Ceramic Capacitors (Information Provided by Murata Corporation)*

For example, to get 20 µF output capacitance at an output voltage of 2.5 V, based on Figure 40, as well as to give some margin for temperature variance, a 22 µF and a 10 µF capacitor are to be used in parallel to ensure that the output capacitance is sufficient under all conditions for stable behavior.

**Table 10. Recommended Input and Output Capacitor Selection for the ADP2105/ADP2106/ADP2107**

| | Vendor | |
|---|---|---|
| **Capacitor** | **Murata** | **Taiyo Yuden** |
| 4.7 µF, 10 V X5R 0805 | GRM21BR61A475K | LMK212BJ475KG |
| 10 µF, 10 V X5R 0805 | GRM21BR61A106K | LMK212BJ106KG |
| 22 µF, 6.3 V X5R 0805 | GRM21BR60J226M | JMK212BJ226MG |

## INPUT CAPACITOR SELECTION

The input capacitor reduces input voltage ripple caused by the switch currents on the PWIN pins. Place the input capacitors as close as possible to the PWIN pins. Select an input capacitor capable of withstanding the rms input current for the maximum load current in your application.

For the ADP2105, it is recommended that each PWIN pin be bypassed with a 4.7 µF or larger input capacitor. For the ADP2106, bypass each PWIN pin with a 10 µF and a 4.7 µF capacitor, and for the ADP2107, bypass each PWIN pin with a 10 µF capacitor.

As with the output capacitor, a low ESR ceramic capacitor is recommended to minimize input voltage ripple. X5R or X7R dielectrics are recommended, with a voltage rating of 6.3 V or 10 V. Y5V and Z5U dielectrics are not recommended due to their poor temperature and dc bias characteristics. Refer to Table 10 for input capacitor recommendations.

## INPUT FILTER

The IN pin is the power source for the ADP2105/ADP2106/ADP2107 internal circuitry, including the voltage reference and current sense amplifier that are sensitive to power supply noise. To prevent high frequency switching noise on the PWIN pins from corrupting the internal circuitry of the ADP2105/ADP2106/ADP2107, a low-pass RC filter must be placed between the IN pin and the PWIN1 pin. The suggested input filter consists of a small 0.1 µF ceramic capacitor placed between IN and AGND and a 10 Ω resistor placed between IN and PWIN1. This forms a 150 kHz low-pass filter between PWIN1 and IN that prevents any high frequency noise on PWIN1 from coupling into the IN pin.

## SOFT START PERIOD

To set the soft start period, connect a soft start capacitor ($C_{SS}$) from SS to AGND. The soft start period varies linearly with the size of the soft start capacitor, as shown in the following equation:

$$T_{SS} = C_{SS} \times 10^9 \text{ ms}$$

For a soft start period of 1 ms, a 1 nF capacitor must be connected between SS and AGND.

## LOOP COMPENSATION

The ADP2105/ADP2106/ADP2107 utilize a transconductance error amplifier to compensate the external voltage loop. The open loop transfer function at angular frequency (s) is given by

$$H(s) = G_m G_{CS}\left(\frac{Z_{COMP}(s)}{sC_{OUT}}\right)\left(\frac{V_{REF}}{V_{OUT}}\right)$$

where:
$V_{REF}$ is the internal reference voltage (0.8 V).
$V_{OUT}$ is the nominal output voltage.
$Z_{COMP}(s)$ is the impedance of the compensation network at the angular frequency.
$C_{OUT}$ is the output capacitor.
$g_m$ is the transconductance of the error amplifier (50 µA/V nominal).
$G_{CS}$ is the effective transconductance of the current loop.

$G_{CS}$ = 1.875 A/V for the ADP2105.
$G_{CS}$ = 2.8125 A/V for the ADP2106.
$G_{CS}$ = 3.625 A/V for the ADP2107.

The transconductance error amplifier drives the compensation network that consists of a resistor ($R_{COMP}$) and capacitor ($C_{COMP}$) connected in series to form a pole and a zero, as shown in the following equation:

$$Z_{COMP}(s) = \left(R_{COMP} + \frac{1}{sC_{COMP}}\right) = \left(\frac{1 + sR_{COMP}C_{COMP}}{sC_{COMP}}\right)$$

At the crossover frequency, the gain of the open loop transfer function is unity. For the compensation network impedance at the crossover frequency, this yields the following equation:

$$Z_{COMP}(F_{CROSS}) = \left(\frac{(2\pi)F_{CROSS}}{G_m G_{CS}}\right)\left(\frac{C_{OUT}V_{OUT}}{V_{REF}}\right)$$

where:
$F_{CROSS}$ = 80 kHz, the crossover frequency of the loop.
$C_{OUT}V_{OUT}$ is determined from the Output Capacitor Selection section.

To ensure that there is sufficient phase margin at the crossover frequency, place the compensator zero at 1/4 of the crossover frequency, as shown in the following equation:

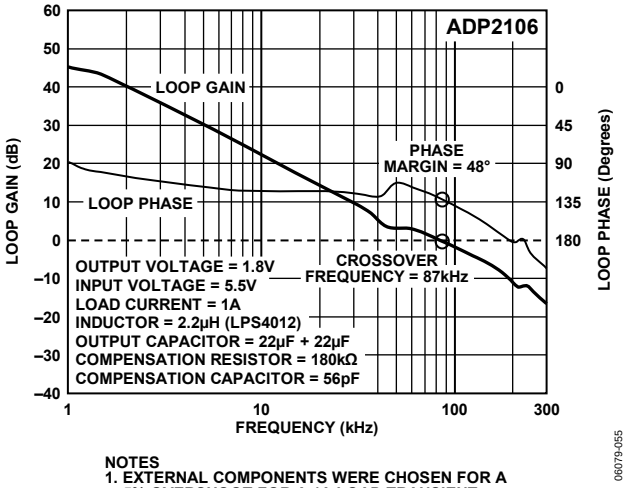
$$(2\pi)\left(\frac{F_{CROSS}}{4}\right)R_{COMP}C_{COMP} = 1$$

Solving the three equations in this section simultaneously yields the value for the compensation resistor and compensation capacitor, as shown in the following equation:

$$R_{COMP} = 0.8\left(\frac{(2\pi)F_{CROSS}}{G_m G_{CS}}\right)\left(\frac{C_{OUT}V_{OUT}}{V_{REF}}\right)$$

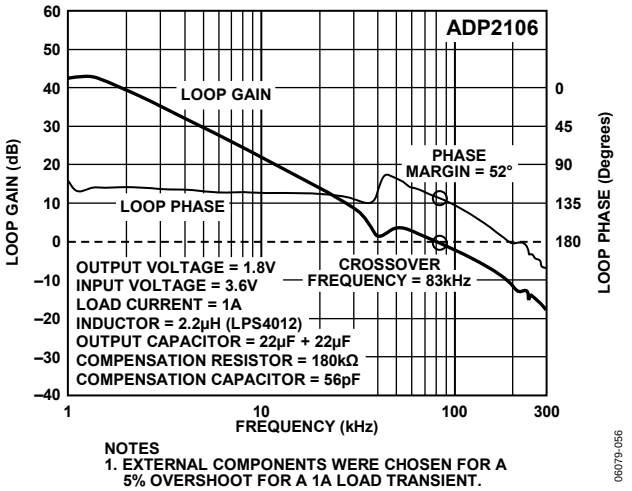
$$C_{COMP} = \frac{2}{\pi F_{CROSS} R_{COMP}}$$

## BODE PLOTS



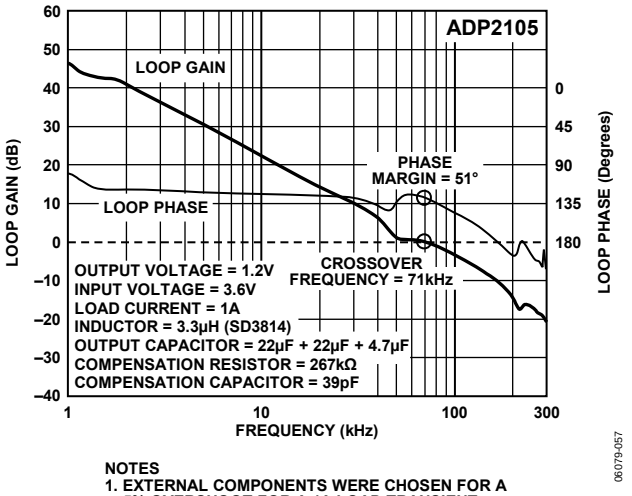

NOTES
1. EXTERNAL COMPONENTS WERE CHOSEN FOR A 5% OVERSHOOT FOR A 1A LOAD TRANSIENT.

*Figure 41. ADP2106 Bode Plot at $V_{IN}$ = 5.5 V, $V_{OUT}$ = 1.8 V and Load = 1 A*



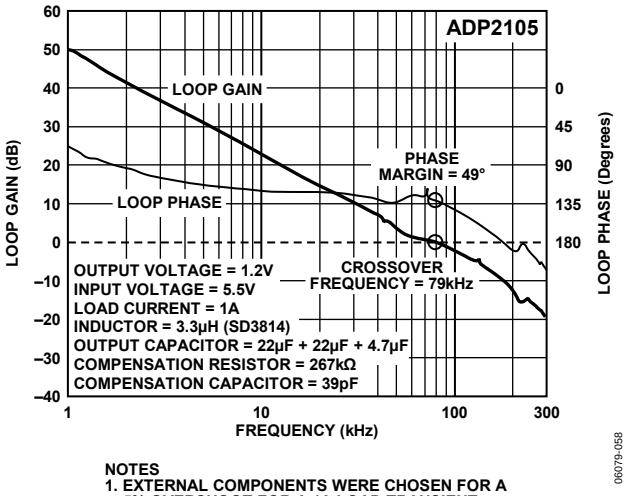

NOTES
1. EXTERNAL COMPONENTS WERE CHOSEN FOR A 5% OVERSHOOT FOR A 1A LOAD TRANSIENT.

*Figure 42. ADP2106 Bode Plot at $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.8 V, and Load = 1 A*



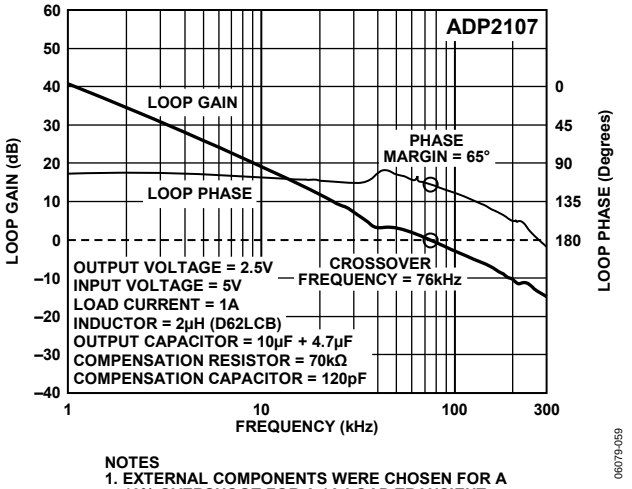

NOTES
1. EXTERNAL COMPONENTS WERE CHOSEN FOR A 5% OVERSHOOT FOR A 1A LOAD TRANSIENT.

*Figure 43. ADP2105 Bode Plot at $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.2 V, and Load = 1 A*



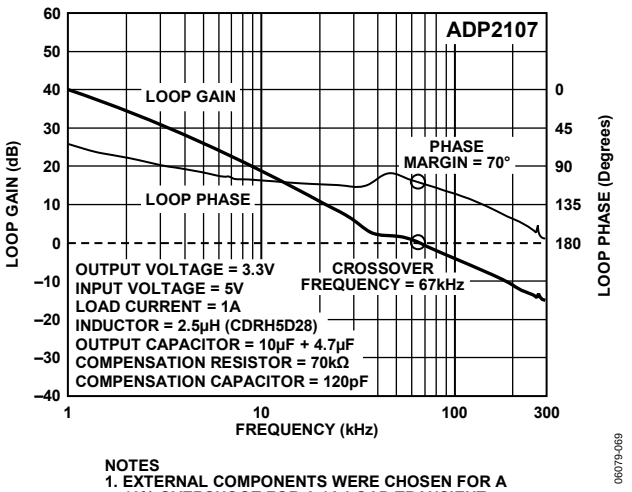

NOTES
1. EXTERNAL COMPONENTS WERE CHOSEN FOR A 5% OVERSHOOT FOR A 1A LOAD TRANSIENT.

*Figure 44. ADP2105 Bode Plot at $V_{IN}$ = 5.5 V, $V_{OUT}$ = 1.2 V and Load = 1 A*




NOTES
1. EXTERNAL COMPONENTS WERE CHOSEN FOR A 10% OVERSHOOT FOR A 1A LOAD TRANSIENT.

*Figure 45. ADP2107 Bode Plot at $V_{IN}$ = 5 V, $V_{OUT}$ = 2.5 V and Load = 1 A*




NOTES
1. EXTERNAL COMPONENTS WERE CHOSEN FOR A 10% OVERSHOOT FOR A 1A LOAD TRANSIENT.

*Figure 46. ADP2107 Bode Plot at $V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, and Load = 1 A*

## LOAD TRANSIENT RESPONSE

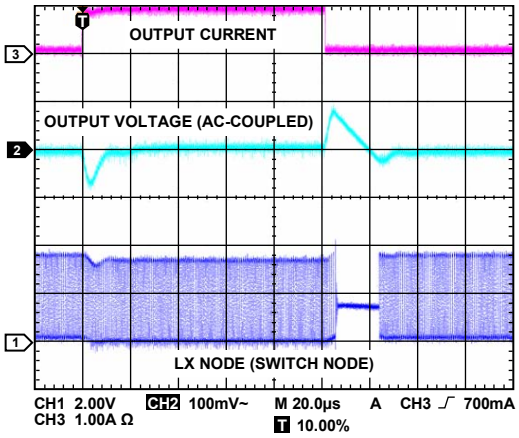



*Figure 47. 1 A Load Transient Response for ADP2105-1.2 with External Components Chosen for 5% Overshoot*

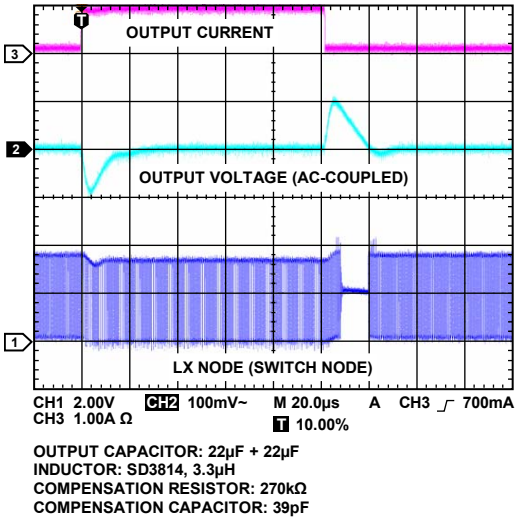



*Figure 48. 1 A Load Transient Response for ADP2105-1.8 with External Components Chosen for 5% Overshoot*

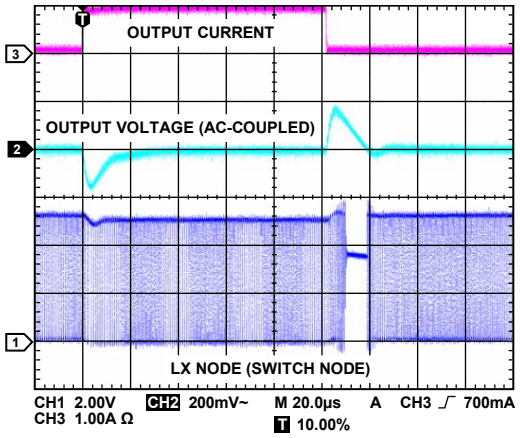



*Figure 49. 1 A Load Transient Response for ADP2105-3.3 with External Components Chosen for 5% Overshoot*

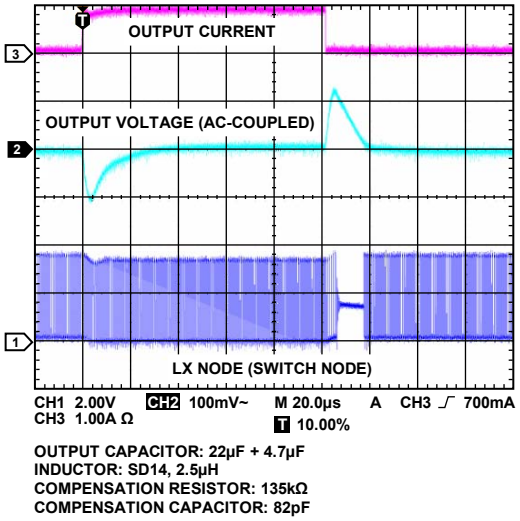



*Figure 50. 1 A Load Transient Response for ADP2105-1.2 with External Components Chosen for 10% Overshoot*

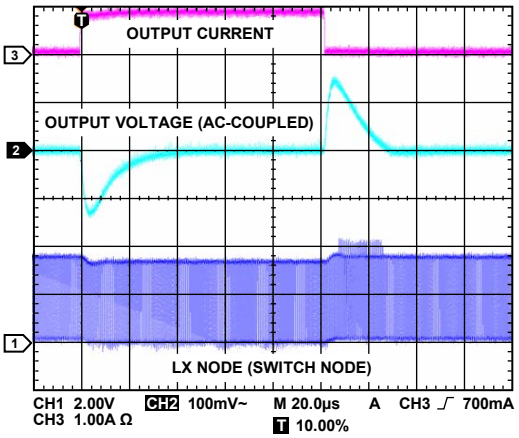



*Figure 51. 1 A Load Transient Response for ADP2105-1.8 with External Components Chosen for 10% Overshoot*

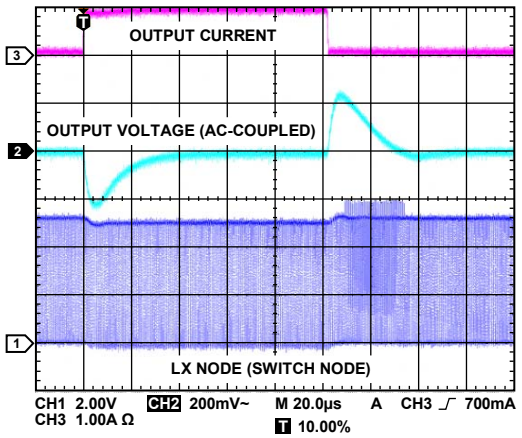



*Figure 52. 1 A Load Transient Response for ADP2105-3.3 with External Components Chosen for 10% Overshoot*

## EFFICIENCY CONSIDERATIONS

Efficiency is the ratio of output power to input power. The high efficiency of the ADP2105/ADP2106/ADP2107 has two distinct advantages. First, only a small amount of power is lost in the dc-to-dc converter package that reduces thermal constraints. Second, the high efficiency delivers the maximum output power for the given input power, extending battery life in portable applications.

There are four major sources of power loss in dc-to-dc converters like the ADP2105/ADP2106/ADP2107:

- Power switch conduction losses
- Inductor losses
- Switching losses
- Transition losses

### *Power Switch Conduction Losses*

Power switch conduction losses are caused by the flow of output current through the P-channel power switch and the N-channel synchronous rectifier, which have internal resistances ($R_{DS(ON)}$) associated with them. The amount of power loss can be approximated by

$$P_{SW-COND} = [R_{DS(ON)-P} \times D + R_{DS(ON)-N} \times (1 - D)] \times I_{OUT}^2$$

where $D = V_{OUT}/V_{IN}$.

The internal resistance of the power switches increases with temperature but decreases with higher input voltage. Figure 20 and Figure 21 show the change in $R_{DS(ON)}$ vs. input voltage, whereas Figure 29 and Figure 30 show the change in $R_{DS(ON)}$ vs. temperature for both power devices.

### *Inductor Losses*

Inductor conduction losses are caused by the flow of current through the inductor, which has an internal resistance (DCR) associated with it. Larger sized inductors have smaller DCR, which can improve inductor conduction losses.

Inductor core losses are related to the magnetic permeability of the core material. Because the ADP2105/ADP2106/ADP2107 are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for the low core losses and low EMI.

The total amount of inductor power loss can be calculated by

$$P_L = DCR \times I_{OUT}^2 + Core\ Losses$$

### *Switching Losses*

Switching losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. Each time a power device gate is turned on and turned off, the driver transfers a charge ΔQ from the input supply to the gate and then from the gate to ground.

The amount of power loss can by calculated by

$$P_{SW} = (C_{GATE-P} + C_{GATE-N}) \times V_{IN}^2 \times f_{SW}$$

where:
$(C_{GATE-P} + C_{GATE-N}) \approx 600$ pF.
$f_{SW} = 1.2$ MHz, the switching frequency.

### *Transition Losses*

Transition losses occur because the P-channel MOSFET power switch cannot turn on or turn off instantaneously. At the middle of an LX (switch) node transition, the power switch is providing all the inductor current, while the source to drain voltage of the power switch is half the input voltage, resulting in power loss. Transition losses increase with load current and input voltage and occur twice for each switching cycle.

The amount of power loss can be calculated by

$$P_{TRAN} = \frac{V_{IN}}{2} \times I_{OUT} \times (t_{ON} + t_{OFF}) \times f_{SW}$$

where $t_{ON}$ and $t_{OFF}$ are the rise time and fall time of the LX (switch) node, and are both approximately 3 ns.

## THERMAL CONSIDERATIONS

In most applications, the ADP2105/ADP2106/ADP2107 do not dissipate a lot of heat due to their high efficiency. However, in applications with high ambient temperature, low supply voltage, and high duty cycle, the heat dissipated in the package is large enough that it can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C. Once the junction temperature exceeds 140°C, the converter goes into thermal shutdown. To prevent any permanent damage it recovers only after the junction temperature has decreased below 100°C. Therefore, thermal analysis for the chosen application solution is very important to guarantee reliable performance over all conditions.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
$T_J$ is the junction temperature.
$T_A$ is the ambient temperature.
$T_R$ is the rise in temperature of the package due to the power dissipation in the package.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is defined as the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
$T_R$ is the rise in temperature of the package.
$P_D$ is the power dissipation in the package.
$\theta_{JA}$ is the thermal resistance from the junction of the die to the ambient temperature of the package.

For example, in an application where the ADP2107(1.8 V) is used with an input voltage of 3.6 V, a load current of 2 A, and a maximum ambient temperature of 85°C, at a load current of 2 A, the most significant contributor of power dissipation in the dc-to-dc converter package is the conduction loss of the power switches. Using the graph of switch on resistance vs. temperature (see Figure 30), as well as the equation of power loss given in the Power Switch Conduction Losses section, the power dissipation in the package can be calculated by the following:

$$P_{SW-COND} = [R_{DS(ON)-P} \times D + R_{DS(ON)-N} \times (1 - D)] \times I_{OUT}^2 =$$

$$[109\ m\Omega \times 0.5 + 90\ m\Omega \times 0.5] \times (2\ A)^2 \approx 400\ mW$$

The $\theta_{JA}$ for the LFCSP package is 40°C/W, as shown in Table 3. Therefore, the rise in temperature of the package due to power dissipation is

$$T_R = \theta_{JA} \times P_D = 40°C/W \times 0.40\ W = 16°C$$

The junction temperature of the converter is

$$T_J = T_A + T_R = 85°C + 16°C = 101°C$$

Because the junction temperature of the converter is below the maximum junction temperature of 125°C, this application operates reliably from a thermal point of view.

# DESIGN EXAMPLE

Consider an application with the following specifications:

- Input Voltage = 3.6 V to 4.2 V.
- Output Voltage = 2 V.
- Typical Output Current = 600 mA.
- Maximum Output Current = 1.2 A.
- Soft Start Time = 2 ms.

Overshoot ≤ 100 mV under all load transient conditions.

1. Choose the dc-to-dc converter that satisfies the maximum output current requirement. Because the maximum output current for this application is 1.2 A, the ADP2106 with a maximum output current of 1.5 A is ideal for this application.
2. See whether the output voltage desired is available as a fixed output voltage option. Because 2 V is not one of the fixed output voltage options available, choose the adjustable version of ADP2106.
3. The first step in external component selection for an adjustable version converter is to calculate the resistance of the resistive voltage divider that sets the output voltage.

$$R_{BOT} = \frac{V_{FB}}{I_{STRING}} = \frac{0.8\text{ V}}{20\ \mu\text{A}} = 40\ \text{k}\Omega$$

$$R_{TOP} = R_{BOT}\left[\frac{V_{OUT} - V_{FB}}{V_{FB}}\right] = 40\ \text{k}\Omega \times \left[\frac{2\text{ V} - 0.8\text{ V}}{0.8\text{ V}}\right] = 60\ \text{k}\Omega$$

Calculate the minimum inductor value as follows:

For the ADP2106:
$L > (0.83\ \mu\text{H/V}) \times V_{OUT}$
$\Rightarrow L > 0.83\ \mu\text{H/V} \times 2\text{ V}$
$\Rightarrow L > 1.66\ \mu\text{H}$
Next, calculate the ideal inductor value that sets the inductor peak-to-peak current ripple ($\Delta I_L$) to 1/3 of the maximum load current at the maximum input voltage as follows:

$$L_{IDEAL} = \frac{2.5 \times V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times I_{LOAD(MAX)}}\ \mu\text{H} =$$

$$\frac{2.5 \times 2 \times (4.2 - 2)}{4.2 \times 1.2}\ \mu\text{H} = 2.18\ \mu\text{H}$$

4. The closest standard inductor value is 2.2 µH. The maximum rms current of the inductor is to be greater than 1.2 A, and the saturation current of the inductor is to be greater than 2 A. One inductor that meets these criteria is the LPS4012-2.2 µH from Coilcraft.
5. Choose the output capacitor based on the transient response requirements. The worst-case load transient is 1.2 A, for which the overshoot must be less than 100 mV, which is 5% of the output voltage. For a 1 A load transient, the overshoot must be less than 4% of the output voltage, then from Figure 39:

Output Capacitor × Output Voltage = 60 µC

$$\Rightarrow Output\ Capacitor = \frac{60\ \mu\text{C}}{2.0\text{ V}} \approx 30\ \mu\text{F}$$

Taking into account the loss of capacitance due to dc bias, as shown in Figure 40, two 22 µF X5R MLCC capacitors from Murata (GRM21BR60J226M) are sufficient for this application.

6. Because the ADP2106 is being used in this application, the input capacitors are 10 µF and 4.7 µF X5R Murata capacitors (GRM21BR61A106K and GRM21BR61A475K).
7. The input filter consists of a small 0.1 µF ceramic capacitor placed between IN and AGND and a 10 Ω resistor placed between IN and PWIN1.
8. Choose a soft start capacitor of 2 nF to achieve a soft start time of 2 ms.
9. Calculate the compensation resistor and capacitor as follows:

$$R_{COMP} = 0.8\left(\frac{(2\pi)F_{CROSS}}{G_m G_{CS}}\right)\left(\frac{C_{OUT}V_{OUT}}{V_{REF}}\right) =$$

$$0.8\left(\frac{(2\pi) \times 80\ \text{kHz}}{50\ \mu\text{A/V} \times 2.8125\ \text{A/V}}\right)\left(\frac{30\ \mu\text{F} \times 2\text{ V}}{0.8\text{ V}}\right) = 215\ \text{k}\Omega$$

$$C_{COMP} = \frac{2}{\pi F_{CROSS} R_{COMP}} = \frac{2}{\pi \times 80\ \text{kHz} \times 215\ \text{k}\Omega} = 39\ \text{pF}$$

# EXTERNAL COMPONENT RECOMMENDATIONS

For popular output voltage options at 80 kHz crossover frequency with 10% overshoot for a 1 A load transient (refer to Figure 37 and Figure 38).

**Table 11. Recommended External Components**

| Device | $V_{OUT}$ (V) | $C_{IN1}$ [1] (µF) | $C_{IN2}$ [1] (µF) | $C_{OUT}$ [2] (µF) | L (µH) | $R_{COMP}$ (kΩ) | $C_{COMP}$ (pF) | $R_{TOP}$ [3] (kΩ) | $R_{BOT}$ [3] (kΩ) |
|---|---|---|---|---|---|---|---|---|---|
| ADP2105 (ADJ) | 0.9 | 4.7 | 4.7 | 22 + 10 | 2.0 | 135 | 82 | 5 | 40 |
| ADP2105 (ADJ) | 1.2 | 4.7 | 4.7 | 22 + 4.7 | 2.5 | 135 | 82 | 20 | 40 |
| ADP2105 (ADJ) | 1.5 | 4.7 | 4.7 | 10 + 10 | 3.0 | 135 | 82 | 35 | 40 |
| ADP2105 (ADJ) | 1.8 | 4.7 | 4.7 | 10 + 10 | 3.3 | 135 | 82 | 50 | 40 |
| ADP2105 (ADJ) | 2.5 | 4.7 | 4.7 | 10 + 4.7 | 3.6 | 135 | 82 | 85 | 40 |
| ADP2105 (ADJ) | 3.3 | 4.7 | 4.7 | 10 + 4.7 | 4.1 | 135 | 82 | 125 | 40 |
| ADP2106 (ADJ) | 0.9 | 4.7 | 10 | 22 + 10 | 1.5 | 90 | 100 | 5 | 40 |
| ADP2106 (ADJ) | 1.2 | 4.7 | 10 | 22 + 4.7 | 1.8 | 90 | 100 | 20 | 40 |
| ADP2106 (ADJ) | 1.5 | 4.7 | 10 | 10 + 10 | 2.0 | 90 | 100 | 35 | 40 |
| ADP2106 (ADJ) | 1.8 | 4.7 | 10 | 10 + 10 | 2.2 | 90 | 100 | 50 | 40 |
| ADP2106 (ADJ) | 2.5 | 4.7 | 10 | 10 + 4.7 | 2.5 | 90 | 100 | 85 | 40 |
| ADP2106 (ADJ) | 3.3 | 4.7 | 10 | 10 + 4.7 | 3.0 | 90 | 100 | 125 | 40 |
| ADP2107 (ADJ) | 0.9 | 10 | 10 | 22 + 10 | 1.2 | 70 | 120 | 5 | 40 |
| ADP2107 (ADJ) | 1.2 | 10 | 10 | 22 + 4.7 | 1.5 | 70 | 120 | 20 | 40 |
| ADP2107 (ADJ) | 1.5 | 10 | 10 | 10 + 10 | 1.5 | 70 | 120 | 35 | 40 |
| ADP2107 (ADJ) | 1.8 | 10 | 10 | 10 + 10 | 1.8 | 70 | 120 | 50 | 40 |
| ADP2107 (ADJ) | 2.5 | 10 | 10 | 10 + 4.7 | 1.8 | 70 | 120 | 85 | 40 |
| ADP2107 (ADJ) | 3.3 | 10 | 10 | 10 + 4.7 | 2.5 | 70 | 120 | 125 | 40 |
| ADP2105-1.2 | 1.2 | 4.7 | 4.7 | 22 + 4.7 | 2.5 | 135 | 82 | N/A | N/A |
| ADP2105-1.5 | 1.5 | 4.7 | 4.7 | 10 + 10 | 3.0 | 135 | 82 | N/A | N/A |
| ADP2105-1.8 | 1.8 | 4.7 | 4.7 | 10 + 10 | 3.3 | 135 | 82 | N/A | N/A |
| ADP2105-3.3 | 3.3 | 4.7 | 4.7 | 10 + 4.7 | 4.1 | 135 | 82 | N/A | N/A |
| ADP2106-1.2 | 1.2 | 4.7 | 10 | 22 + 4.7 | 1.8 | 90 | 100 | N/A | N/A |
| ADP2106-1.5 | 1.5 | 4.7 | 10 | 10 + 10 | 2.0 | 90 | 100 | N/A | N/A |
| ADP2106-1.8 | 1.8 | 4.7 | 10 | 10 + 10 | 2.2 | 90 | 100 | N/A | N/A |
| ADP2106-3.3 | 3.3 | 4.7 | 10 | 10 + 4.7 | 3.0 | 90 | 100 | N/A | N/A |
| ADP2107-1.2 | 1.2 | 10 | 10 | 22 + 4.7 | 1.5 | 70 | 120 | N/A | N/A |
| ADP2107-1.5 | 1.5 | 10 | 10 | 10 + 10 | 1.5 | 70 | 120 | N/A | N/A |
| ADP2107-1.8 | 1.8 | 10 | 10 | 10 + 10 | 1.8 | 70 | 120 | N/A | N/A |
| ADP2107-3.3 | 3.3 | 10 | 10 | 10 + 4.7 | 2.5 | 70 | 120 | N/A | N/A |

[1] 4.7 µF 0805 X5R 10 V Murata—GRM21BR61A475KA73L. 10 µF 0805 X5R 10 V Murata—GRM21BR61A106KE19L.
[2] 4.7 µF 0805 X5R 10 V Murata—GRM21BR61A475KA73L. 10 µF 0805 X5R 10 V Murata—GRM21BR61A106KE19L. 22 µF 0805 X5R 6.3 V Murata—GRM21BR60J226ME39L.
[3] 0.5% accuracy resistor.

For popular output voltage options at 80 kHz crossover frequency with 5% overshoot for a 1 A load transient (refer to Figure 37 and Figure 38).

**Table 12. Recommended External Components**

| Device | $V_{OUT}$ (V) | $C_{IN1}$[1] (µF) | $C_{IN2}$[1] (µF) | $C_{OUT}$[2] (µF) | L (µH) | $R_{COMP}$ (kΩ) | $C_{COMP}$ (pF) | $R_{TOP}$[3] (kΩ) | $R_{BOT}$[3] (kΩ) |
|---|---|---|---|---|---|---|---|---|---|
| ADP2105 (ADJ) | 0.9 | 4.7 | 4.7 | 22 + 22 + 22 | 2.0 | 270 | 39 | 5 | 40 |
| ADP2105 (ADJ) | 1.2 | 4.7 | 4.7 | 22 + 22 + 4.7 | 2.5 | 270 | 39 | 20 | 40 |
| ADP2105 (ADJ) | 1.5 | 4.7 | 4.7 | 22 + 22 | 3.0 | 270 | 39 | 35 | 40 |
| ADP2105 (ADJ) | 1.8 | 4.7 | 4.7 | 22 + 22 | 3.3 | 270 | 39 | 50 | 40 |
| ADP2105 (ADJ) | 2.5 | 4.7 | 4.7 | 22 + 10 | 3.6 | 270 | 39 | 85 | 40 |
| ADP2105 (ADJ) | 3.3 | 4.7 | 4.7 | 22 + 4.7 | 4.1 | 270 | 39 | 125 | 40 |
| ADP2106 (ADJ) | 0.9 | 4.7 | 10 | 22 + 22 + 22 | 1.5 | 180 | 56 | 5 | 40 |
| ADP2106 (ADJ) | 1.2 | 4.7 | 10 | 22 + 22 + 4.7 | 1.8 | 180 | 56 | 20 | 40 |
| ADP2106 (ADJ) | 1.5 | 4.7 | 10 | 22 + 22 | 2.0 | 180 | 56 | 35 | 40 |
| ADP2106 (ADJ) | 1.8 | 4.7 | 10 | 22 + 22 | 2.2 | 180 | 56 | 50 | 40 |
| ADP2106 (ADJ) | 2.5 | 4.7 | 10 | 22 + 10 | 2.5 | 180 | 56 | 85 | 40 |
| ADP2106 (ADJ) | 3.3 | 4.7 | 10 | 22 + 4.7 | 3.0 | 180 | 56 | 125 | 40 |
| ADP2107 (ADJ) | 0.9 | 10 | 10 | 22 + 22 + 22 | 1.2 | 140 | 68 | 5 | 40 |
| ADP2107 (ADJ) | 1.2 | 10 | 10 | 22 + 22 + 4.7 | 1.5 | 140 | 68 | 20 | 40 |
| ADP2107 (ADJ) | 1.5 | 10 | 10 | 22 + 22 | 1.5 | 140 | 68 | 35 | 40 |
| ADP2107 (ADJ) | 1.8 | 10 | 10 | 22 + 22 | 1.8 | 140 | 68 | 50 | 40 |
| ADP2107 (ADJ) | 2.5 | 10 | 10 | 22 + 10 | 1.8 | 140 | 68 | 85 | 40 |
| ADP2107 (ADJ) | 3.3 | 10 | 10 | 22 + 4.7 | 2.5 | 140 | 68 | 125 | 40 |
| ADP2105-1.2 | 1.2 | 4.7 | 4.7 | 22 + 22 + 4.7 | 2.5 | 270 | 39 | N/A | N/A |
| ADP2105-1.5 | 1.5 | 4.7 | 4.7 | 22 + 22 | 3.0 | 270 | 39 | N/A | N/A |
| ADP2105-1.8 | 1.8 | 4.7 | 4.7 | 22 + 22 | 3.3 | 270 | 39 | N/A | N/A |
| ADP2105-3.3 | 3.3 | 4.7 | 4.7 | 22 + 4.7 | 4.1 | 270 | 39 | N/A | N/A |
| ADP2106-1.2 | 1.2 | 4.7 | 10 | 22 + 22 + 4.7 | 1.8 | 180 | 56 | N/A | N/A |
| ADP2106-1.5 | 1.5 | 4.7 | 10 | 22 + 22 | 2.0 | 180 | 56 | N/A | N/A |
| ADP2106-1.8 | 1.8 | 4.7 | 10 | 22 + 22 | 2.2 | 180 | 56 | N/A | N/A |
| ADP2106-3.3 | 3.3 | 4.7 | 10 | 22 + 4.7 | 3.0 | 180 | 56 | N/A | N/A |
| ADP2107-1.2 | 1.2 | 10 | 10 | 22 + 22 + 4.7 | 1.5 | 140 | 68 | N/A | N/A |
| ADP2107-1.5 | 1.5 | 10 | 10 | 22 + 22 | 1.5 | 140 | 68 | N/A | N/A |
| ADP2107-1.8 | 1.8 | 10 | 10 | 22 + 22 | 1.8 | 140 | 68 | N/A | N/A |
| ADP2107-3.3 | 3.3 | 10 | 10 | 22 + 4.7 | 2.5 | 140 | 68 | N/A | N/A |

[1] 4.7µF 0805 X5R 10V Murata—GRM21BR61A475KA73L. 10µF 0805 X5R 10V Murata—GRM21BR61A106KE19L.
[2] 4.7µF 0805 X5R 10V Murata—GRM21BR61A475KA73L. 10µF 0805 X5R 10V Murata—GRM21BR61A106KE19L. 22µF 0805 X5R 6.3V Murata—GRM21BR60J226ME39L.
[3] 0.5% accuracy resistor.

# CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential to obtaining the best performance from the ADP2105/ADP2106/ADP2107. Poor circuit layout degrades the output ripple, as well as the electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance.

Figure 54 and Figure 55 show the ideal circuit board layout for the ADP2105/ADP2106/ADP2107 to achieve the highest performance. Refer to the following guidelines if adjustments to the suggested layout are needed:

- Use separate analog and power ground planes. Connect the ground reference of sensitive analog circuitry (such as compensation and output voltage divider components) to analog ground; connect the ground reference of power components (such as input and output capacitors) to power ground. In addition, connect both the ground planes to the exposed pad of the ADP2105/ADP2106/ADP2107.
- For each PWIN pin, place an input capacitor as close to the PWIN pin as possible and connect the other end to the closest power ground plane.
- Place the 0.1 µF, 10 Ω low-pass input filter between the IN pin and the PWIN1 pin, as close to the IN pin as possible.
- Ensure that the high current loops are as short and as wide as possible. Make the high current path from $C_{IN}$ through L, $C_{OUT}$, and the PGND plane back to $C_{IN}$ as short as possible. To accomplish this, ensure that the input and output capacitors share a common PGND plane.
- Make the high current path from the PGND pin through L and $C_{OUT}$ back to the PGND plane as short as possible. To accomplish this, ensure that the PGND pin is tied to the PGND plane as close as possible to the input and output capacitors.
- The feedback resistor divider network is to be placed as close as possible to the FB pin to prevent noise pickup. The length of trace connecting the top of the feedback resistor divider to the output is to be as short as possible while keeping away from the high current traces and the LX (switch) node that can lead to noise pickup. An analog ground plane is to be placed on either side of the FB trace to reduce noise pickup. For the low fixed voltage options (1.2 V and 1.5 V), poor routing of the OUT_SENSE trace can lead to noise pickup, adversely affecting load regulation. This can be fixed by placing a 1 nF bypass capacitor close to the FB pin.
- The placement and routing of the compensation components are critical for proper behavior of the ADP2105/ADP2106/ADP2107. The compensation components are to be placed as close to the COMP pin as possible. It is advisable to use 0402-sized compensation components for closer placement, leading to smaller parasitics. Surround the compensation components with an analog ground plane to prevent noise pickup. The metal layer under the compensation components is to be the analog ground plane.

# EVALUATION BOARD

## EVALUATION BOARD SCHEMATIC FOR ADP2107 (1.8 V)

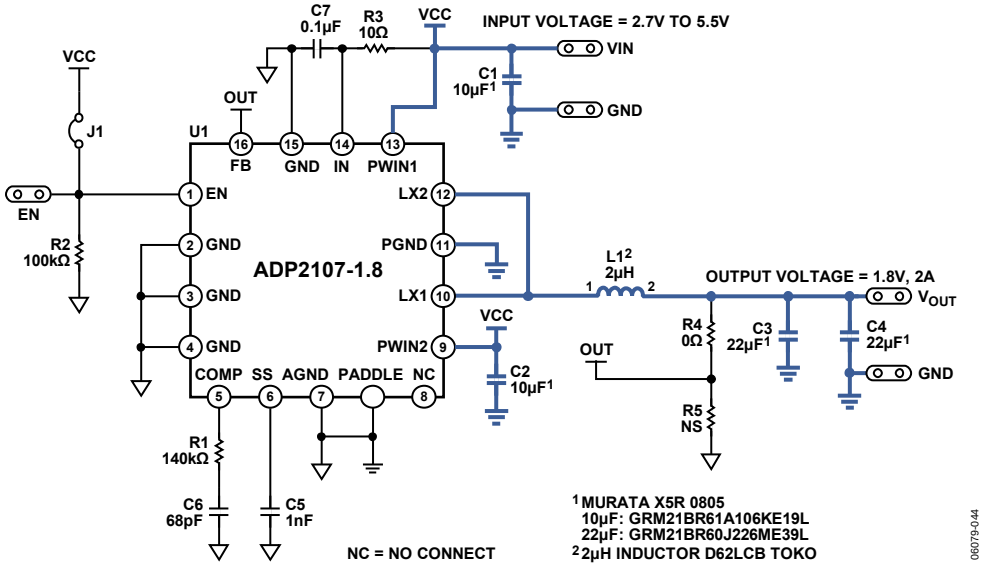



*Figure 53. Evaluation Board Schematic of the ADP2107-1.8 (Bold Traces are High Current Paths)*

## RECOMMENDED PCB LAYOUT (EVALUATION BOARD LAYOUT)

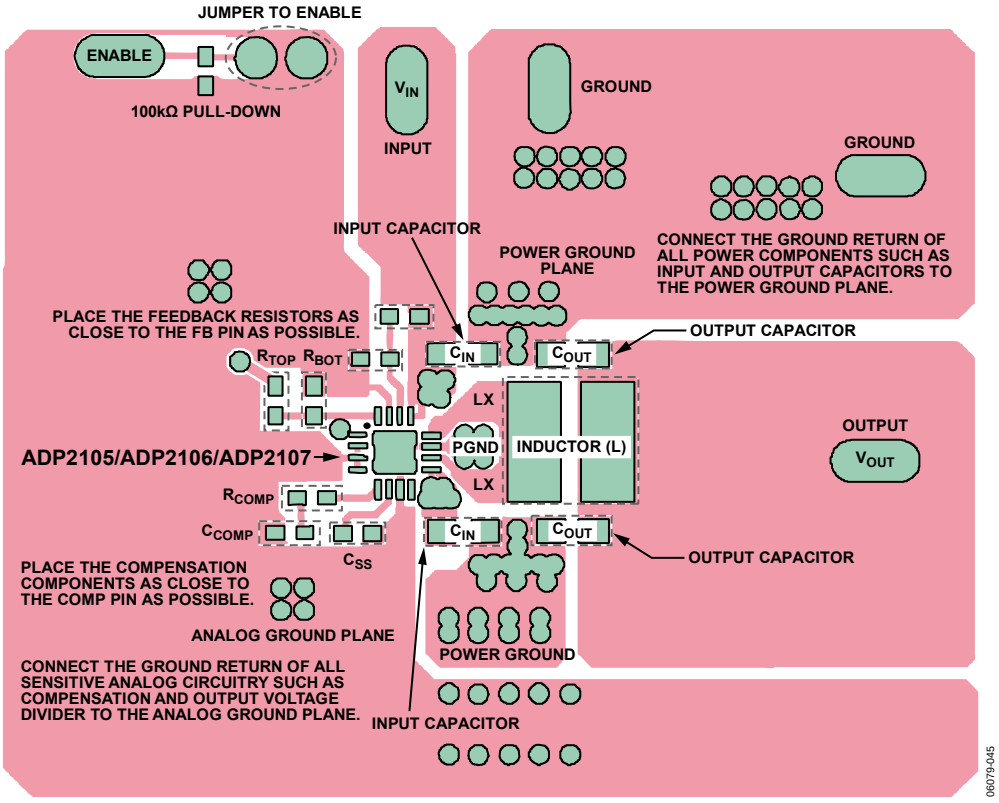



*Figure 54. Recommended Layout of Top Layer of ADP2105/ADP2106/ADP2107*

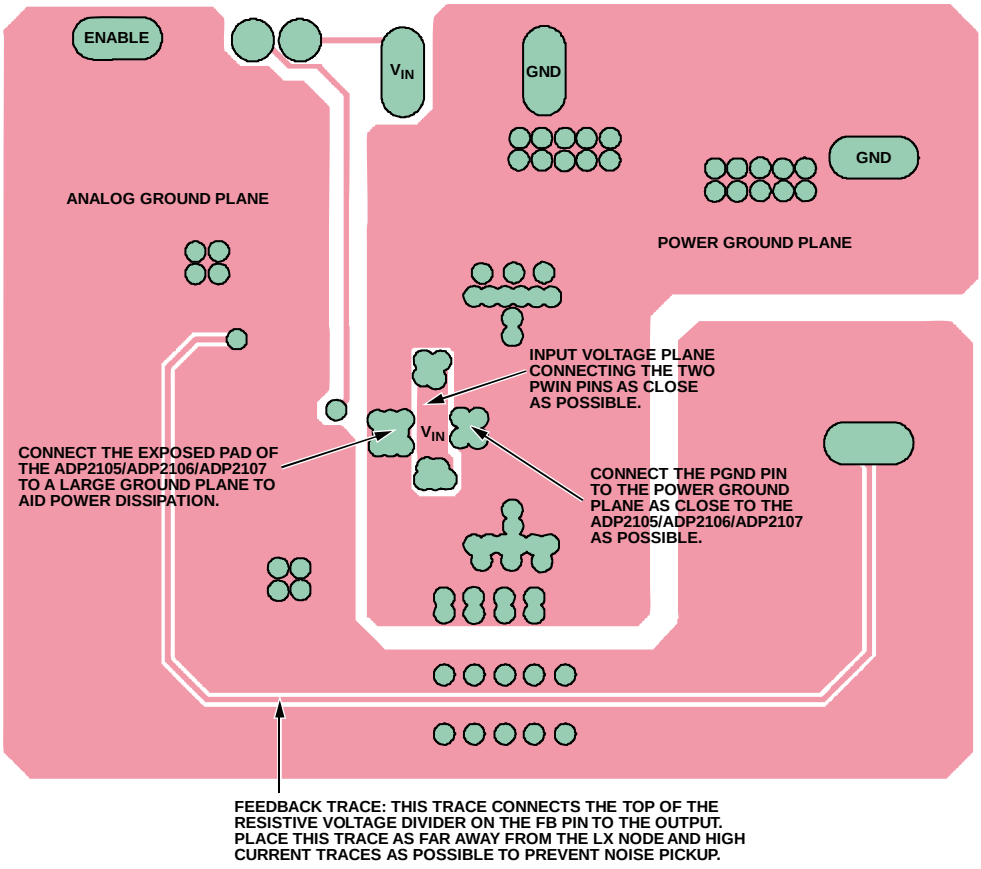



*Figure 55. Recommended Layout of Bottom Layer of ADP2105/ADP2106/ADP2107*

# APPLICATION CIRCUITS

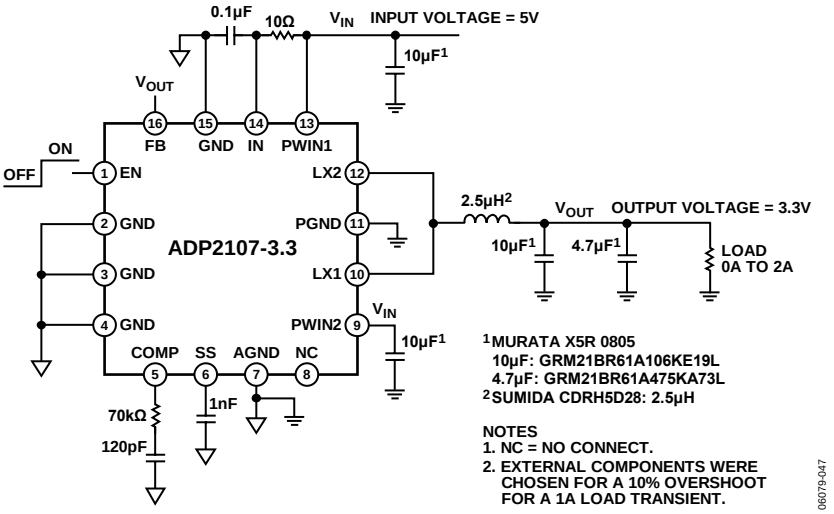



*Figure 56. Application Circuit—$V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, Load = 0 A to 2 A*

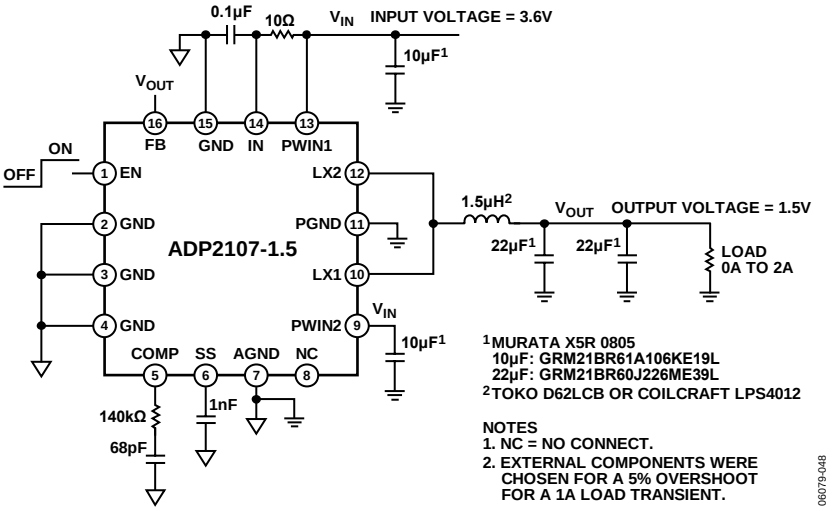



*Figure 57. Application Circuit—$V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.5 V, Load = 0 A to 2 A*

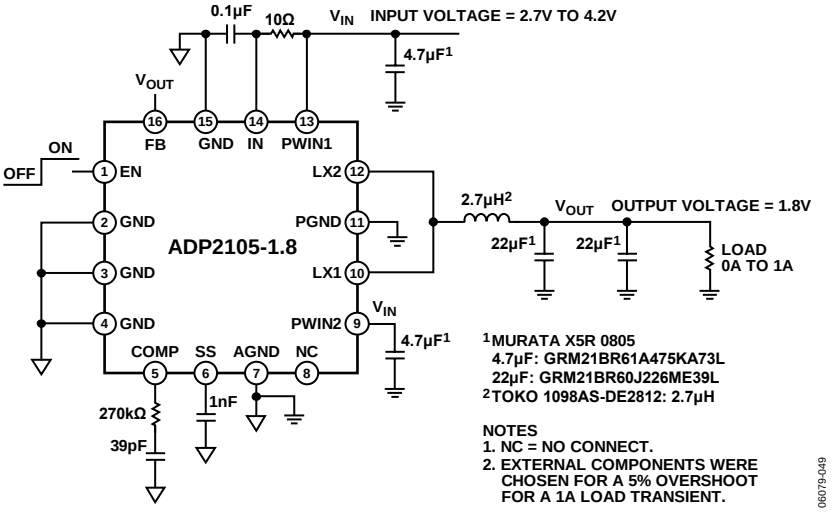



*Figure 58. Application Circuit—$V_{IN}$ = Li-Ion Battery, $V_{OUT}$ = 1.8 V, Load = 0 A to 1 A*

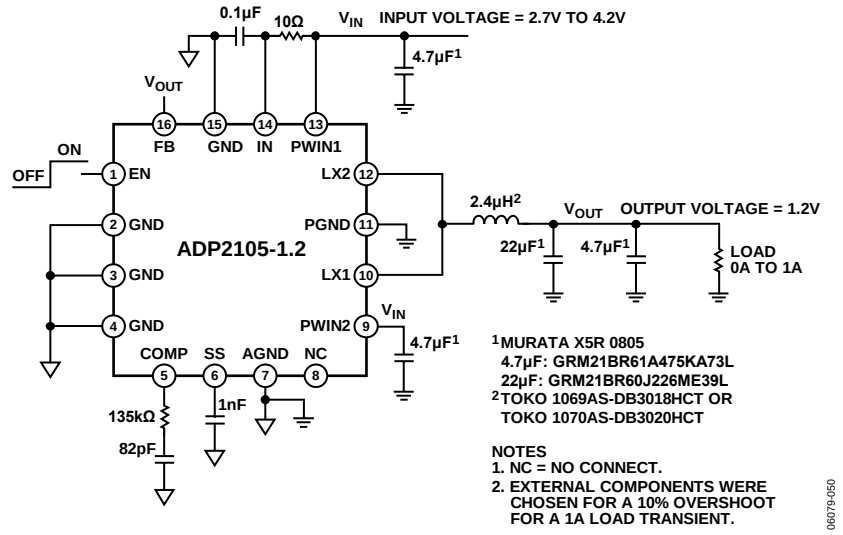



*Figure 59. Application Circuit—$V_{IN}$ = Li-Ion Battery, $V_{OUT}$ = 1.2 V, Load = 0 A to 1 A*

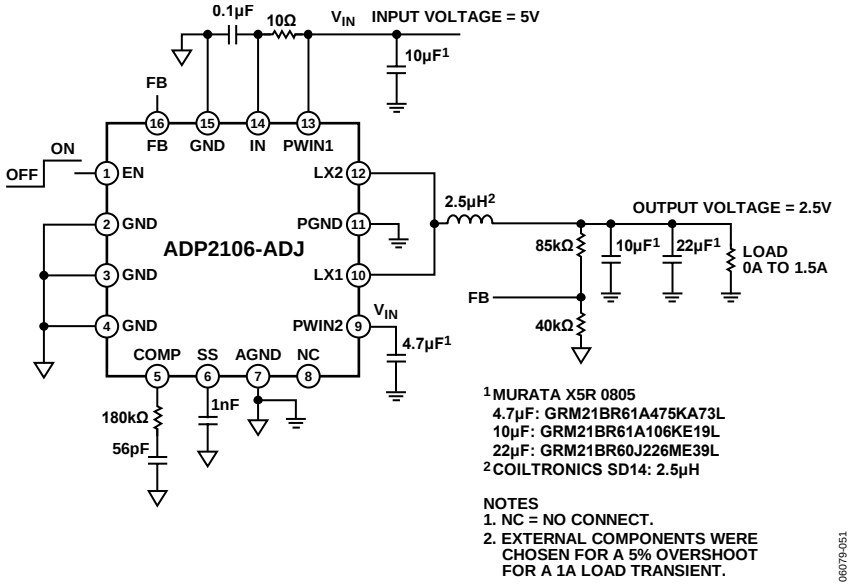



*Figure 60. Application Circuit—$V_{IN}$ = 5 V, $V_{OUT}$ = 2.5 V, Load = 0 A to 1.5 A*

# OUTLINE DIMENSIONS

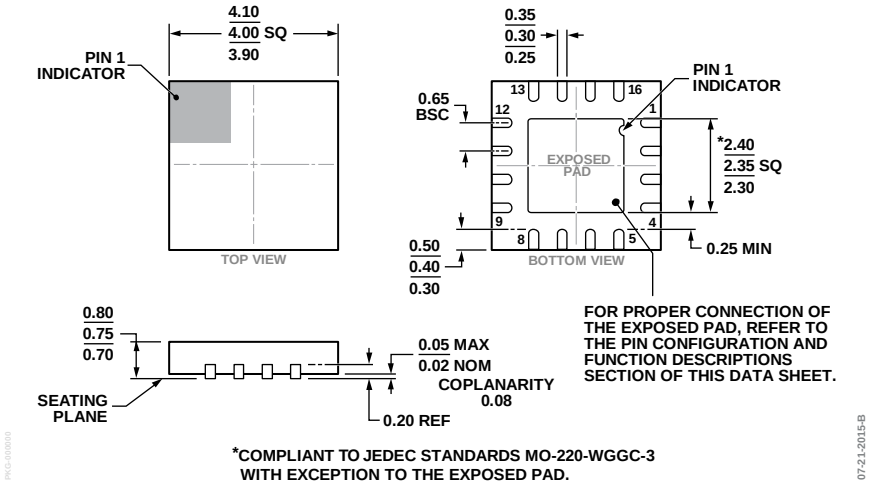



*Figure 61. 16-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm × 4 mm Body and 0.75 mm Package Height*
*(CP-16-20)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Output Current | Temperature Range | Output Voltage | Package Description | Package Option |
|---|---|---|---|---|---|
| ADP2105ACPZ-1.2-R7 | 1 A | −40°C to +125°C | 1.2 V | 16-Lead LFCSP | CP-16-20 |
| ADP2105ACPZ-1.5-R7 | 1 A | −40°C to +125°C | 1.5 V | 16-Lead LFCSP | CP-16-20 |
| ADP2105ACPZ-1.8-R7 | 1 A | −40°C to +125°C | 1.8 V | 16-Lead LFCSP | CP-16-20 |
| ADP2105ACPZ-3.3-R7 | 1 A | −40°C to +125°C | 3.3 V | 16-Lead LFCSP | CP-16-20 |
| ADP2105ACPZ-R7 | 1 A | −40°C to +125°C | ADJ | 16-Lead LFCSP | CP-16-20 |
| ADP2106ACPZ-1.2-R7 | 1.5 A | −40°C to +125°C | 1.2 V | 16-Lead LFCSP | CP-16-20 |
| ADP2106ACPZ-1.5-R7 | 1.5 A | −40°C to +125°C | 1.5 V | 16-Lead LFCSP | CP-16-20 |
| ADP2106ACPZ-1.8-R7 | 1.5 A | −40°C to +125°C | 1.8 V | 16-Lead LFCSP | CP-16-20 |
| ADP2106ACPZ-3.3-R7 | 1.5 A | −40°C to +125°C | 3.3 V | 16-Lead LFCSP | CP-16-20 |
| ADP2106ACPZ-R7 | 1.5 A | −40°C to +125°C | ADJ | 16-Lead LFCSP | CP-16-20 |
| ADP2107ACPZ-1.2-R7 | 2 A | −40°C to +125°C | 1.2 V | 16-Lead LFCSP | CP-16-20 |
| ADP2107ACPZ-1.5-R7 | 2 A | −40°C to +125°C | 1.5 V | 16-Lead LFCSP | CP-16-20 |
| ADP2107ACPZ-1.8-R7 | 2 A | −40°C to +125°C | 1.8 V | 16-Lead LFCSP | CP-16-20 |
| ADP2107ACPZ-3.3-R7 | 2 A | −40°C to +125°C | 3.3 V | 16-Lead LFCSP | CP-16-20 |
| ADP2107ACPZ-R7 | 2 A | −40°C to +125°C | ADJ | 16-Lead LFCSP | CP-16-20 |
| ADP2105-1.8-EVALZ | | | 1.8 V | Evaluation Board | |
| ADP2105-EVALZ | | | Adjustable, but set to 2.5 V | Evaluation Board | |
| ADP2106-1.8-EVALZ | | | 1.8 V | Evaluation Board | |
| ADP2106-EVALZ | | | Adjustable, but set to 2.5 V | Evaluation Board | |
| ADP2107-1.8-EVALZ | | | 1.8 V | Evaluation Board | |
| ADP2107-EVALZ | | | Adjustable, but set to 2.5 V | Evaluation Board | |

[1] Z = RoHS Compliant Part.

## NOTES

## NOTES


D06079-0-3/16(E)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADP2106-EVALZ ADP2105-1.8-EVALZ ADP2106-1.8-EVALZ ADP2107ACPZ-3.3-R7 ADP2105ACPZ-1.8-R7 ADP2106ACPZ-R7 ADP2105-EVALZ ADP2107ACPZ-R7 ADP2107ACPZ-1.5-R7 ADP2107ACPZ-1.8-R7 ADP2107ACPZ-1.2-R7 ADP2106ACPZ-3.3-R7 ADP2105ACPZ-R7 ADP2105ACPZ-1.2-R7 ADP2107-1.8-EVALZ ADP2105ACPZ-3.3-R7 ADP2106ACPZ-1.8-R7 ADP2107-EVALZ