



## Features

- Very high speed
  - 55 ns
- Wide voltage range
  - 2.2 V to 3.7 V
- Ultra low standby power
  - Typical standby current: 8  $\mu$ A
  - Maximum standby current: 48  $\mu$ A
- Ultra low active power
  - Typical active current: 7.5 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 48-ball FBGA package

## Functional Description

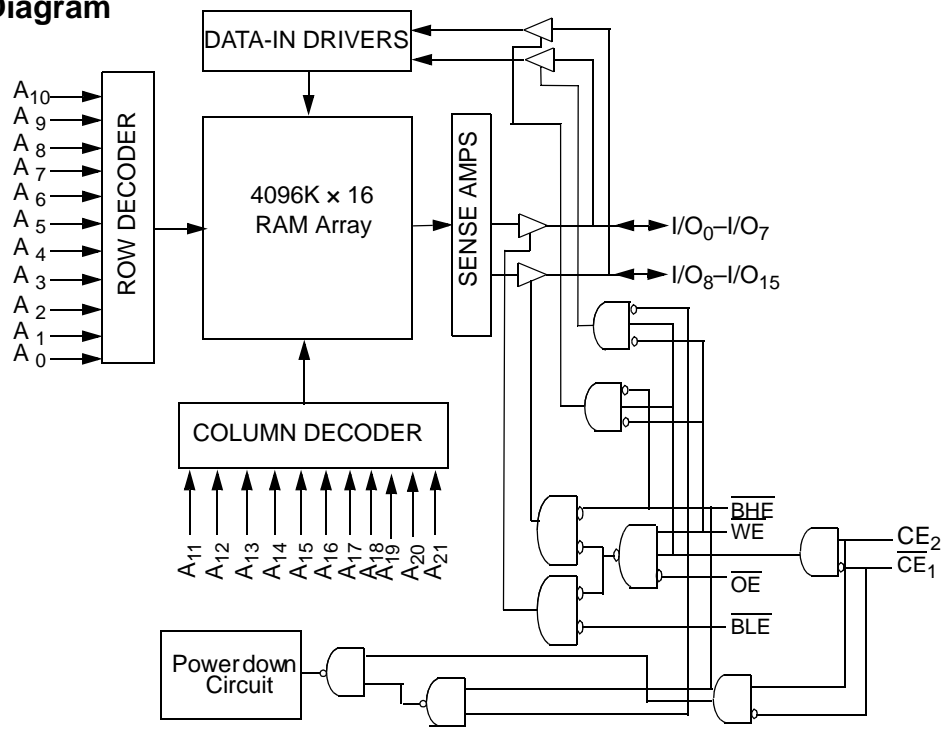
The CY62187EV30 is a high performance CMOS static RAM organized as 4 M words by 16-bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input and output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH and  $\overline{WE}$  LOW).

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{21}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{21}$ ).

To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See the [Truth Table](#) on page 9 for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

**Logic Block Diagram**

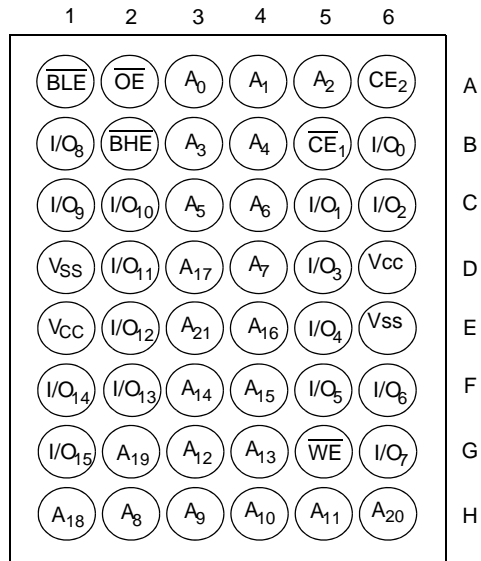


## Contents

<b>Pin Configuration</b> .....	<b>4</b>	<b>Ordering Information</b> .....	<b>13</b>
<b>Product Portfolio</b> .....	<b>4</b>	Ordering Code Definitions .....	13
<b>Maximum Ratings</b> .....	<b>5</b>	<b>Package Diagram</b> .....	<b>14</b>
<b>Operating Range</b> .....	<b>5</b>	<b>Acronyms</b> .....	<b>15</b>
<b>Electrical Characteristics</b> .....	<b>5</b>	<b>Document Conventions</b> .....	<b>15</b>
<b>Capacitance</b> .....	<b>6</b>	Units of Measure .....	15
<b>Thermal Resistance</b> .....	<b>6</b>	<b>Document History Page</b> .....	<b>16</b>
<b>AC Test Loads and Waveforms</b> .....	<b>6</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>19</b>
<b>Data Retention Characteristics</b> .....	<b>7</b>	Worldwide Sales and Design Support .....	19
<b>Data Retention Waveform</b> .....	<b>7</b>	Products .....	19
<b>Switching Characteristics</b> .....	<b>8</b>	PSoC <sup>®</sup> Solutions .....	19
<b>Switching Waveforms</b> .....	<b>9</b>	Cypress Developer Community .....	19
<b>Truth Table</b> .....	<b>12</b>	Technical Support .....	19

## Pin Configuration

Figure 1. 48-ball FBGA pinout



## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1 MHz		f = f <sub>Max</sub>			
Min	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max		
CY62187EV30LL	2.2	3.0	3.7	55	7.5	9	45	55	8	48

### Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....	-65 °C to +150 °C
Ambient Temperature with Power Applied .....	-55 °C to +125 °C
Supply Voltage to Ground Potential .....	-0.3 V to $V_{CC(max)} + 0.3$ V
DC Voltage Applied to Outputs in High Z State <sup>[2, 3]</sup> .....	-0.3 V to $V_{CC(max)} + 0.3$ V

DC Input Voltage <sup>[2, 3]</sup> .....	-0.3 V to $V_{CC(max)} + 0.3$ V
Output Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015) .....	> 2001 V
Latch Up Current .....	> 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[4]</sup>
CY62187EV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.7 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	55 ns			Unit
			Min	Typ <sup>[5]</sup>	Max	
V <sub>OH</sub>	Output HIGH voltage	2.2 V ≤ V <sub>CC</sub> ≤ 2.7 V   I <sub>OH</sub> = -0.1 mA	2.0	-	-	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.7 V   I <sub>OH</sub> = -1.0 mA	2.4	-	-	V
V <sub>OL</sub>	Output LOW voltage	2.2 V ≤ V <sub>CC</sub> ≤ 2.7 V   I <sub>OL</sub> = 0.1 mA	-	-	0.4	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.7 V   I <sub>OL</sub> = 2.1 mA	-	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage	2.2 V ≤ V <sub>CC</sub> ≤ 2.7 V	1.8	-	V <sub>CC</sub> + 0.3 V	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.7 V	2.2	-	V <sub>CC</sub> + 0.3 V	V
V <sub>IL</sub>	Input LOW voltage	2.2 V ≤ V <sub>CC</sub> ≤ 2.7 V	-0.3	-	0.6	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.7 V	-0.3	-	0.8 <sup>[6]</sup>	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled	-1	-	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = f <sub>Max</sub> = 1/t <sub>RC</sub>   V <sub>CC</sub> = V <sub>CC(max)</sub> I <sub>OUT</sub> = 0 mA CMOS levels	-	45	55	mA
		f = 1 MHz	-	7.5	9	mA
I <sub>SB2</sub> <sup>[7]</sup>	Automatic CE power down current — CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or (BHE and BLE) ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0, V <sub>CC</sub> = 3.7 V	-	8	48	μA

### Notes

- V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub> (min) and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
- Under DC conditions the device meets a V<sub>IL</sub> of 0.8 V. However, in dynamic conditions input LOW Voltage applied to the device must not be higher than 0.7 V.
- Chip enables (CE<sub>1</sub> and CE<sub>2</sub>), Address Pins A<sub>20</sub>, A<sub>21</sub> and Byte Enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

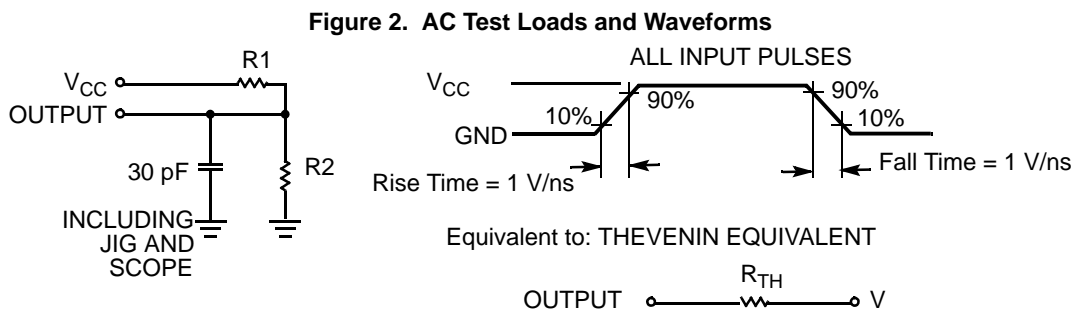
### Capacitance

Parameter <sup>[8]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	25	pF
C <sub>OUT</sub>	Output capacitance		35	pF

### Thermal Resistance

Parameter <sup>[8]</sup>	Description	Test Conditions	FBGA	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	42.35	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		6.25	°C/W

### AC Test Loads and Waveforms



**Table 1. AC Test Loads**

Parameter	2.5 V	3.3 V	Unit
R <sub>1</sub>	16667	1103	Ω
R <sub>2</sub>	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

**Note**

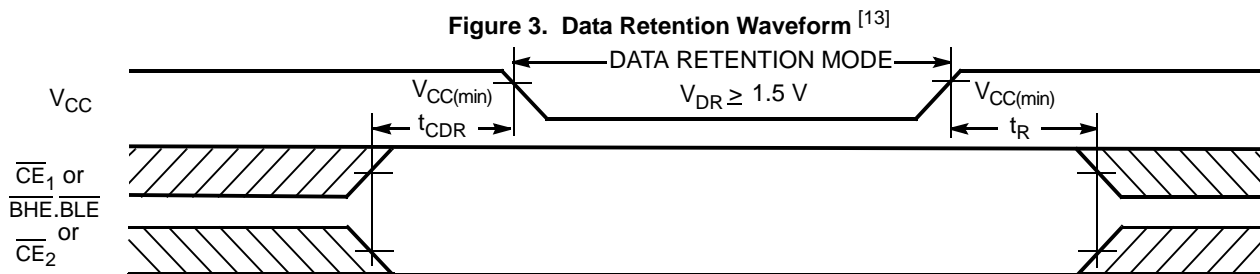
8. Tested initially and after any design or process changes that may affect these parameters.

## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[9]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		1.5	–	–	V
I <sub>CCDR</sub> <sup>[10]</sup>	Data retention current	V <sub>CC</sub> = 1.5 V, CE <sub>1</sub> ≥ V <sub>CC</sub> – 0.2 V or CE <sub>2</sub> ≤ 0.2 V or (BHE and BLE) ≥ V <sub>CC</sub> – 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V or V <sub>IN</sub> ≤ 0.2 V	–	–	48	μA
t <sub>CDR</sub> <sup>[11]</sup>	Chip deselect to data retention time		0	–	–	ns
t <sub>R</sub> <sup>[12]</sup>	Operation recovery time		55	–	–	ns

## Data Retention Waveform



### Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
10. Chip enables ( $\overline{CE}_1$  and CE<sub>2</sub>), Address Pins A<sub>20</sub>, A<sub>21</sub> and Byte Enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB2</sub>/I<sub>CCDR</sub> spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.
13. BHE.BLE is the AND of both BHE and BLE. Chip is deselected by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	55 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	55	–	ns
$t_{AA}$	Address to data valid	–	55	ns
$t_{OHA}$	Data hold from address change	6	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to LOW Z <sup>[16]</sup>	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[16, 17]</sup>	–	20	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to low Z <sup>[16]</sup>	10	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to high Z <sup>[16, 17]</sup>	–	20	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to power up	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to power down	–	55	ns
$t_{DBE}$	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	55	ns
$t_{LZBE}$	$\overline{BLE}/\overline{BHE}$ LOW to low Z <sup>[16]</sup>	10	–	ns
$t_{HZBE}$	$\overline{BLE}/\overline{BHE}$ HIGH to high Z <sup>[16, 17]</sup>	–	20	ns
<b>Write Cycle<sup>[18, 19]</sup></b>				
$t_{WC}$	Write cycle time	55	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to write end	45	–	ns
$t_{AW}$	Address setup to write end	45	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	40	–	ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to write end	45	–	ns
$t_{SD}$	Data setup to write end	25	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[16, 17]</sup>	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[16]</sup>	10	–	ns

### Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of  $V_{TH}$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in Figure 2 on page 6.
16. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
18. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .



### Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled) [20, 21]

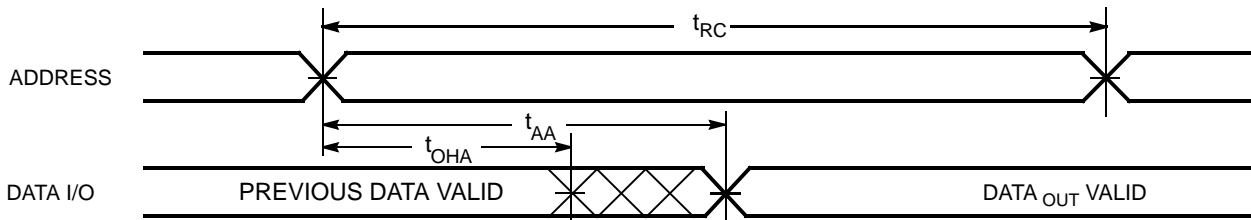
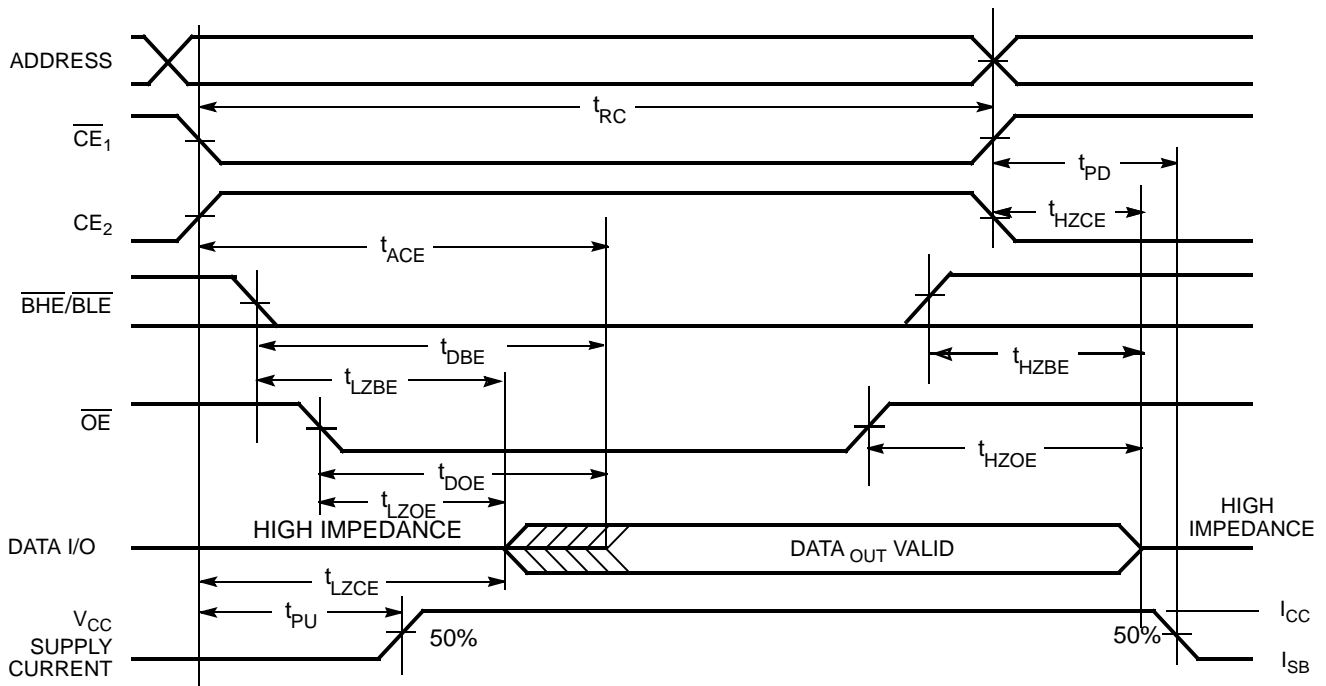


Figure 5. Read Cycle 2 ( $\overline{OE}$  Controlled) [21, 22]



**Notes**

- 20. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ .
- 21.  $\overline{WE}$  is HIGH for read cycle.
- 22. Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle 1 ( $\overline{WE}$  Controlled) [23, 24, 25, 26]

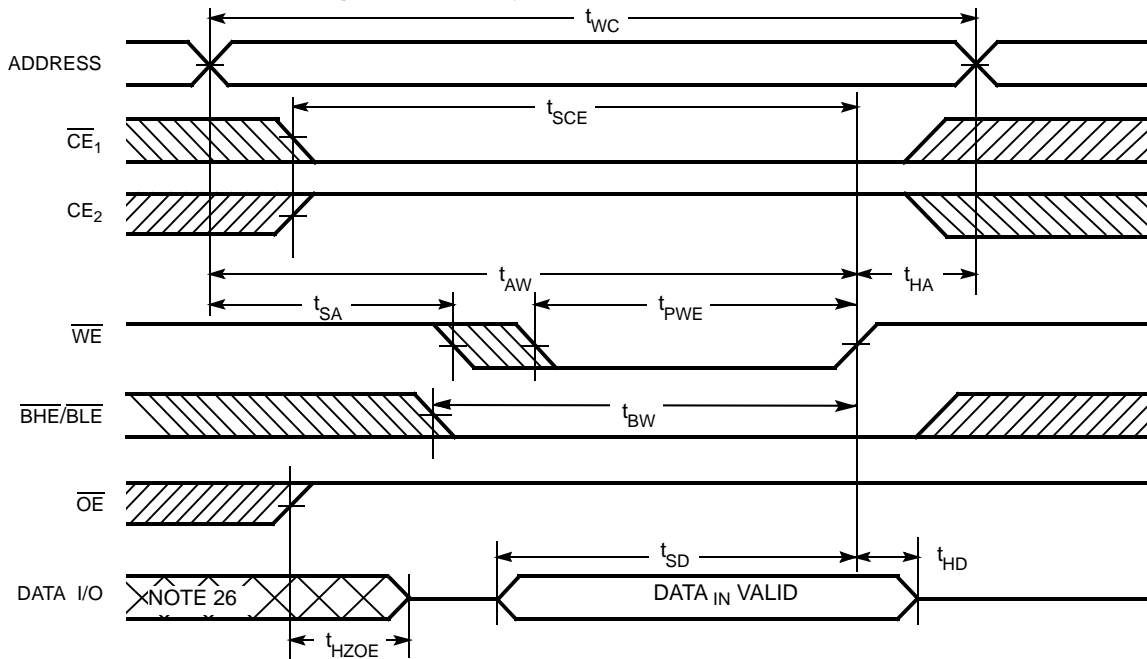
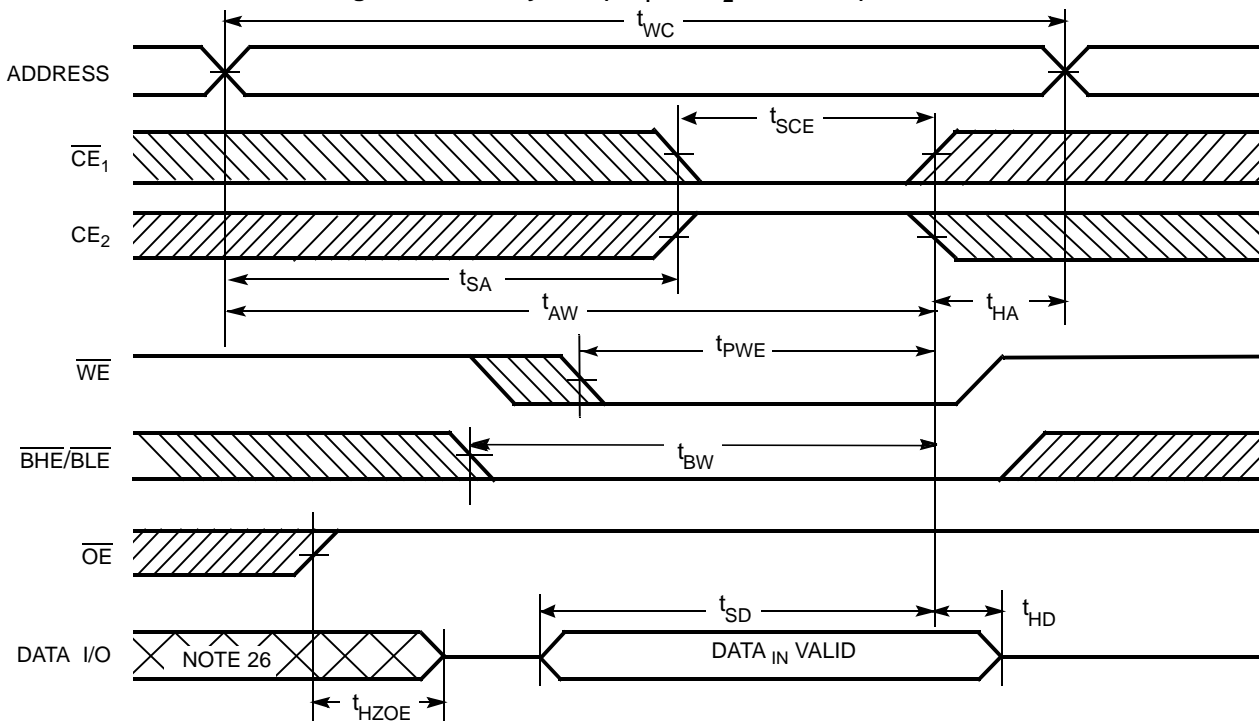


Figure 7. Write Cycle 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [23, 24, 25, 26]



Notes

23. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

24. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

25. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

26. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [27, 28, 29]

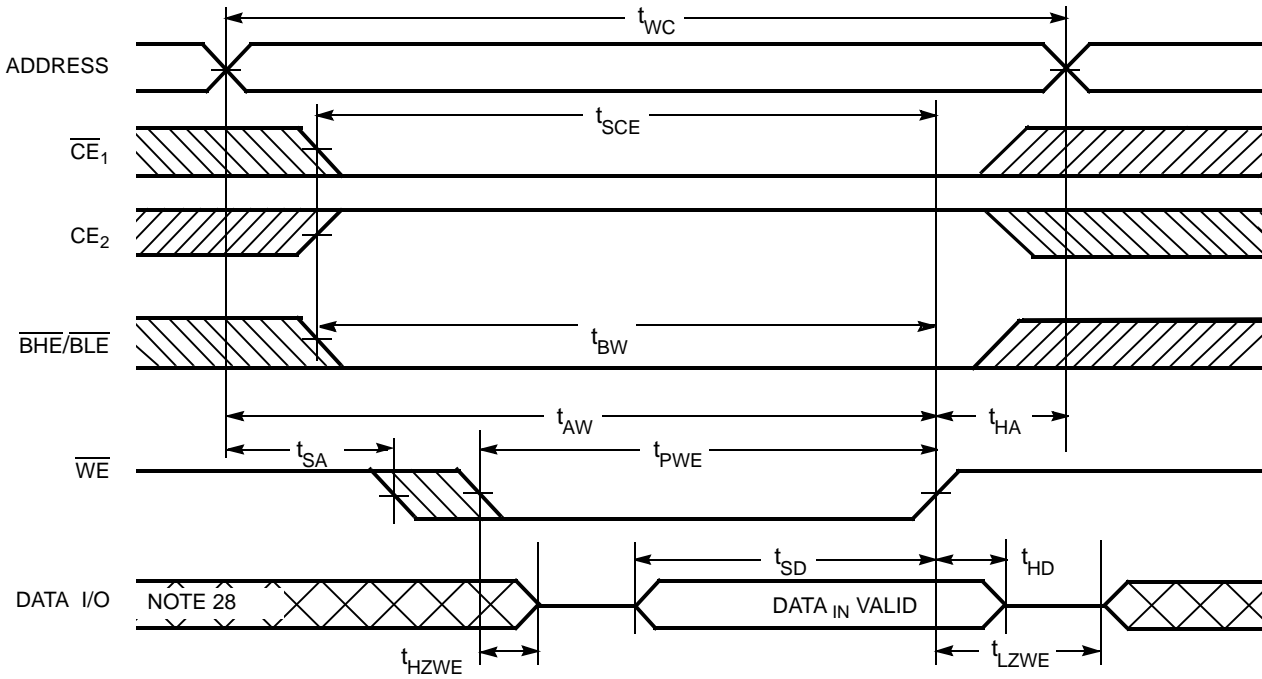
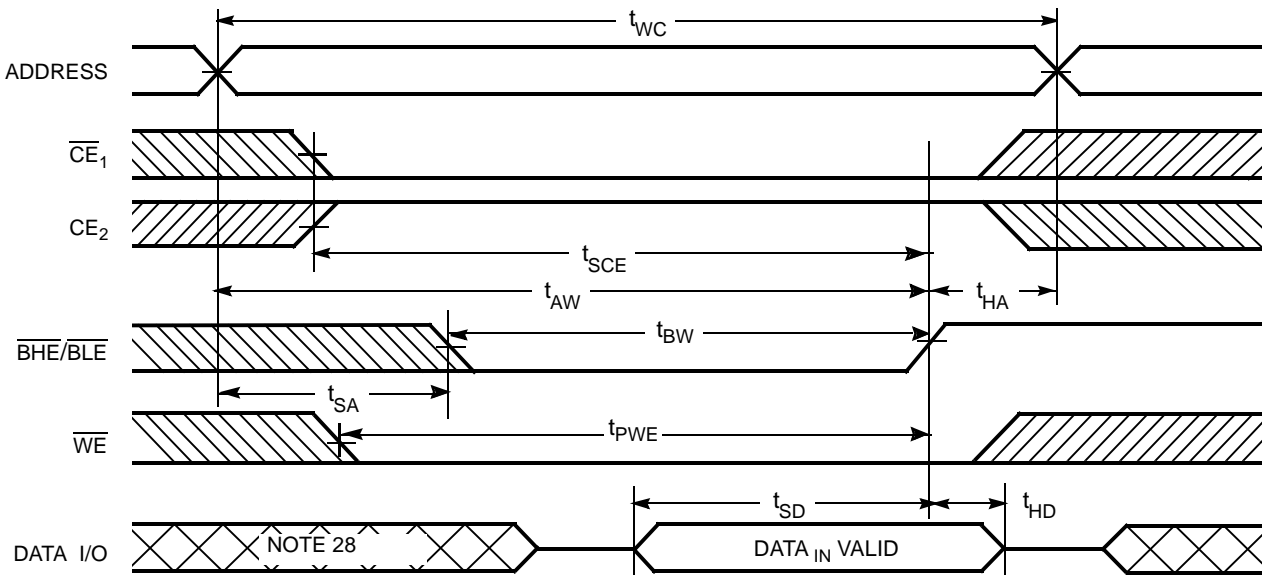


Figure 9. Write Cycle 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW) [27, 28]



Notes

- 27. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 28. During this period the I/Os are in output state and input signals should not be applied.
- 29. The minimum write cycle pulse width should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	$X^{[30]}$	X	X	$X^{[30]}$	$X^{[30]}$	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
$X^{[30]}$	L	X	X	$X^{[30]}$	$X^{[30]}$	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
$X^{[30]}$	$X^{[30]}$	X	X	H	H	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	High Z ( $I/O_8$ – $I/O_{15}$ ); Data Out ( $I/O_0$ – $I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); High Z ( $I/O_0$ – $I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	High Z ( $I/O_8$ – $I/O_{15}$ ); Data In ( $I/O_0$ – $I/O_7$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); High Z ( $I/O_0$ – $I/O_7$ )	Write	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )

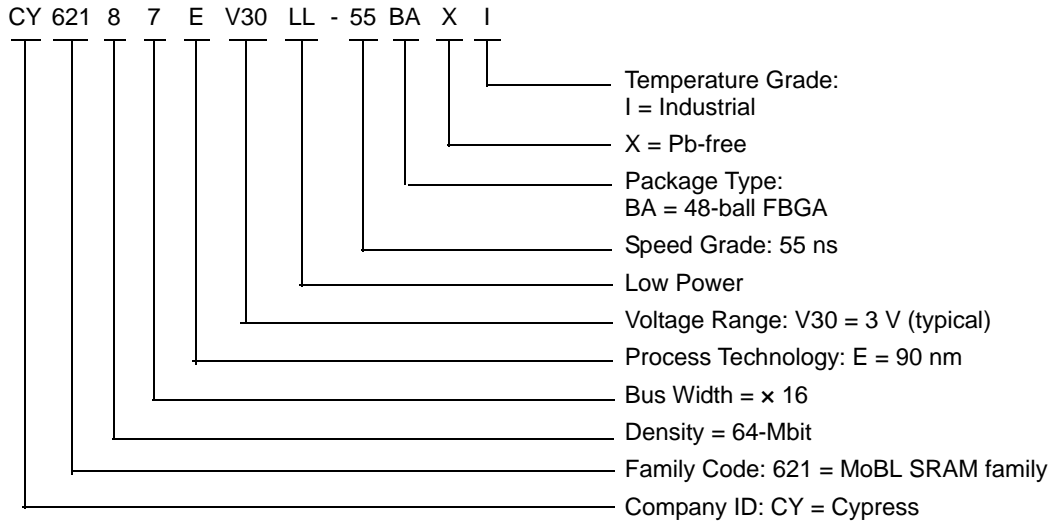
**Note**

30. The 'X' (Don't care) state for the chip enables and byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

### Ordering Information

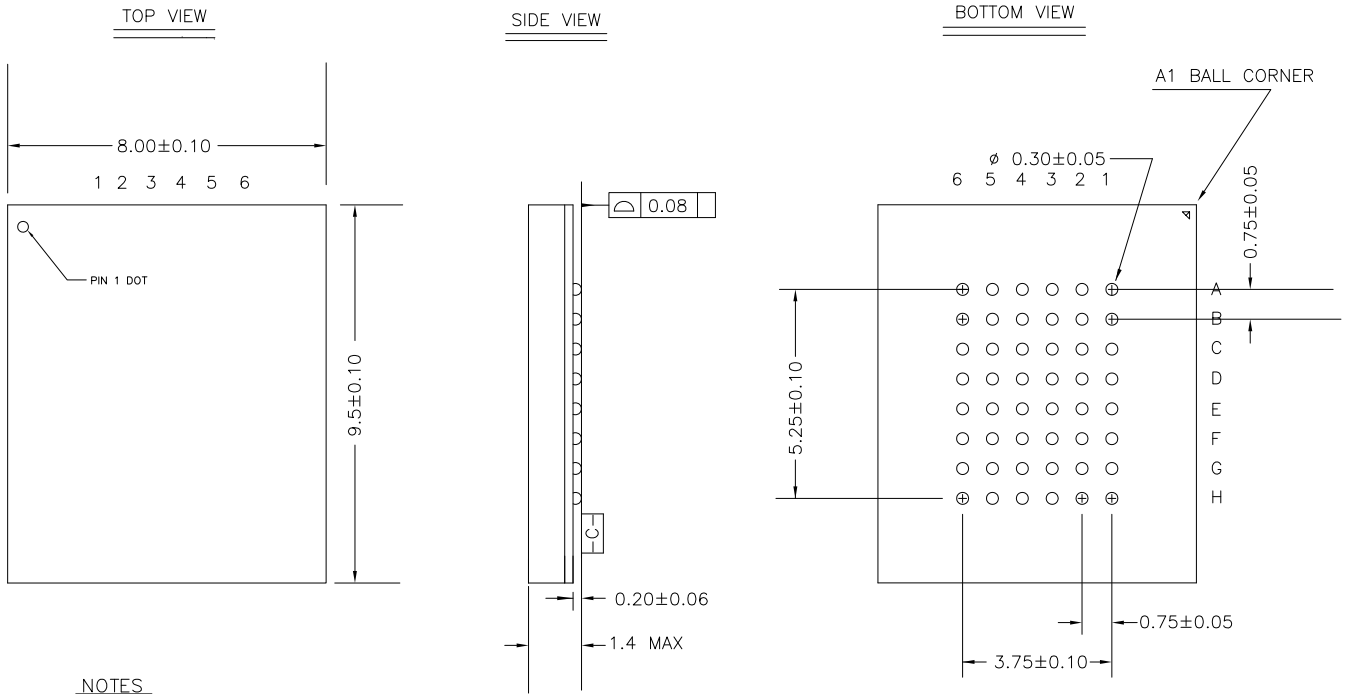
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62187EV30LL-55BAXI	001-50044	48-ball FBGA (8 × 9.5 × 1.4 mm) Pb-free	Industrial

### Ordering Code Definitions



**Package Diagram**

**Figure 10. 48-ball FBGA (8 × 9.5 × 1.4 mm) BK48L Package Outline, 001-50044**



NOTES

1. REFERENCE JEDEC # MO-205
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-50044 \*D

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohms
%	percent
pF	picofarad
V	volt
W	watt

**Document History Page**

Document Title: CY62187EV30 MoBL <sup>®</sup> , 64-Mbit (4 M × 16) Static RAM Document Number: 001-48998				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2595932	VKN / PYRS	10/24/08	New data sheet.
*A	2644442	VKN / PYRS	01/23/09	Updated <a href="#">Package Diagram</a> .
*B	2672650	VKN / PYRS	03/12/09	<p>Added 55 ns speed bin related information in all instances across the document.</p> <p>Updated <a href="#">Product Portfolio</a>:</p> <p>Changed maximum value in <math>V_{CC}</math> range from 3.6 V to 3.7 V.</p> <p>Changed typical value of "Operating <math>I_{CC}</math>" from 2.5 mA to 3.5 mA at <math>f = 1</math> MHz corresponding to 70 ns speed bin.</p> <p>Changed maximum value of "Operating <math>I_{CC}</math>" from 4 mA to 6 mA at <math>f = 1</math> MHz corresponding to 70 ns speed bin.</p> <p>Changed typical value of "Operating <math>I_{CC}</math>" from 33 mA to 28 mA at <math>f = f_{MAX}</math> corresponding to 70 ns speed bin.</p> <p>Changed maximum value of "Operating <math>I_{CC}</math>" from 40 mA to 45 mA at <math>f = f_{MAX}</math> corresponding to 70 ns speed bin.</p> <p>Updated <a href="#">Electrical Characteristics</a>:</p> <p>Changed typical value of <math>I_{CC}</math> parameter from 33 mA to 28 mA at <math>f = f_{MAX}</math> corresponding to 70 ns speed bin.</p> <p>Changed maximum value of <math>I_{CC}</math> parameter from 40 mA to 45 mA at <math>f = f_{MAX}</math> corresponding to 70 ns speed bin.</p> <p>Changed typical value of <math>I_{CC}</math> parameter from 2.5 mA to 3.5 mA at <math>f = 1</math> MHz corresponding to 70 ns speed bin.</p> <p>Changed maximum value of <math>I_{CC}</math> parameter from 4 mA to 6 mA at <math>f = 1</math> MHz corresponding to 70 ns speed bin.</p> <p>Updated Note 7.</p> <p>Updated <a href="#">Switching Characteristics</a>:</p> <p>Changed minimum value of <math>t_{PWE}</math> parameter from 45 ns to 50 ns corresponding to 70 ns speed bin.</p> <p>Changed minimum value of <math>t_{SD}</math> parameter from 30 ns to 35 ns corresponding to 70 ns speed bin.</p> <p>Updated <a href="#">Package Diagram</a>:</p> <p>Changed 48-ball FBGA package dimensions from "8 × 9.5 × 1.6 mm" to "8 × 9.5 × 1.4 mm".</p> <p>spec 001-50044 – Changed revision from ** to *A.</p>
*C	2737164	VKN / AESA	07/13/09	<p>Changed status from Preliminary to Final.</p> <p>Updated <a href="#">Product Portfolio</a>:</p> <p>Changed typical value of "Operating <math>I_{CC}</math>" from 3.5 mA to 4 mA at <math>f = 1</math> MHz corresponding to 55 ns and 70 ns speed bins.</p> <p>Changed typical value of "Operating <math>I_{CC}</math>" from 35 mA to 45 mA at <math>f = f_{max}</math> corresponding to 55 ns speed bin.</p> <p>Changed typical value of "Operating <math>I_{CC}</math>" from 28 mA to 35 mA at <math>f = f_{max}</math> corresponding to 70 ns speed bin.</p>



**Document History Page** *(continued)*

Document Title: CY62187EV30 MoBL <sup>®</sup> , 64-Mbit (4 M × 16) Static RAM Document Number: 001-48998				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*C (cont.)	2737164	VKN / AESA	07/13/09	<p>Updated <a href="#">Electrical Characteristics</a>: Updated details in "Test Conditions" column of <math>V_{OH}</math>, <math>V_{OL}</math>, <math>V_{IH}</math>, <math>V_{IL}</math> parameters (Included <math>V_{CC}</math> range). Changed maximum value of <math>V_{IL}</math> parameter from 0.8 V to 0.7 V corresponding to Test Condition "<math>V_{CC} = 2.7</math> V to 3.7 V". Changed typical value of <math>I_{CC}</math> parameter from 35 mA to 45 mA at <math>f = f_{max}</math> corresponding to 55 ns speed bin. Changed typical value of <math>I_{CC}</math> parameter from 28 mA to 35 mA at <math>f = f_{max}</math> corresponding to 70 ns speed bin. Changed typical value of <math>I_{CC}</math> parameter from 3.5 mA to 4 mA at <math>f = 1</math> MHz corresponding to 55 ns and 70 ns speed bins.</p> <p>Updated <a href="#">Capacitance</a>: Changed maximum value of <math>C_{IN}</math> parameter from 20 pF to 25 pF. Changed maximum value of <math>C_{OUT}</math> parameter from 20 pF to 35 pF.</p> <p>Updated <a href="#">Thermal Resistance</a>: Replaced TBD with values for 48-ball FBGA package.</p> <p>Updated <a href="#">AC Test Loads and Waveforms</a>: Updated <a href="#">Table 1</a>: Included <math>V_{CC}</math> range for <math>V_{TH}</math> parameter.</p> <p>Updated <a href="#">Switching Characteristics</a>: Changed minimum value of <math>t_{LZBE}</math> parameter from 5 ns to 10 ns.</p> <p>Updated <a href="#">Truth Table</a>: Added Note 30 and referred the same note in "X" in "<math>\overline{CE}_1</math>" and "<math>\overline{CE}_2</math>" columns.</p>
*D	2765892	VKN	09/18/09	<p>Removed 70 ns speed bin related information in all instances across the document.</p> <p>Updated <a href="#">Product Portfolio</a>: Changed maximum value of "Operating <math>I_{CC}</math>" from 6 mA to 9 mA at <math>f = 1</math> MHz corresponding to 55 ns speed bin.</p> <p>Updated <a href="#">Electrical Characteristics</a>: Changed typical value of <math>I_{CC}</math> parameter from 4 mA to 7.5 mA at <math>f = 1</math> MHz corresponding to 55 ns speed bin. Changed maximum value of <math>I_{CC}</math> parameter from 6 mA to 9 mA at <math>f = 1</math> MHz corresponding to 55 ns speed bin.</p>
*E	3177000	AJU	02/18/2011	<p>Updated <a href="#">Features</a>: Changed value of "Typical Active Current" from 4 mA to 7.5 mA.</p> <p>Updated <a href="#">Pin Configuration</a>: Fixed typo in <a href="#">Figure 1</a> (Renamed "48-Ball VFPGA" as "48-ball FBGA").</p> <p>Updated <a href="#">Product Portfolio</a>: Changed typical value of "Operating <math>I_{CC}</math>" from 4 mA to 7.5 mA at <math>f = 1</math> MHz corresponding to 55 ns speed bin.</p> <p>Updated <a href="#">Electrical Characteristics</a>: Updated details in "Test Conditions" column of <math>I_{SB2}</math> parameter (Included <math>\overline{BHE}</math> and <math>\overline{BLE}</math> to reflect Byte power down feature).</p> <p>Updated <a href="#">AC Test Loads and Waveforms</a>: Updated <a href="#">Table 1</a>.</p> <p>Updated <a href="#">Data Retention Characteristics</a>: Updated details in "Test Conditions" column of <math>I_{CCDR}</math> parameter (Included <math>\overline{BHE}</math> and <math>\overline{BLE}</math> to reflect Byte power down feature).</p> <p>Changed minimum value of <math>t_R</math> parameter from <math>t_{RC}</math> to 55 ns.</p> <p>Added <a href="#">Ordering Code Definitions</a> under <a href="#">Ordering Information</a>.</p> <p>Updated <a href="#">Package Diagram</a>.</p> <p>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a>.</p> <p>Changed all instances of IO to I/O.</p> <p>Updated to new template.</p>

**Document History Page** *(continued)*

Document Title: CY62187EV30 MoBL <sup>®</sup> , 64-Mbit (4 M × 16) Static RAM Document Number: 001-48998				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*F	3282088	RAME	06/14/2011	Updated <b>Functional Description</b> : Removed the note "For best practice recommendations, refer to the Cypress application note "System Design Guidelines" on <a href="http://www.cypress.com">http://www.cypress.com</a> website" and its reference. Updated <b>Electrical Characteristics</b> : Changed maximum value of $V_{IL}$ parameter corresponding to Test Condition " $2.7\text{ V} \leq V_{CC} \leq 3.7\text{ V}$ " from 0.7 V to 0.8 V. Added Note 6 and referred the same note in maximum value of $V_{IL}$ parameter. Updated to new template.
*G	3785005	TAVA	10/18/2012	Minor text edits. Updated <b>Package Diagram</b> : spec 001-50044 – Changed revision from *C to *D.
*H	4101127	VINI	08/21/2013	Updated <b>Switching Characteristics</b> : Added Note 14 and referred the same note in "Parameter" column. Updated to new template. Completing Sunset Review.
*I	4114808	NILE	09/12/2013	Updated <b>Electrical Characteristics</b> : Updated Note 7. Updated <b>Data Retention Characteristics</b> : Updated Note 10.
*J	4576478	NILE	11/21/2014	Updated <b>Functional Description</b> : Added "For a complete list of related documentation, <a href="#">click here.</a> " at the end. Updated <b>Switching Characteristics</b> : Added Note 19 and referred the same note in "Write Cycle". Updated <b>Switching Waveforms</b> : Added Note 29 and referred the same note in <b>Figure 8</b> .
*K	4990839	VINI	10/27/2015	Updated <b>Thermal Resistance</b> : Replaced "2-layer" with "four-layer" in "Test Conditions" column. Changed value of $\theta_{JA}$ parameter corresponding to FBGA package from 59.06 °C/W to 42.35 °C/W. Changed value of $\theta_{JC}$ parameter corresponding to FBGA package from 14.08 °C/W to 6.25 °C/W. Updated to new template. Completing Sunset Review.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

Automotive	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
Interface	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
Lighting & Power Control	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a>
Memory	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
PSoC	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
Touch Sensing	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
USB Controllers	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
Wireless/RF	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

#### PSoC<sup>®</sup> Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

#### Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

#### Technical Support

[cypress.com/go/support](http://cypress.com/go/support)

---

© Cypress Semiconductor Corporation, 2008-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Cypress Semiconductor:](#)

[CY62187EV30LL-55BAXI](#) [CY62187EV30LL-55BAXIT](#)