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# FAN7190\_F085

## High-Current, High & Low-Side, Gate-Drive IC

### Features

- Floating Channels for Bootstrap Operation to +600V
- Typically 4.5A/4.5A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- 3.3V and 5V Input Logic Compatible
- Output In-phase with Input

### Applications

- Diesel and gasoline Injectors/Valves
- MOSFET-and IGBT high side driver applications

### Description

The FAN7190\_F085 is a monolithic high- and low-side gate-drive IC, which can drive high speed MOSFETs and IGBTs that operate up to +600V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level shift circuit offers high-side gate driver operation up to  $V_S = -9.8V$  (typical) for  $V_{BS} = 15V$ .

The UVLO circuit prevents malfunction when  $V_{DD}$  and  $V_{BS}$  are lower than the specified threshold voltage.

The high current and low output voltage drop feature make this device suitable for magnetic- and piezo type injectors and general MOSFET/IGBT based high side driver applications.



8-Lead, SOIC, Narrow Body

### Ordering Information

Part Number	Package	Operating Temperature Range	Eco Status	Packing Method
FAN7190M_F085	8-SOP	-40°C ~ 125°C	RoHS	Tube
FAN7190MX_F085				Tape & Reel

#### Notes:

1. These devices passed wave soldering test by JESD22A-111.
2. A suffix as "...F085P" has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

### Typical Application Circuit

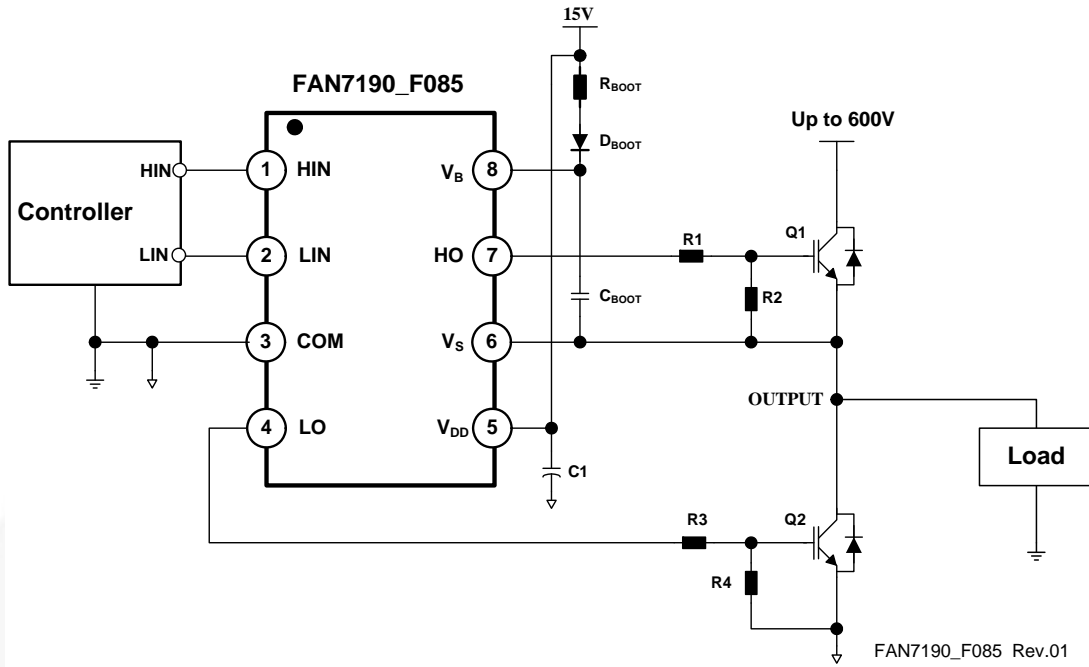


Figure 1. Application Circuit for Half-Bridge

### Internal Block Diagram

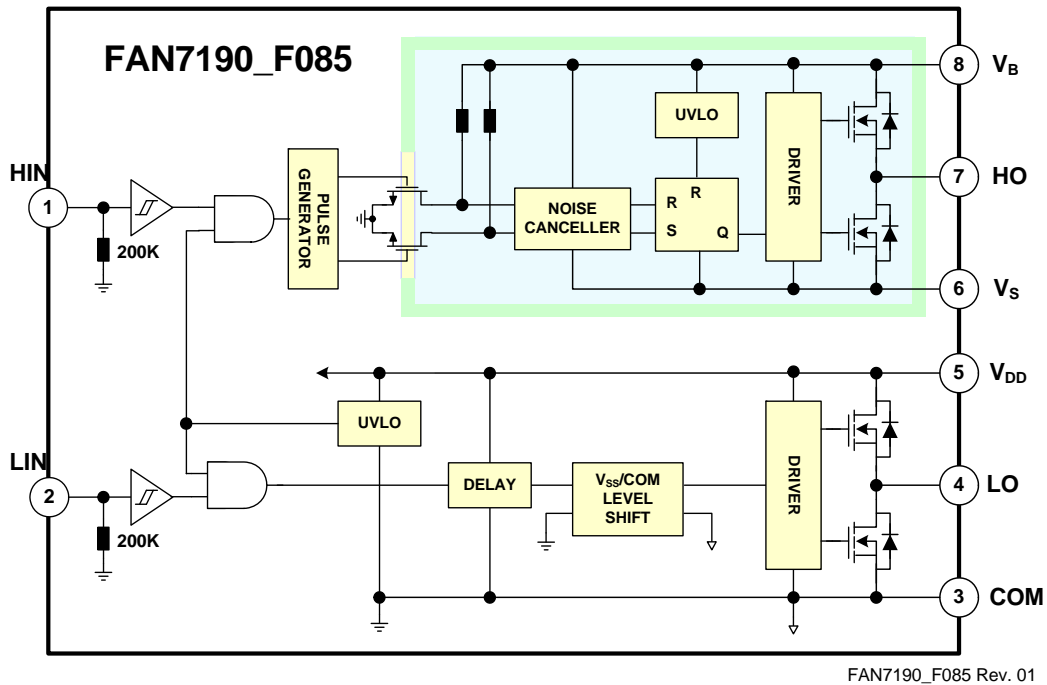
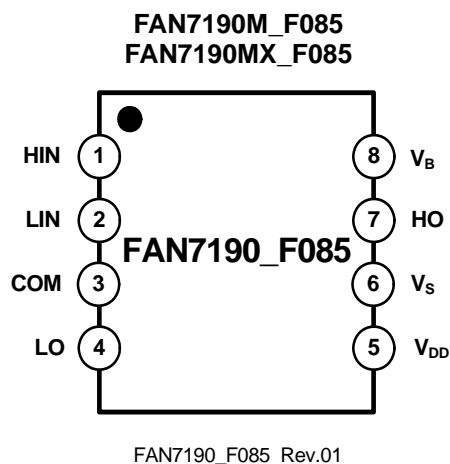


Figure 2. Functional Block Diagram

## Pin Configurations



**Figure 3. Pin Assignments (Top View)**

## Pin Definitions

8-Pin	Name	Description
1	HIN	Logic Input for High-Side Gate Driver Output
2	LIN	Logic Input for Low-Side Gate Driver Output
3	COM	Low-Side Driver Return
4	LO	Low-Side Driver Output
5	V <sub>DD</sub>	Low-Side and Logic Part Supply Voltage
6	V <sub>S</sub>	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	V <sub>B</sub>	High-Side Floating Supply

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
$V_S$	High-Side Floating Supply Offset Voltage	$V_B-25$	$V_B+0.3$	V
$V_B$	High-Side Floating Supply Voltage	-0.3	625.0	V
$V_{HO}$	High-Side Floating Output Voltage HO	$V_S-0.3$	$V_B+0.3$	V
$V_{DD}$	Low-Side and Logic Fixed Supply Voltage	-0.3	25.0	V
$V_{LO}$	Low-Side Output Voltage LO	-0.3	$V_{DD}+0.3$	V
$V_{IN}$	Logic Input Voltage (HIN and LIN)	-0.3	$V_{DD}+0.3$	V
$dV_S/dt$	Allowable Offset Voltage Slew Rate		50	V/ns
$P_D^{(3)(4)(5)}$	Power Dissipation	8-SOP	0.625	W
$\theta_{JA}$	Thermal Resistance, Junction-to-Ambient	8-SOP	200	$^{\circ}\text{C}/\text{W}$
$T_J$	Junction Temperature		+150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature		+150	$^{\circ}\text{C}$

### Notes:

- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
  - JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
  - JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
- Do not exceed  $P_D$  under any circumstances.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_B$	High-Side Floating Supply Voltage	$V_S+10$	$V_S+22$	V
$V_S$	High-Side Floating Supply Offset Voltage	$6-V_{DD}$	600	V
$V_{HO}$	High-Side Output Voltage	$V_S$	$V_B$	V
$V_{DD}$	Low-Side and Logic Supply Voltage	10	22	V
$V_{LO}$	Low-Side Output Voltage	COM	$V_{DD}$	V
$V_{IN}$	Logic Input Voltage (HIN and LIN)	COM	$V_{DD}$	V
$T_A$	Operating Ambient Temperature	-40	+125	$^{\circ}\text{C}$
$T_{\text{pulse}}$	Minimum Pulse Width <sup>(6)</sup>	80	-	ns

### Note:

- Guaranteed by design. Refer to Figure 28, 29 and 30 on page 11

## Electrical Characteristics

$V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ )=15.0V,  $V_S$ =COM,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$ , and  $I_{IN}$  parameters are referenced to COM and are applicable to the respective input signals HIN and LIN. The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_S$  is applicable to the respective output signals HO and LO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
<b>POWER SUPPLY SECTION (<math>V_{DD}</math> AND <math>V_{BS}</math>)</b>						
$V_{DDUV+}$ $V_{BSUV+}$	$V_{DD}$ and $V_{BS}$ Supply Under-Voltage Positive-going Threshold		7.8	8.8	9.8	V
$V_{DDUV-}$ $V_{BSUV-}$	$V_{DD}$ and $V_{BS}$ Supply Under-Voltage Negative-going Threshold		7.2	8.3	9.1	
$V_{DDUVH}$ $V_{BSUVH}$	$V_{DD}$ and $V_{BS}$ Supply Under-Voltage Lockout Hysteresis Voltage			0.5		
$I_{LK}$	Offset Supply Leakage Current	$V_B=V_S=600\text{V}$			50	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	$V_{IN}=0\text{V}$ or $5\text{V}$		45	110	
$I_{QDD}$	Quiescent $V_{DD}$ Supply Current	$V_{IN}=0\text{V}$ or $5\text{V}$		75	150	
$I_{PBS}$	Operating $V_{BS}$ Supply Current	$f_{IN}=20\text{kHz}$ , rms value		530	700	$\mu\text{A}$
$I_{PDD}$	Operating $V_{DD}$ Supply Current	$f_{IN}=20\text{kHz}$ , rms value		530	750	
<b>LOGIC INPUT SECTION (HIN, LIN)</b>						
$V_{IH}$	Logic "1" Input Voltage		2.5			V
$V_{IL}$	Logic "0" Input Voltage				1.2	
$I_{IN+}$	Logic "1" Input Bias Current	$V_{IN}=5\text{V}$		25	50	$\mu\text{A}$
$I_{IN-}$	Logic "0" Input Bias Current	$V_{IN}=0\text{V}$		1.0	2.0	
$R_{IN}$	Input Pull-down Resistance		100	200		$\text{K}\Omega$
<b>GATE DRIVER OUTPUT SECTION (HO, LO)</b>						
$V_{OH}$	High-level Output Voltage, $V_{BIAS}-V_O$	No Load			1.5	V
$V_{OL}$	Low-level Output Voltage, $V_O$	No Load			35	mV
$I_{O+}$	Output High, Short-circuit Pulsed Current <sup>(6)</sup>	$V_O=0\text{V}$ , $V_{IN}=5\text{V}$ with $\text{PW}<10\mu\text{s}$	3.5	4.5		A
$I_{O-}$	Output Low, Short-circuit Pulsed Current <sup>(6)</sup>	$V_O=15\text{V}$ , $V_{IN}=0\text{V}$ with $\text{PW}<10\mu\text{s}$	3.5	4.5		
$V_S$	Allowable Negative $V_S$ Pin Voltage for HIN Signal Propagation to HO			-9.8	-7.0	V

### Note:

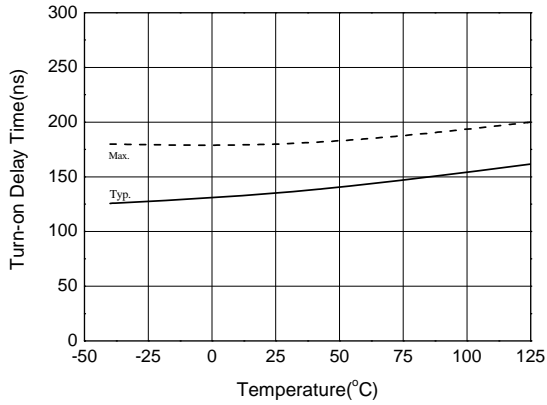
6. This parameter guaranteed by design.

## Dynamic Electrical Characteristics

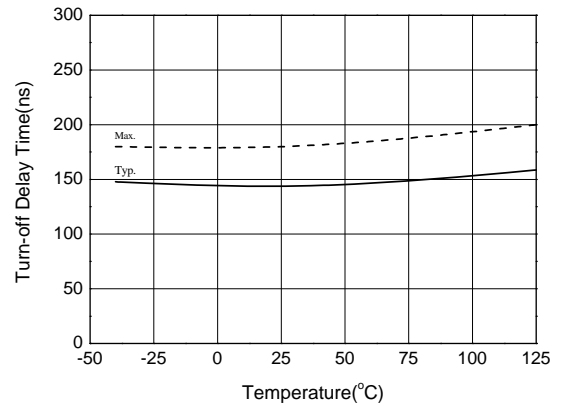
$V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ )=15.0V,  $V_S$ =COM=0V,  $C_L=1000\text{pF}$  and  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on Propagation Delay	$V_S=0\text{V}$		140	200	ns
$t_{off}$	Turn-off Propagation Delay	$V_S=0\text{V}$		140	200	
MT	Delay Matching, HS & LS Turn-on/off			0	50	
$t_r$	Turn-on Rise Time			25	50	
$t_f$	Turn-off Fall Time			20	45	

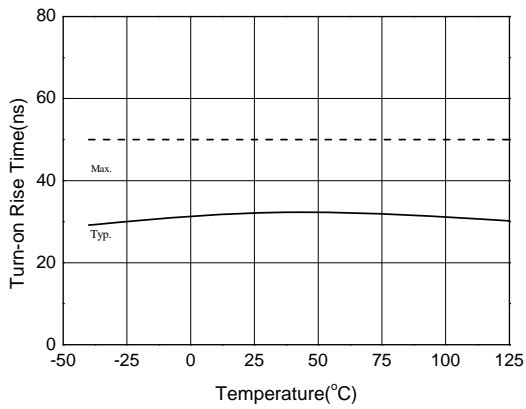
## Typical Characteristics



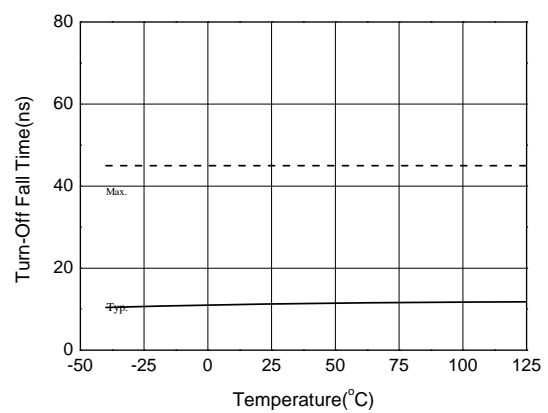
**Figure 4. Turn-on Propagation Delay vs. Temperature**



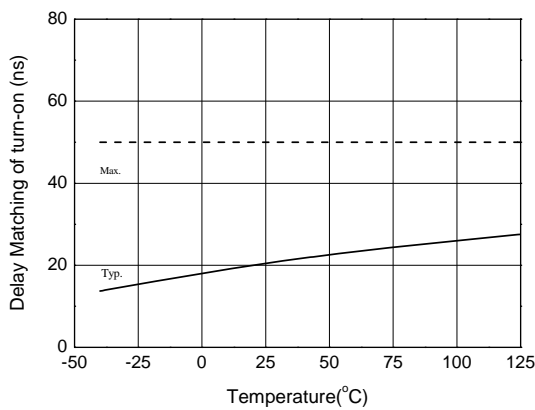
**Figure 5. Turn-off Propagation Delay vs. Temperature**



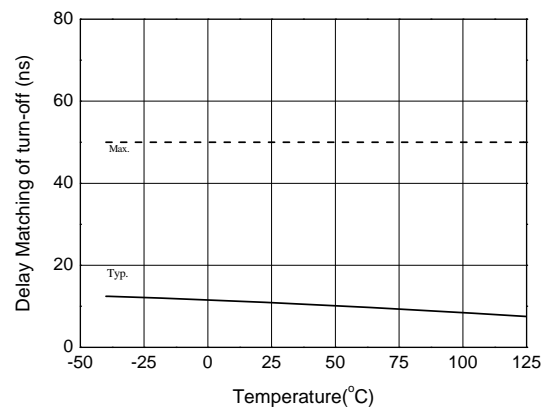
**Figure 6. Turn-on Rise Time vs. Temperature**



**Figure 7. Turn-off Fall Time vs. Temperature**



**Figure 8. Turn-on Delay Matching vs. Temperature**



**Figure 9. Turn-off Delay Matching vs. Temperature**

Typical Characteristics (Continued)

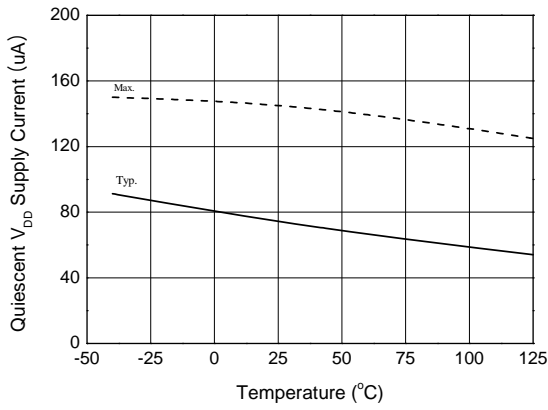


Figure 10. Quiescent  $V_{DD}$  Supply Current vs. Temperature

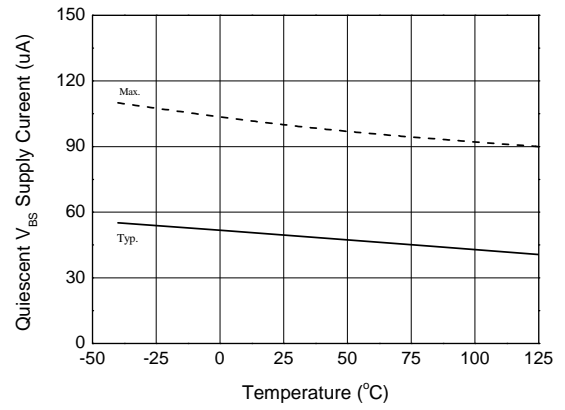


Figure 11. Quiescent  $V_{BS}$  Supply Current vs. Temperature

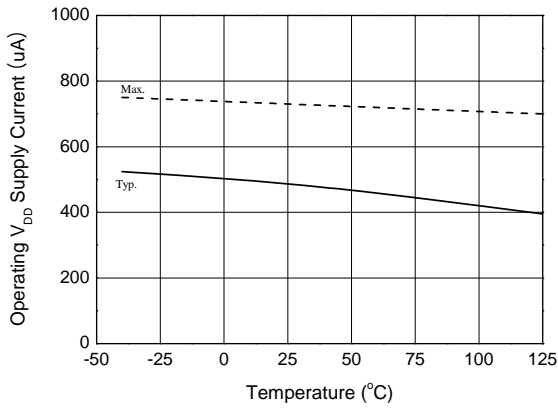


Figure 12. Operating  $V_{DD}$  Supply Current vs. Temperature

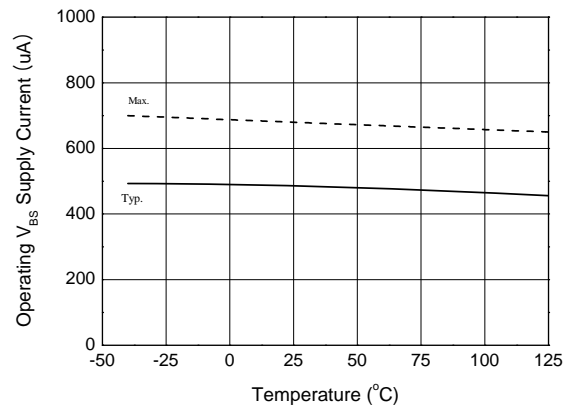


Figure 13. Operating  $V_{BS}$  Supply Current vs. Temperature.

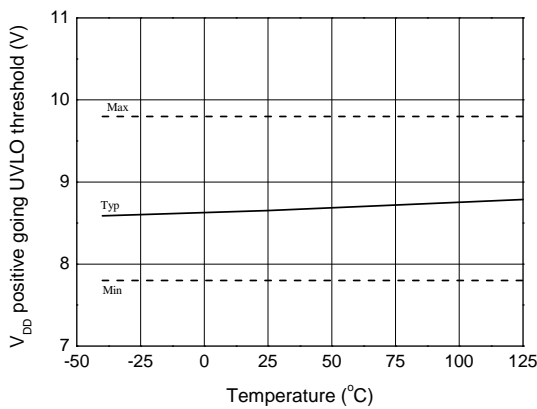


Figure 14.  $V_{DD}$  UVLO+ vs. Temperature

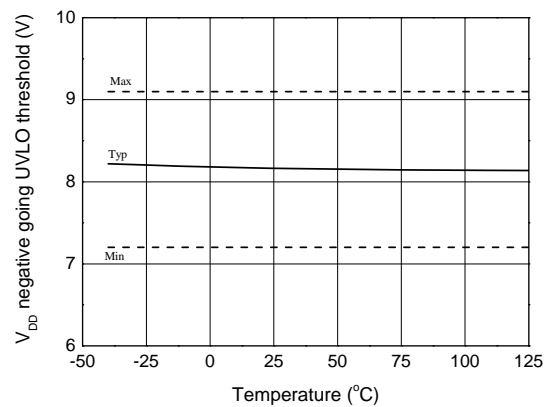


Figure 15.  $V_{DD}$  UVLO- vs. Temperature



Typical Characteristics (Continued)

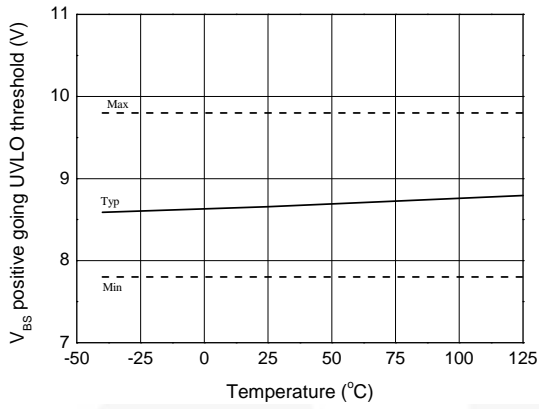


Figure 16.  $V_{BS}$  UVLO+ vs. Temperature

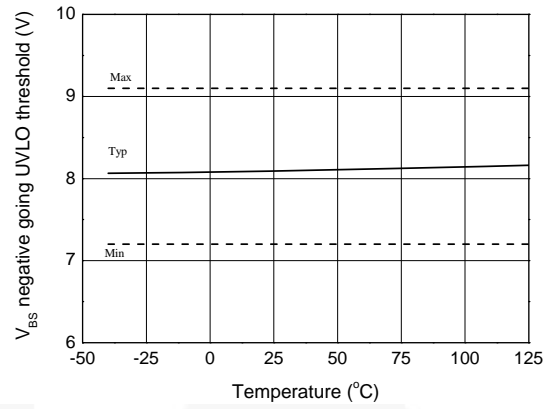


Figure 17.  $V_{BS}$  UVLO- vs. Temperature

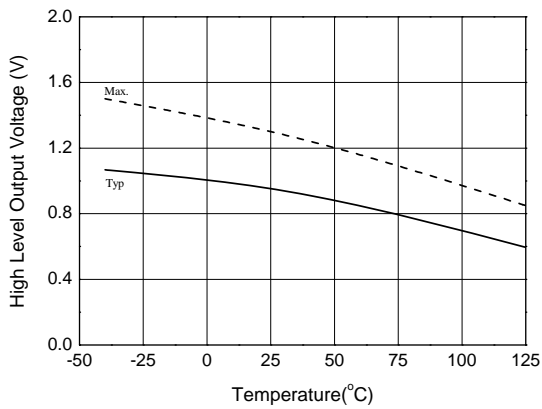


Figure 18. High-Level Output Voltage vs. Temperature

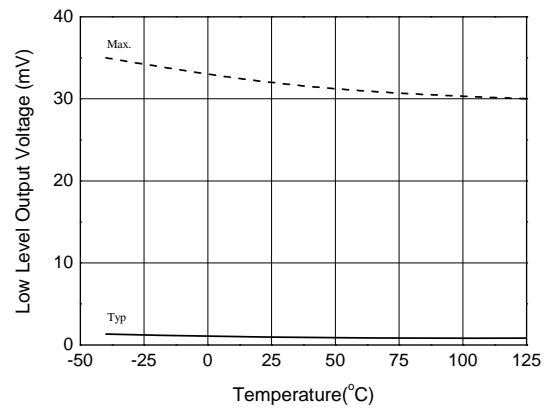


Figure 19. Low-Level Output Voltage vs. Temperature

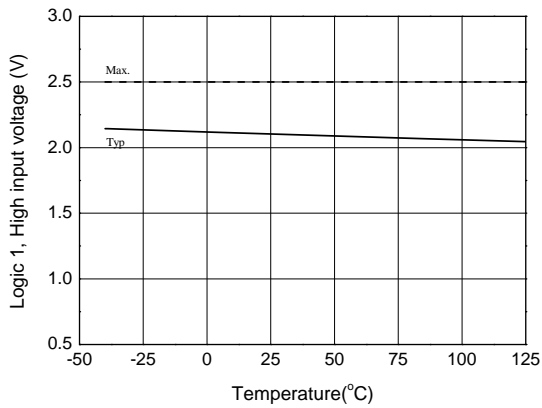


Figure 20. Logic High Input Voltage vs. Temperature

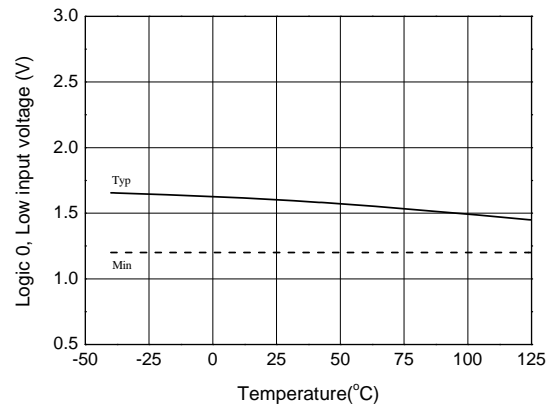


Figure 21. Low Input Voltage vs. Temperature

Typical Characteristics (Continued)

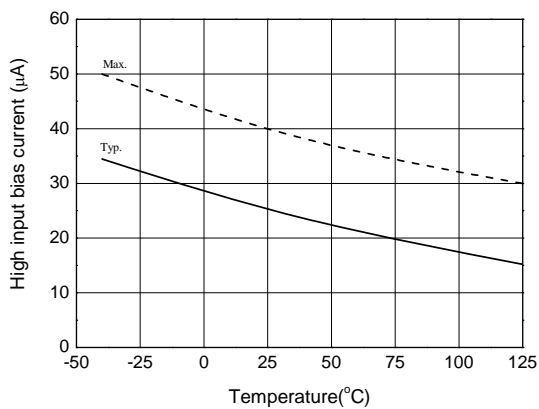


Figure 22. Logic Input High Bias Current vs. Temperature

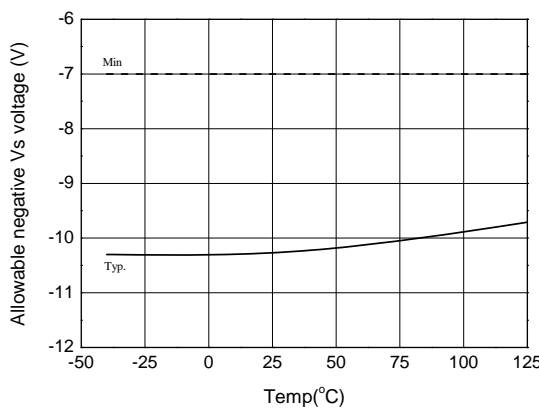


Figure 23. Allowable Negative  $V_S$  Voltage vs. Temperature



### Switching Time Definitions

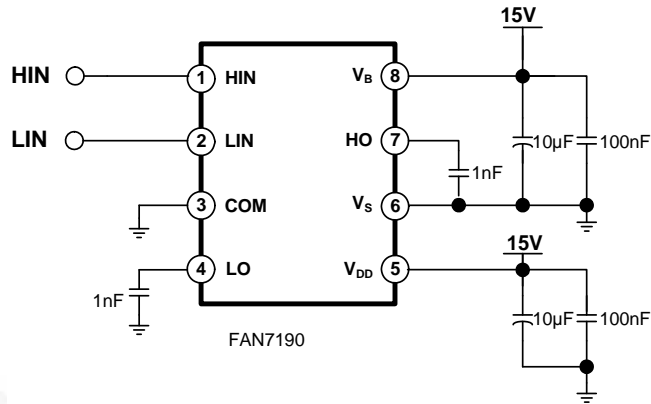


Figure 24. Switching Time Test Circuit (Referenced 8-SOP)

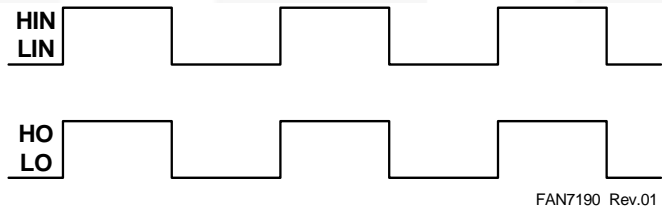


Figure 25. Input/Output Timing Diagram

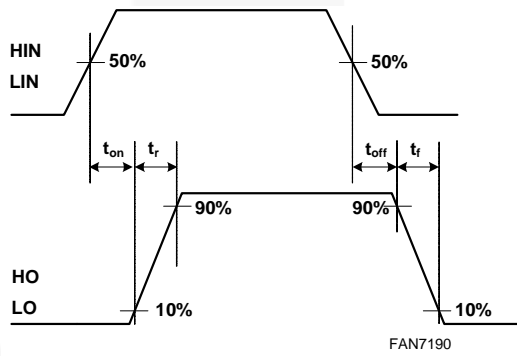


Figure 26. Switching Time Waveform Definitions

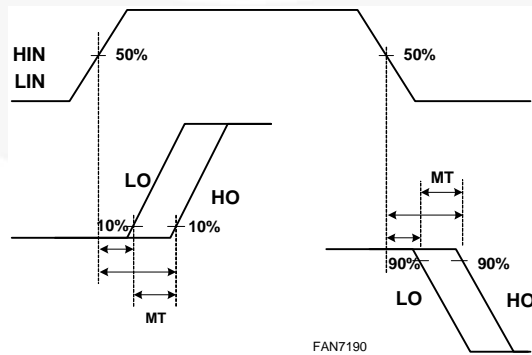


Figure 27. Delay Matching Waveform Definitions

Switching Time Definitions

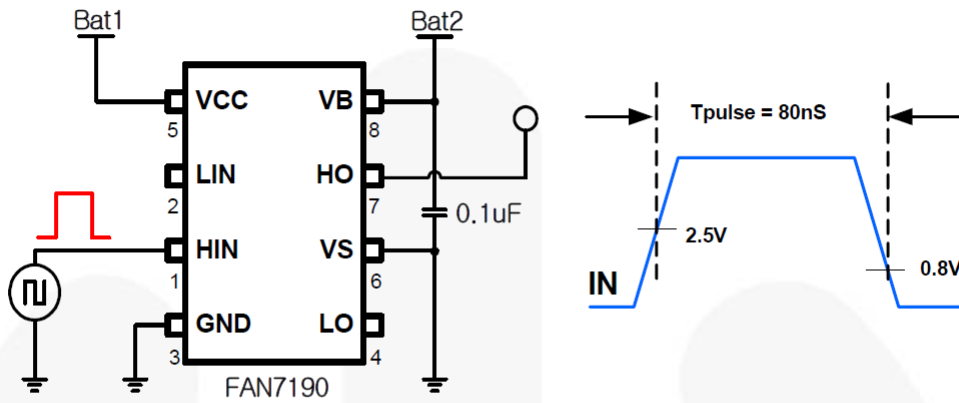


Figure 28. Short Pulse Width Test Circuit and Pulse Width Waveform

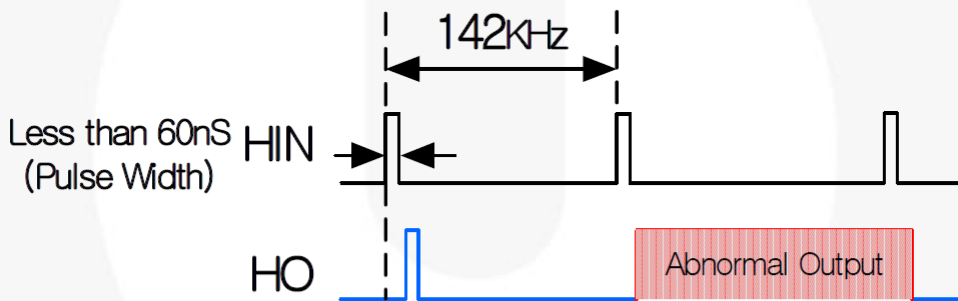


Figure 29. Abnormal Output Waveform with short pulse width

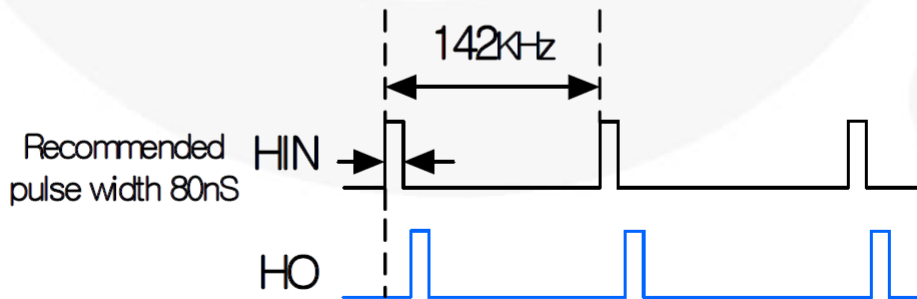
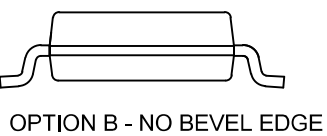
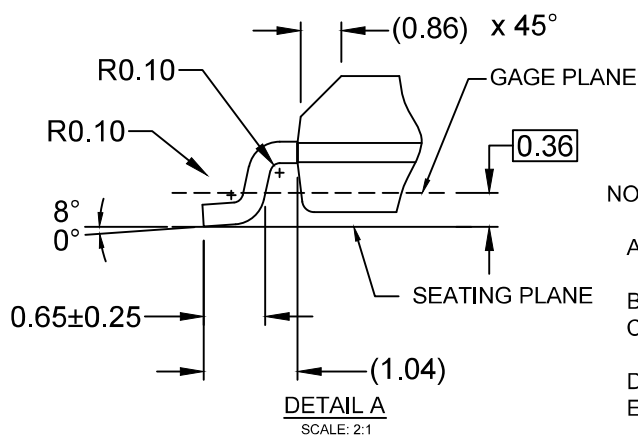
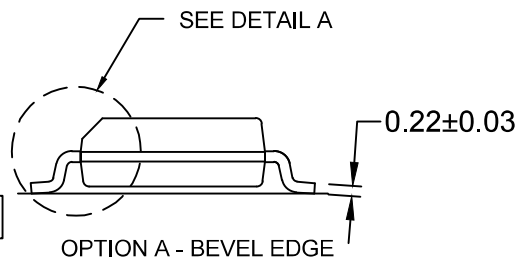
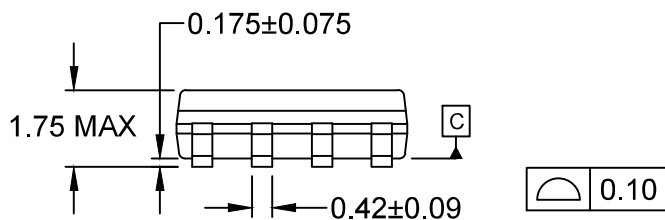
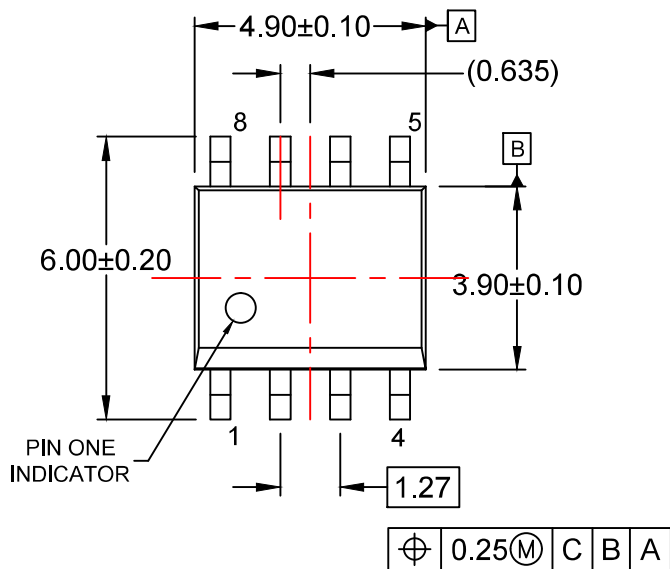


Figure 30. Recommendation of pulse width Output Waveform



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16





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