



# FCH085N80

## N-Channel SuperFET<sup>®</sup> II MOSFET

800 V, 46 A, 85 mΩ

### Features

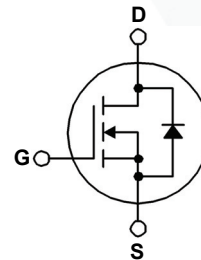
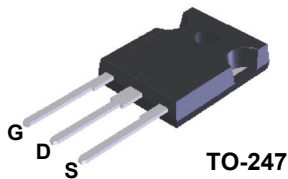
- Typ.  $R_{DS(on)}$  = 67 mΩ
- 850 V @  $T_J = 150^{\circ}\text{C}$
- Ultra Low Gate Charge (Typ.  $Q_g = 196$  nC)
- Low  $E_{OSS}$  (Typ. 18 μJ @ 400 V)
- Low Effective Output Capacitance (Typ.  $C_{OSS(eff.)} = 568$  pF)
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- AC-DC Power Supply
- LED Lighting

### Description

SuperFET<sup>®</sup> II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



### Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$ unless otherwise noted.

Symbol	Parameter	FCH085N80_F155	Unit
$V_{DSS}$	Drain to Source Voltage	800	V
$V_{GSS}$	Gate to Source Voltage	- DC	±20
		- AC (f > 1 Hz)	±30
$I_D$	Drain Current	- Continuous ( $T_C = 25^{\circ}\text{C}$ )	46
		- Continuous ( $T_C = 100^{\circ}\text{C}$ )	29
$I_{DM}$	Drain Current	- Pulsed (Note 1)	138
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	1701
$I_{AR}$	Avalanche Current	(Note 1)	9.2
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	4.4
dv/dt	MOSFET dv/dt		100
	Peak Diode Recovery dv/dt	(Note 3)	20
$P_D$	Power Dissipation	( $T_C = 25^{\circ}\text{C}$ )	446
		- Derate Above 25°C	3.5
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	°C
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	FCH085N80_F155	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.28	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40.0	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH085N80_F155	FCH085N80	TO-247 G03	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	800	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.8	-	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 640\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	-	250	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 4.6\text{ mA}$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 23\text{ A}$	-	67	85	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 23\text{ A}$	-	55	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	8140	10825	pF
$C_{oss}$	Output Capacitance		-	255	340	pF
$C_{riss}$	Reverse Transfer Capacitance		-	10	-	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1000	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	728	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 640\text{ V}, I_D = 46\text{ A}, V_{GS} = 10\text{ V}$	-	196	255	nC
$Q_{gs}$	Gate to Source Gate Charge		-	40	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	72	-
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.8	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 46\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\ \Omega$	-	45	100	ns
$t_r$	Turn-On Rise Time		-	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time		-	160	330	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	35	80

### Drain-Source Diode Characteristics

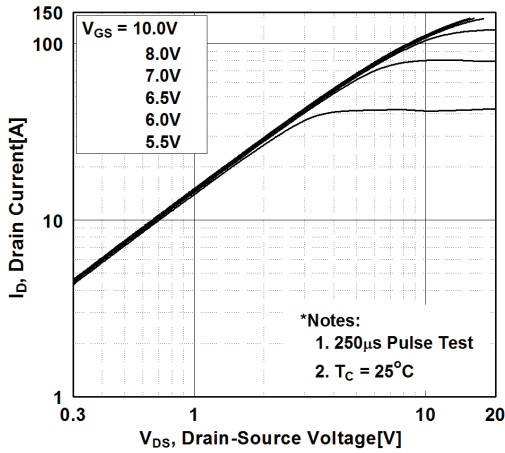
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	46	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	138	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 46\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 46\text{ A}$	-	800	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt = 100\text{ A}/\mu\text{s}$	-	32	-	$\mu\text{C}$

#### Notes:

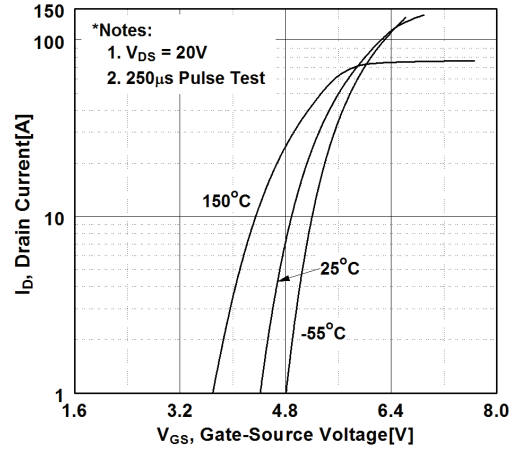
1. Repetitive rating: pulse width limited by maximum junction temperature.
2.  $I_{AS} = 9.2\text{ A}, V_{DD} = 50\text{ V}, R_g = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 46\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

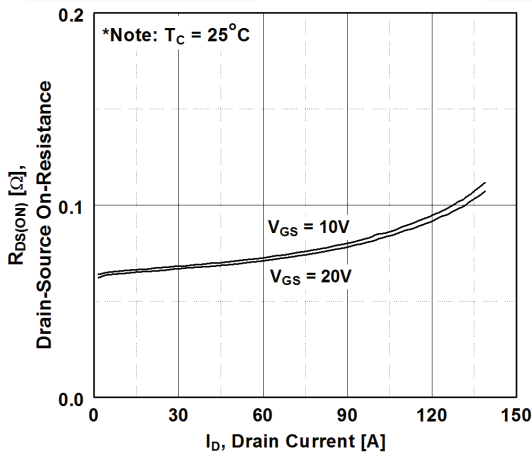
**Figure 1. On-Region Characteristics**



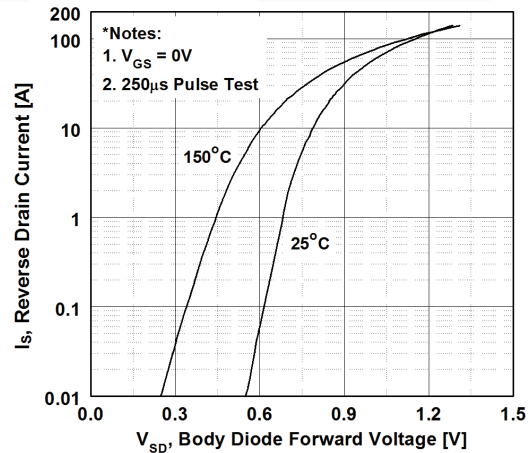
**Figure 2. Transfer Characteristics**



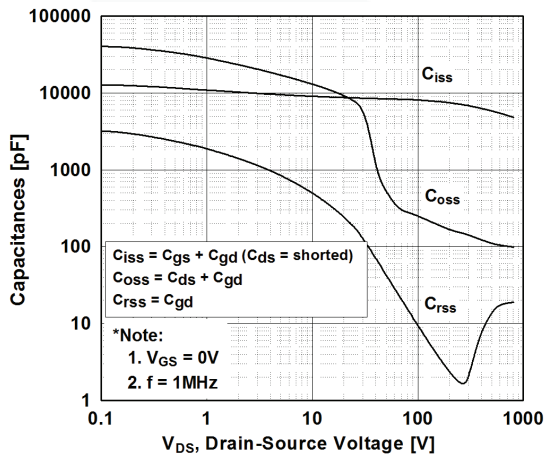
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



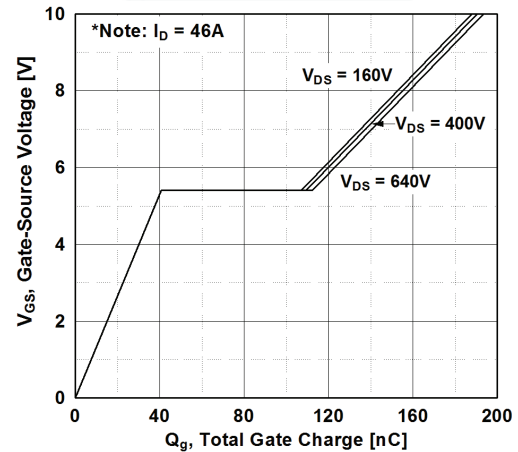
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

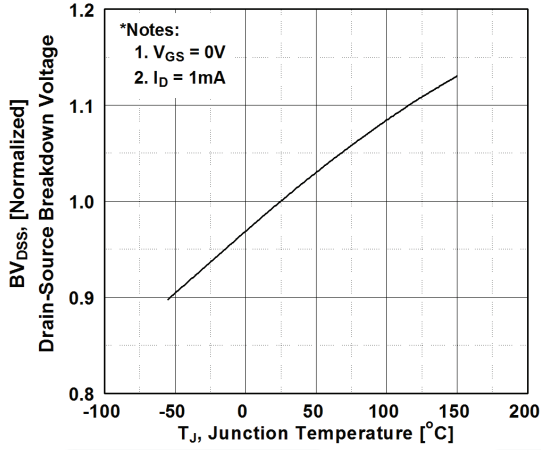


**Figure 6. Gate Charge Characteristics**

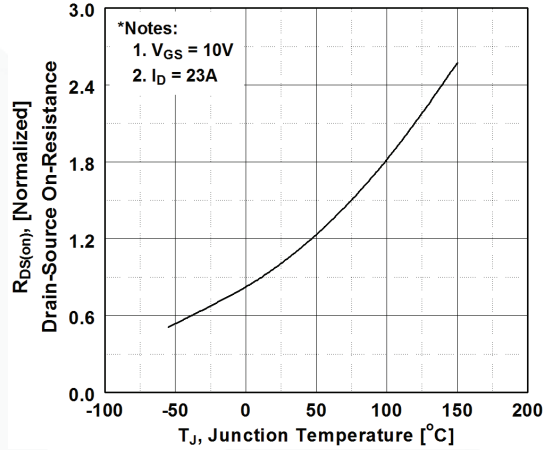


**Typical Performance Characteristics** (Continued)

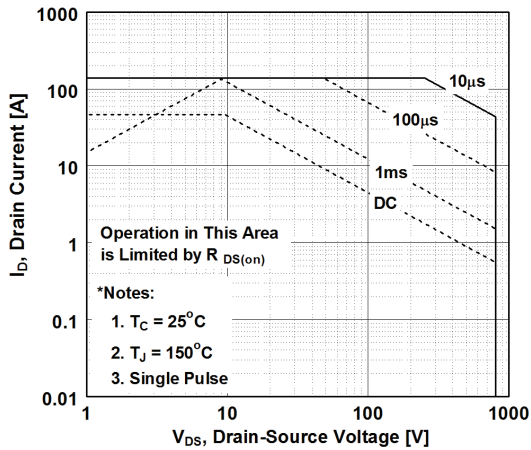
**Figure 7. Breakdown Voltage Variation vs. Temperature**



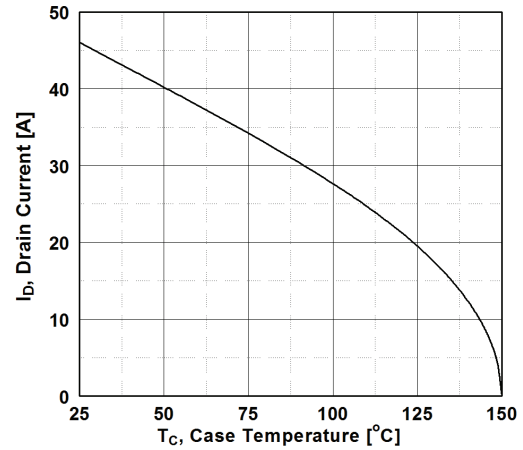
**Figure 8. On-Resistance Variation vs. Temperature**



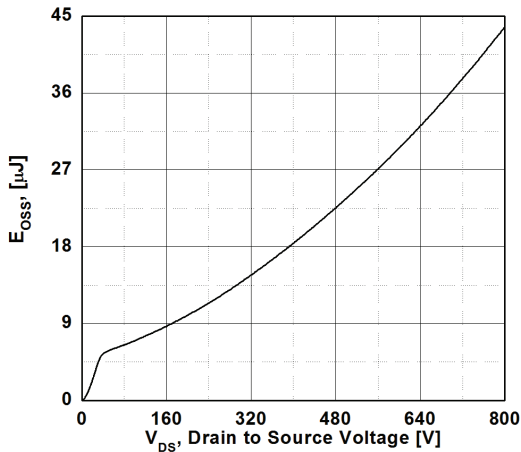
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Eoss vs. Drain to Source Voltage**



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve

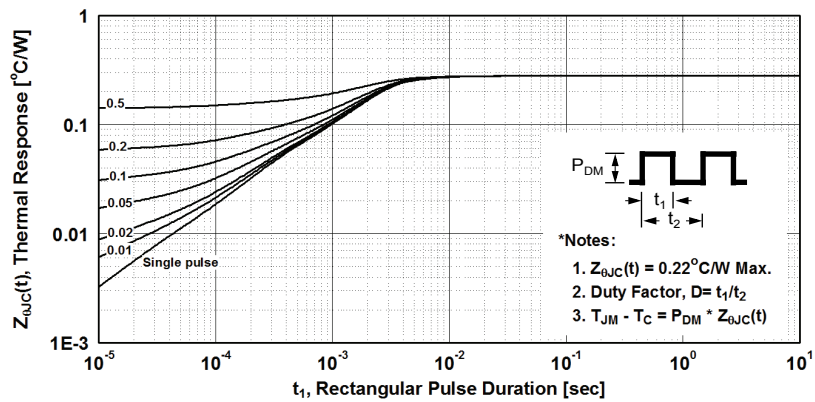


Figure 13. Gate Charge Test Circuit & Waveform

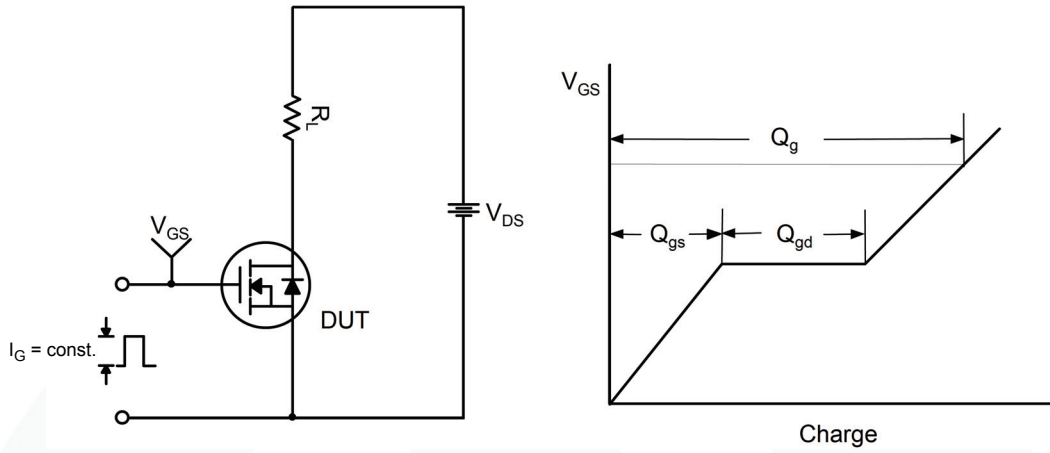


Figure 14. Resistive Switching Test Circuit & Waveforms

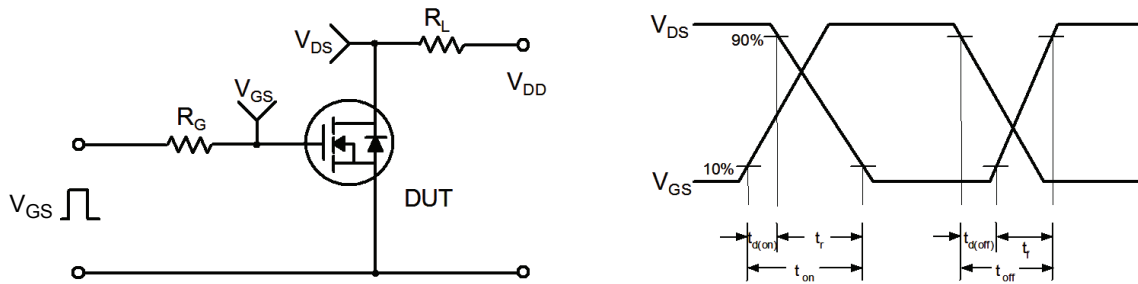


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

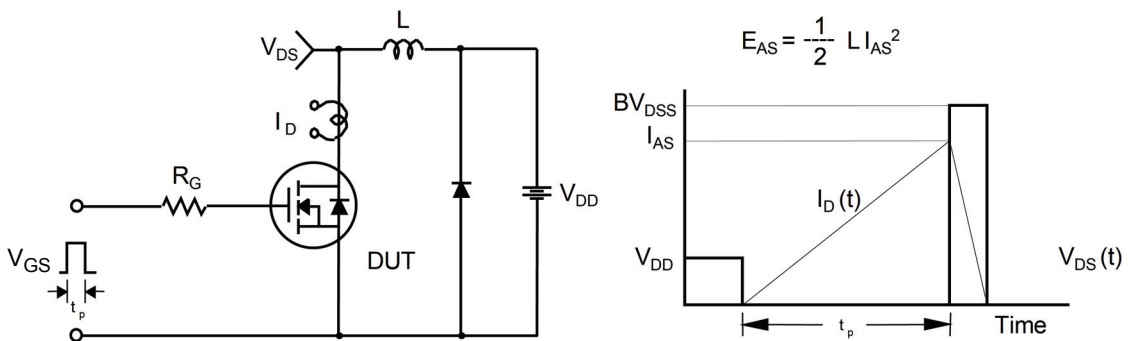
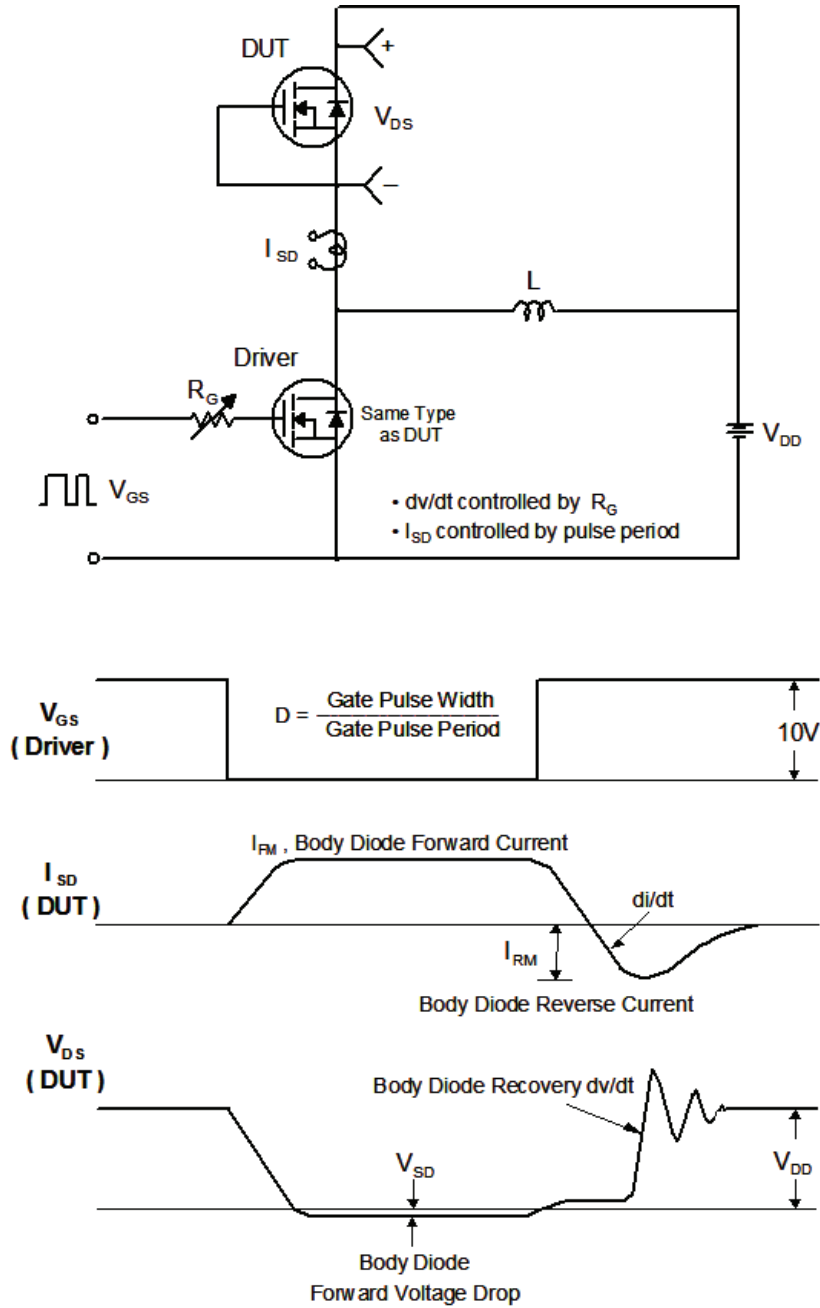
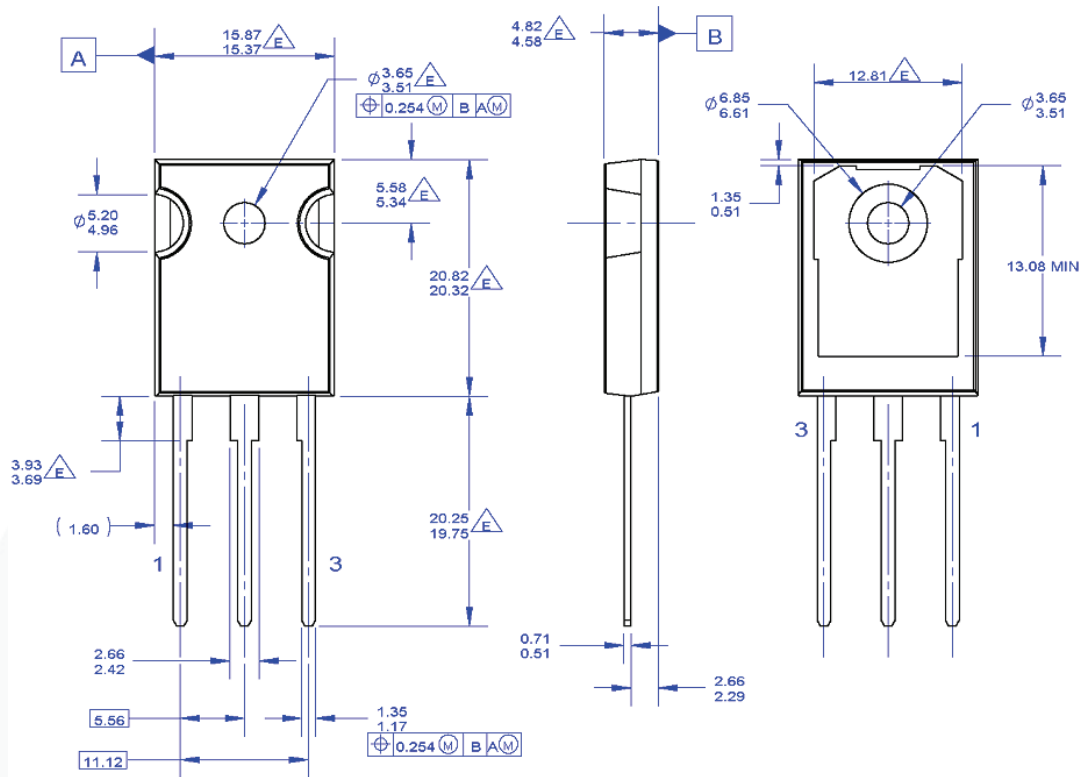


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

- $\triangle E$  DOES NOT COMPLY JEDEC STANDARD VALUE
- F. DRAWING FILENAME: MKT-TO247G03\_REV01

**Figure 17. TO-247, MOLDED, 3 LEAD, JEDEC AB LONG LEADS (Active)**

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| BitSiC™                  | GreenBridge™                                    | QFET®                                 | TinyCalc™        |
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| ESBC™                    | MicroPak™                                       | SuperFET®                             | Ultra FRFET™     |
| <b>F</b> ®               | MicroPak2™                                      | SuperSOT™-3                           | UniFET™          |
| Fairchild®               | MillerDrive™                                    | SuperSOT™-6                           | VCX™             |
| Fairchild Semiconductor® | MotionMax™                                      | SuperSOT™-8                           | VisualMax™       |
| FACT Quiet Series™       | MotionGrid®                                     | SupreMOS®                             | VoltagePlus™     |
| FACT®                    | MTI®  | SyncFET™                              | XS™              |
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