

# FDC2512

## 150V N-Channel PowerTrench® MOSFET

### General Description

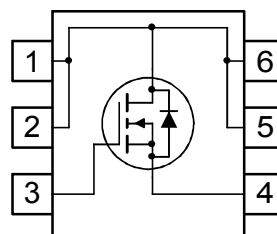
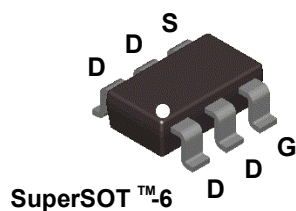
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### Applications

- DC/DC converter

### Features

- 1.4 A, 150 V.  $R_{DS(ON)} = 425 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 475 \text{ m}\Omega @ V_{GS} = 6 \text{ V}$
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Low gate charge (8nC typ)
- High power and current handling capability
- Fast switching speed



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	150	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a)	1.4	A
	– Pulsed	8	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	13.5	mJ
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	1.6	W
		0.8	
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	30	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.252	FDC2512	7"	8mm	3000 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		147		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	2.6	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-5.6		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}$ $V_{GS} = 6.0\text{ V}, I_D = 1.3\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}, T_J = 125^\circ\text{C}$		319 332 624	425 475 875	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	4			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 1.4\text{ A}$		4		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		344		pF
$C_{oss}$	Output Capacitance			22		pF
$C_{rss}$	Reverse Transfer Capacitance			9		pF

### Switching Characteristics (Note 2)

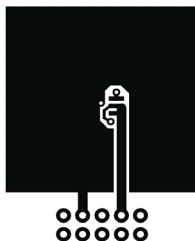
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 75\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		6.5	13	ns
$t_r$	Turn–On Rise Time			3.5	7	ns
$t_{d(off)}$	Turn–Off Delay Time			22	33	ns
$t_f$	Turn–Off Fall Time			4	8	ns
$Q_g$	Total Gate Charge	$V_{DS} = 75\text{ V}, I_D = 1.4\text{ A},$ $V_{GS} = 10\text{ V}$		8	11	nC
$Q_{gs}$	Gate–Source Charge			1.5		nC
$Q_{gd}$	Gate–Drain Charge			2.3		nC

### Drain–Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain–Source Diode Forward Current			1.3		A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 1.4\text{ A},$		45.8		nS
$Q_{rr}$	Diode Reverse Recovery Charge	$dI_F/dt = 300\text{ A}/\mu\text{s}$ (Note 2)		119		nC

#### Notes:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $78^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $156^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

3. Starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 3\text{ mH}, I_{AS} = 3\text{ A}, V_{DD} = 150\text{ V}, V_{GS} = 10\text{ V}$ ; 100% UIL tested.

## Typical Characteristics

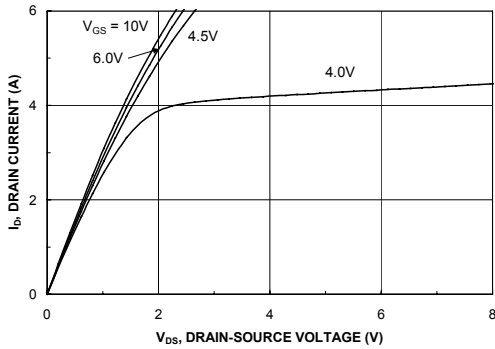


Figure 1. On-Region Characteristics.

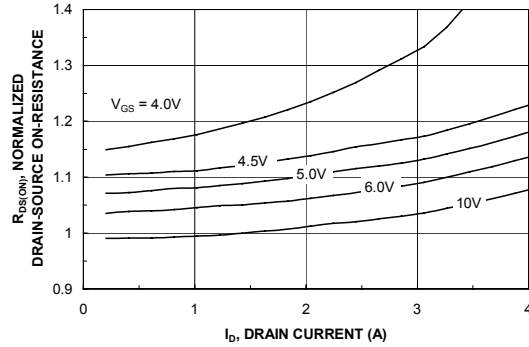


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

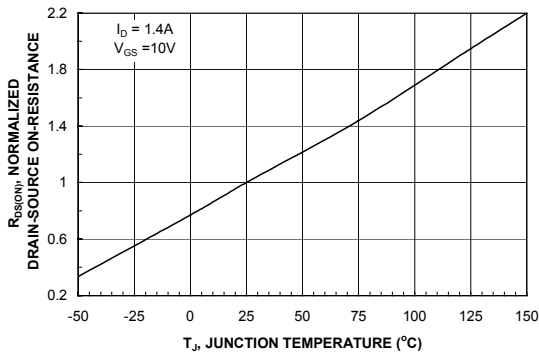


Figure 3. On-Resistance Variation with Temperature.

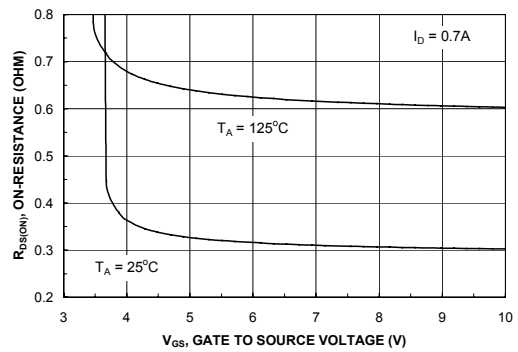


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

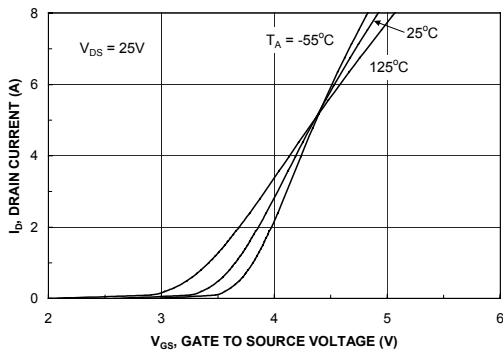


Figure 5. Transfer Characteristics.

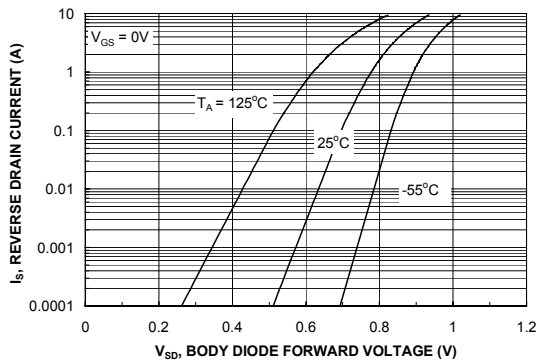
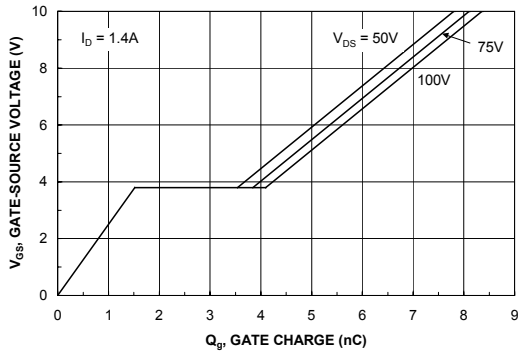
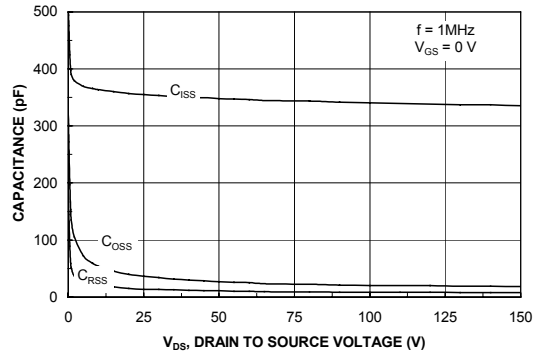


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

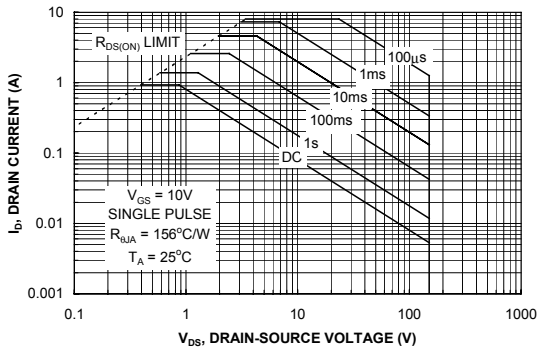
## Typical Characteristics



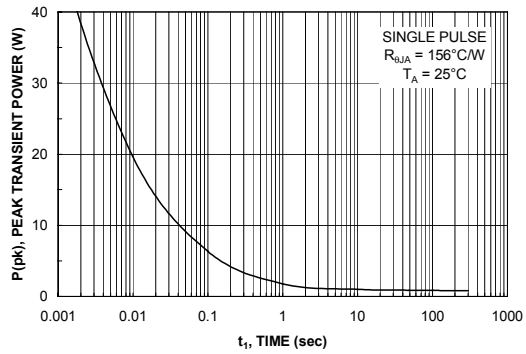
**Figure 7. Gate Charge Characteristics.**



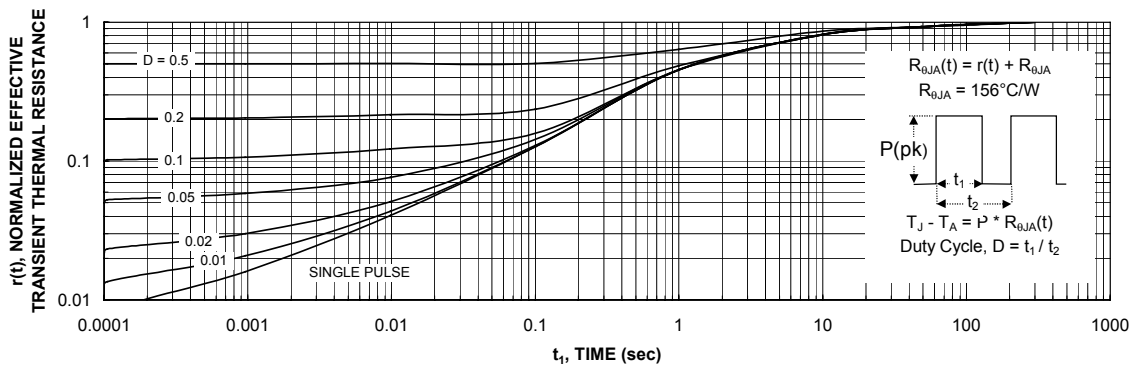
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**





**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.



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