

# FDC8602

## Dual N-Channel Shielded Gate PowerTrench® MOSFET 100 V, 1.2 A, 350 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 350 mΩ at  $V_{GS} = 10$  V,  $I_D = 1.2$  A
- Max  $r_{DS(on)}$  = 575 mΩ at  $V_{GS} = 6$  V,  $I_D = 0.9$  A
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

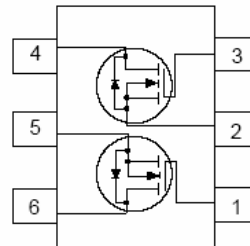
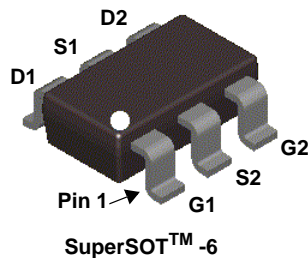


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Applications

- Load Switch
- Synchronous Rectifier



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous (Note 1a)	1.2	A
	-Pulsed	5	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	1.5	mJ
$P_D$	Power Dissipation (Note 1a)	0.96	W
	Power Dissipation (Note 1b)	0.69	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	130	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.862	FDC8602	SSOT-6	7"	8 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		73		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-8		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 1.2\text{ A}$		285	350	m $\Omega$
		$V_{GS} = 6\text{ V}, I_D = 0.9\text{ A}$		409	575	
		$V_{GS} = 10\text{ V}, I_D = 1.2\text{ A}, T_J = 125\text{ }^\circ\text{C}$		489	600	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 1.2\text{ A}$		1.3		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		53	70	pF
$C_{oss}$	Output Capacitance			17	25	pF
$C_{rss}$	Reverse Transfer Capacitance			0.8	5	pF
$R_g$	Gate Resistance			1.6		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 1.2\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		3.5	10	ns	
$t_r$	Rise Time			1.7	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			5.4	11	ns	
$t_f$	Fall Time			2.3	10	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		1.2	2	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }5\text{ V}$	$V_{DD} = 50\text{ V},$ $I_D = 1.2\text{ A}$		0.6	1	nC
$Q_{gs}$	Gate to Source Charge				0.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				0.4		nC

### Drain-Source Diode Characteristics

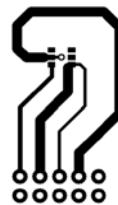
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.2\text{ A}$ (Note 2)		0.86	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = 1.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		27	43	ns
$Q_{rr}$	Reverse Recovery Charge			12	21	nC

#### NOTES:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $130\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2oz copper

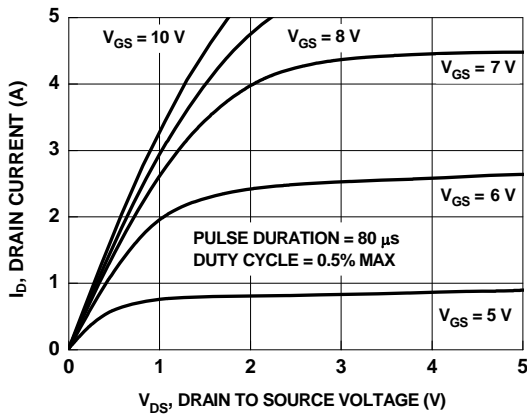


b)  $180\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2oz copper

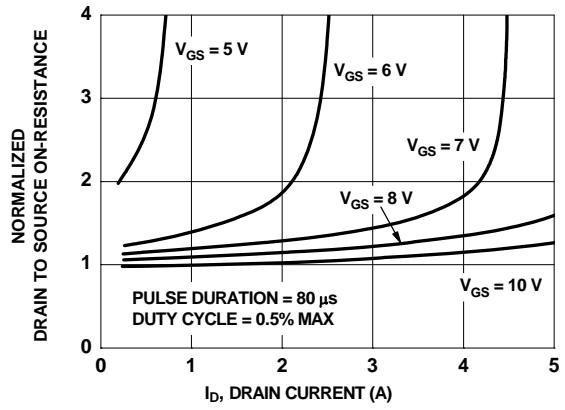
2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 3\text{ mH}, I_{AS} = 1\text{ A}, V_{DD} = 100\text{ V}, V_{GS} = 10\text{ V}$ .

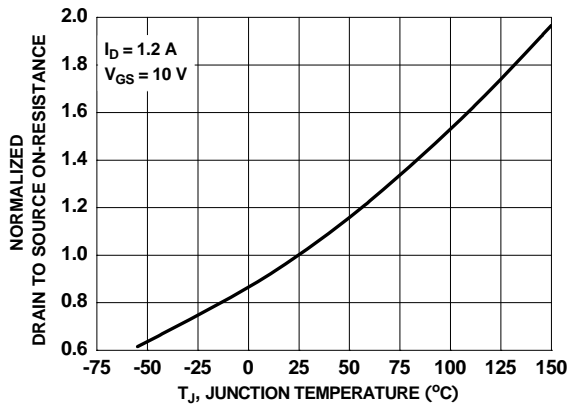
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



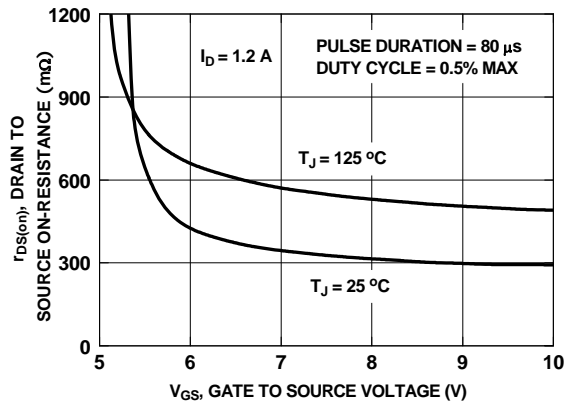
**Figure 1. On Region Characteristics**



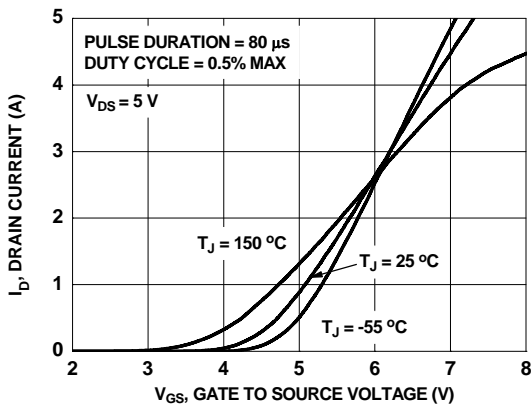
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



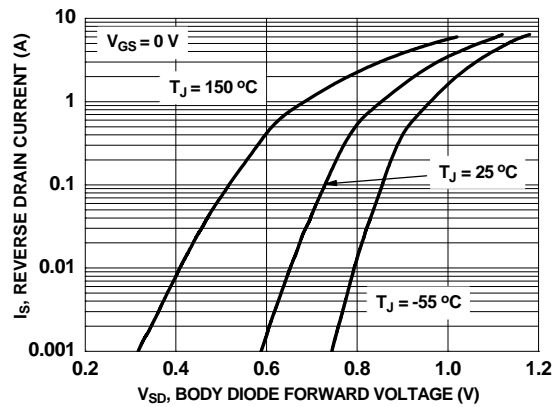
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

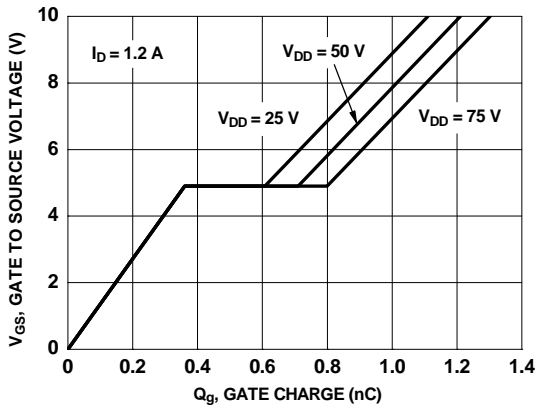


**Figure 5. Transfer Characteristics**

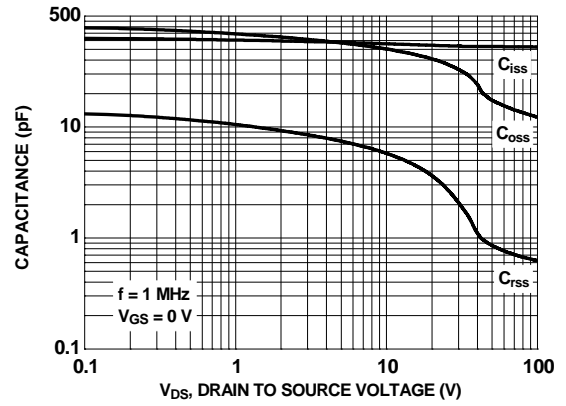


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

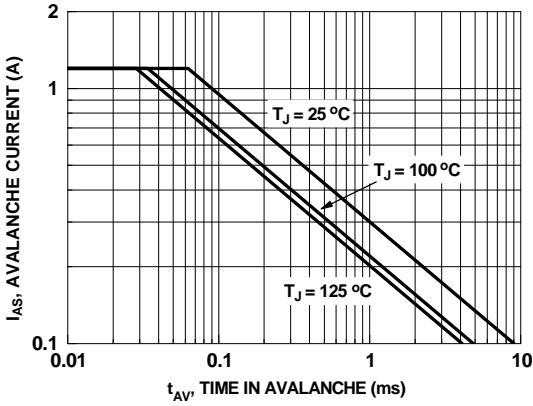
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



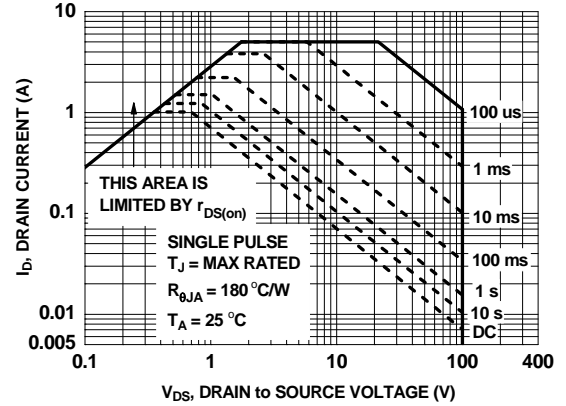
**Figure 7. Gate Charge Characteristics**



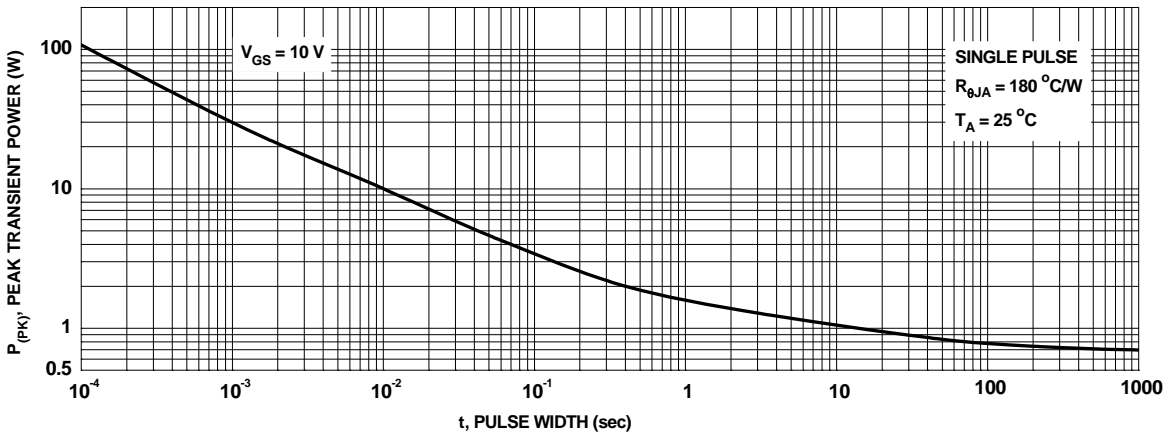
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Unclamped Inductive Switching Capability**

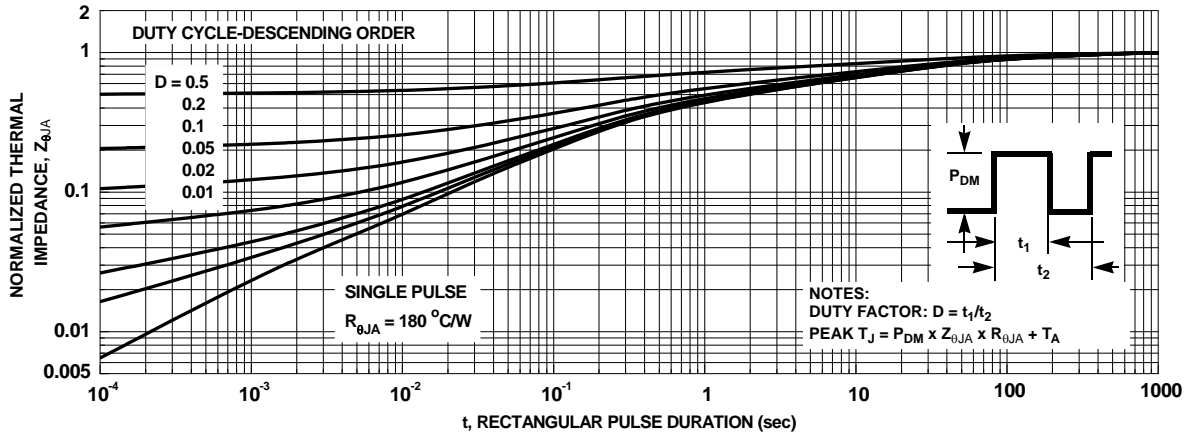


**Figure 10. Forward Bias Safe Operating Area**



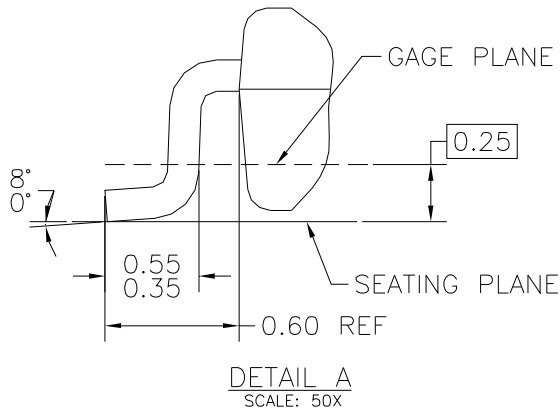
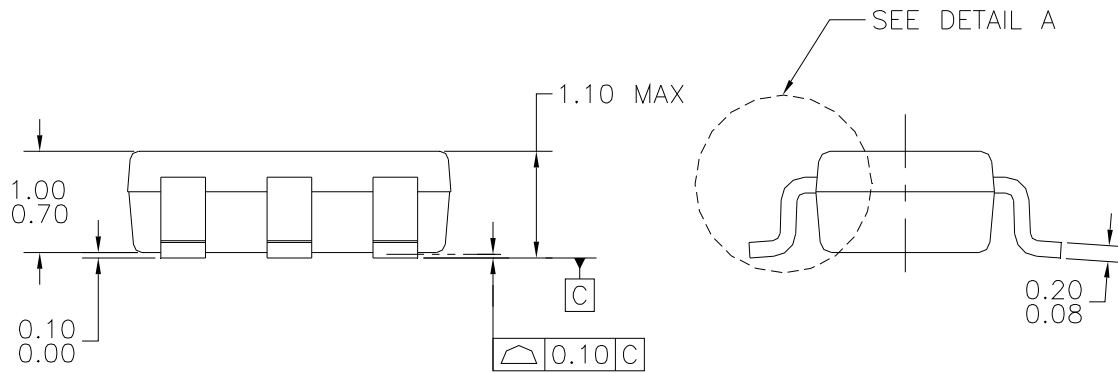
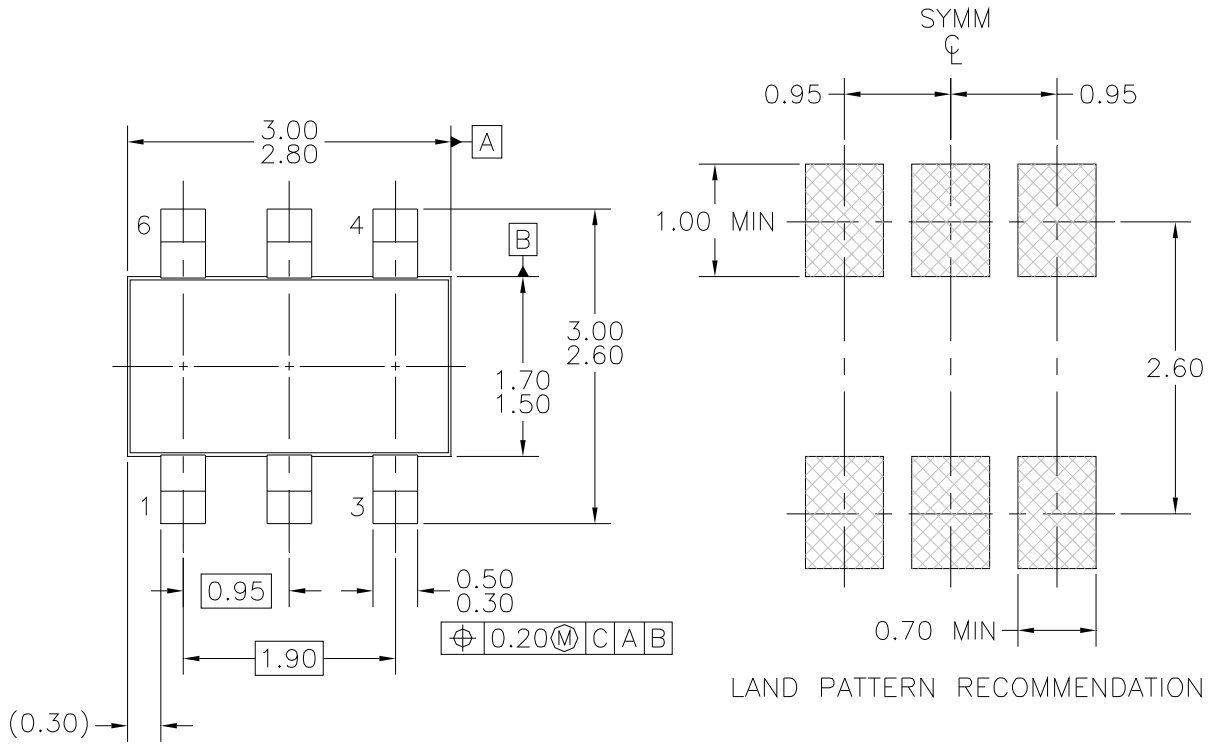
**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

### Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED


- A) THIS PACKAGE CONFORMS TO JEDEC MO-193. VAR. AA, ISSUE C, DATED JANUARY 2000.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.

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