

FDD7N60NZ / FDU7N60NZTU

N-Channel UniFET™ II MOSFET

600 V, 5.5 A, 1.25 Ω

Features

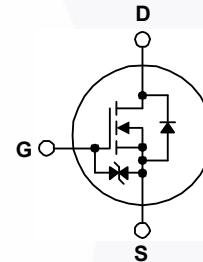
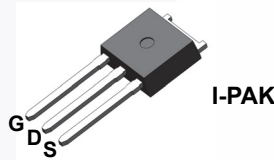
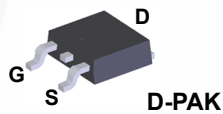
- $R_{DS(on)} = 1.05 \Omega$ (Typ.) @ $V_{GS} = 10 V, I_D = 2.75 A$
- Low Gate Charge (Typ. 13 nC)
- Low C_{rss} (Typ. 7 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Applications

- Lighting
- Uninterruptible Power Supply

Description

UniFET™ II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET™ II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FDD7N60NZTM/ FDU7N60NZTU	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	±25	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ C$)	5.5
		- Continuous ($T_C = 100^\circ C$)	3.3
I_{DM}	Drain Current	- Pulsed (Note 1)	22
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	347
I_{AR}	Avalanche Current	(Note 1)	5.5
E_{AR}	Repetitive Avalanche Energy	(Note 1)	12.5
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	10
P_D	Power Dissipation	($T_C = 25^\circ C$)	90
		- Derate Above $25^\circ C$	0.7
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	FDD7N60NZTM/ FDU7N60NZTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	90	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD7N60NZTM	FDD7N60NZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units
FDU7N60NZTU	FDU7N60NZ	IPAK	Tube	N/A	N/A	75 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$	600	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.6	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	50	μA
		$V_{DS} = 480 \text{ V}, T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.75 \text{ A}$	-	1.05	1.25	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 2.75 \text{ A}$	-	7.3	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	550	730	pF
C_{oss}	Output Capacitance		-	70	90	pF
C_{rSS}	Reverse Transfer Capacitance		-	7	10	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400 \text{ V}, I_D = 5.5 \text{ A}, V_{GS} = 10 \text{ V}$	-	13	17	nC
Q_{gs}	Gate to Source Gate Charge		-	3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	5.6	-

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250 \text{ V}, I_D = 5.5 \text{ A}, V_{GS} = 10 \text{ V}, R_G = 25 \Omega$	-	17.5	45	ns
t_r	Turn-On Rise Time		-	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		-	40	90	ns
t_f	Turn-Off Fall Time		(Note 4)	-	25	60

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	5.5	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	22	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 5.5 \text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 5.5 \text{ A}, di_F/dt = 100 \text{ A}/\mu\text{s}$	-	250	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.4	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 23 \text{ mH}, I_{AS} = 5.5 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 5.5 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

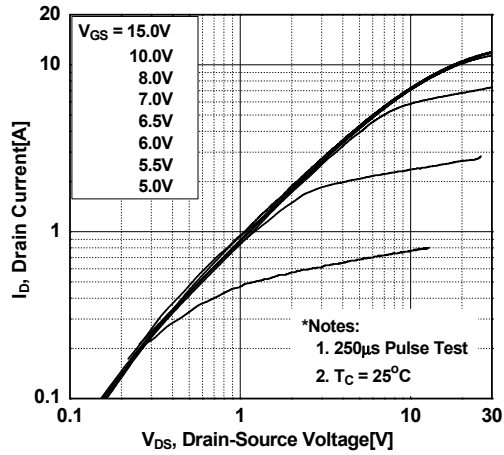


Figure 2. Transfer Characteristics

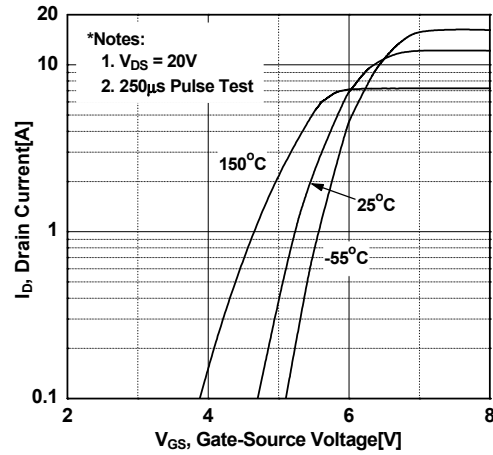


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

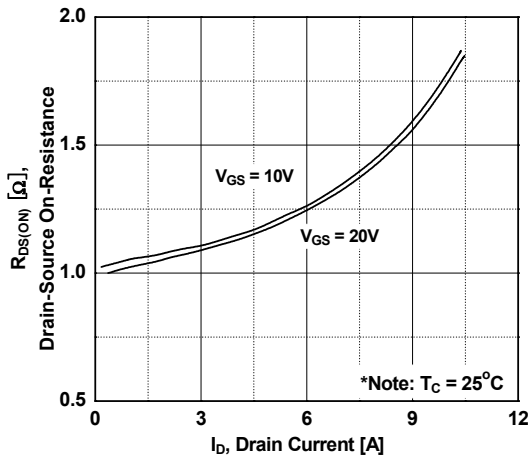


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

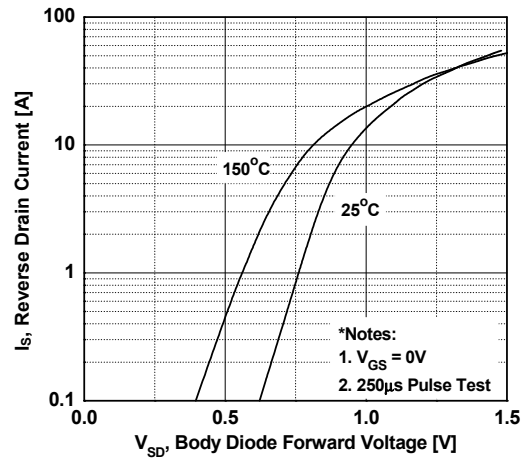


Figure 5. Capacitance Characteristics

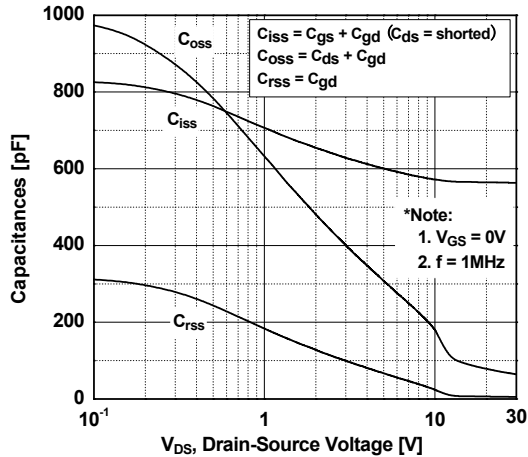
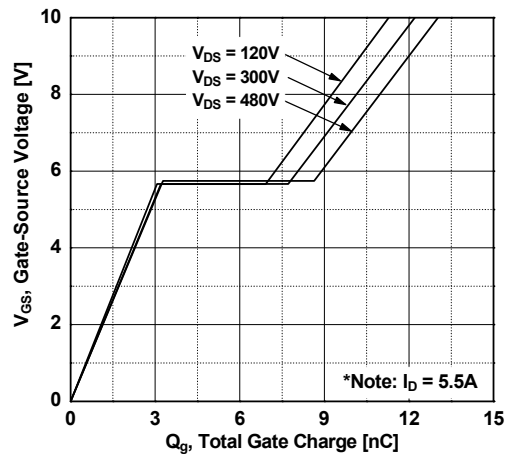


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

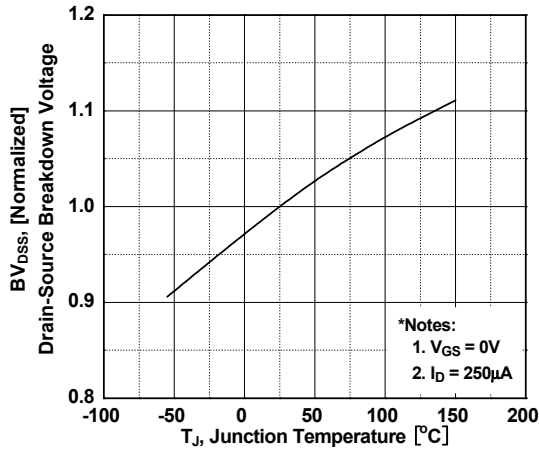


Figure 8. On-Resistance Variation vs. Temperature

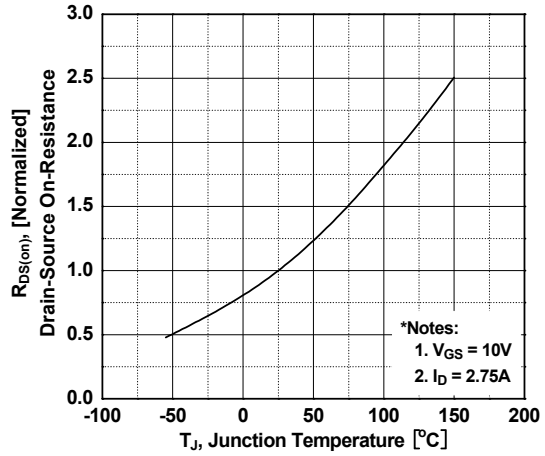


Figure 9. Maximum Safe Operating Area

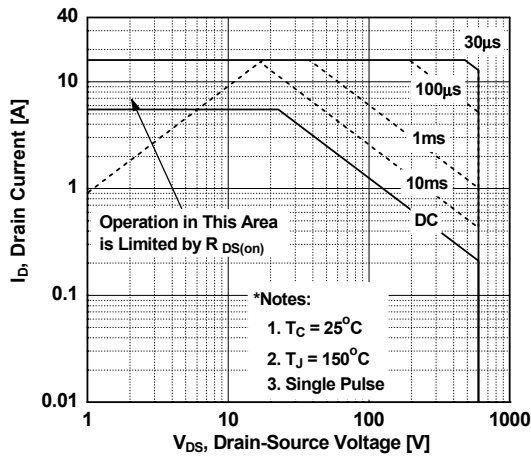


Figure 10. Maximum Drain Current vs. Case Temperature

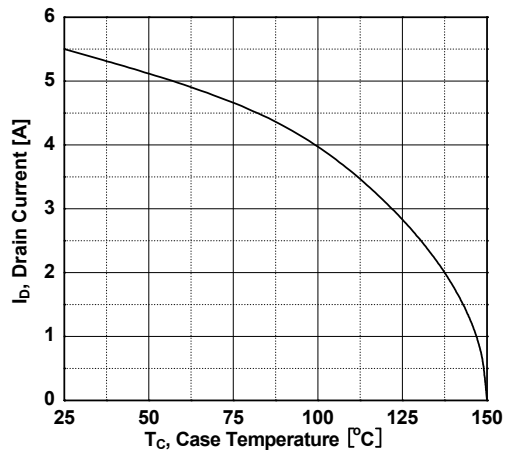
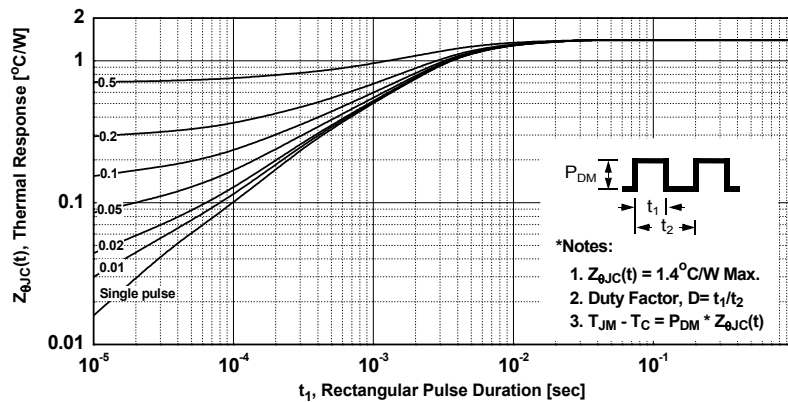


Figure 11. Transient Thermal Response Curve



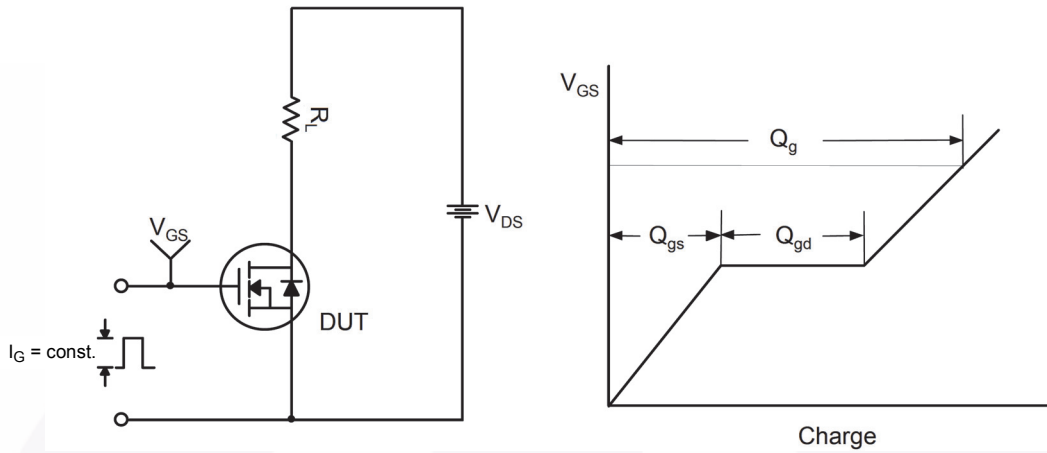


Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms



Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

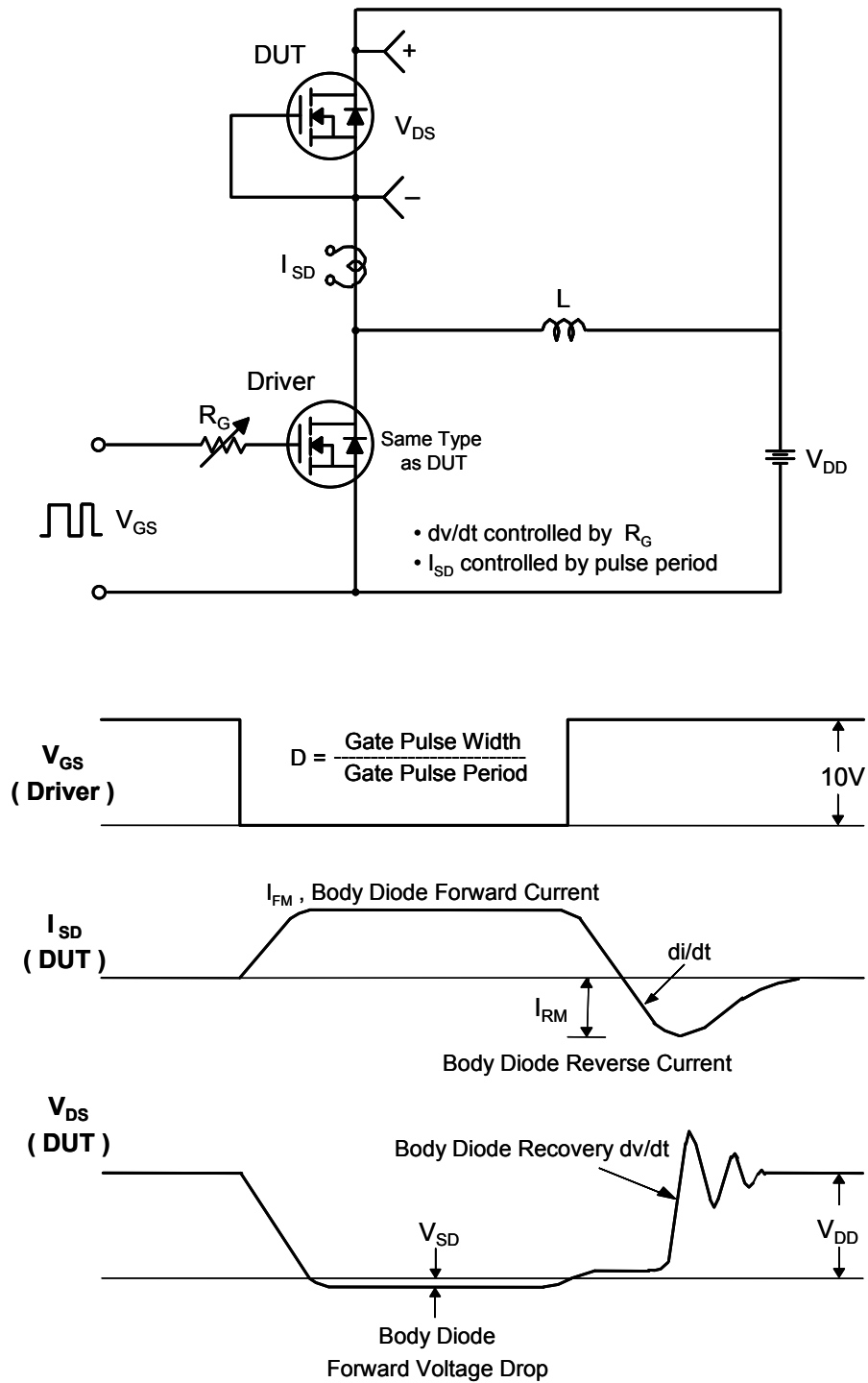
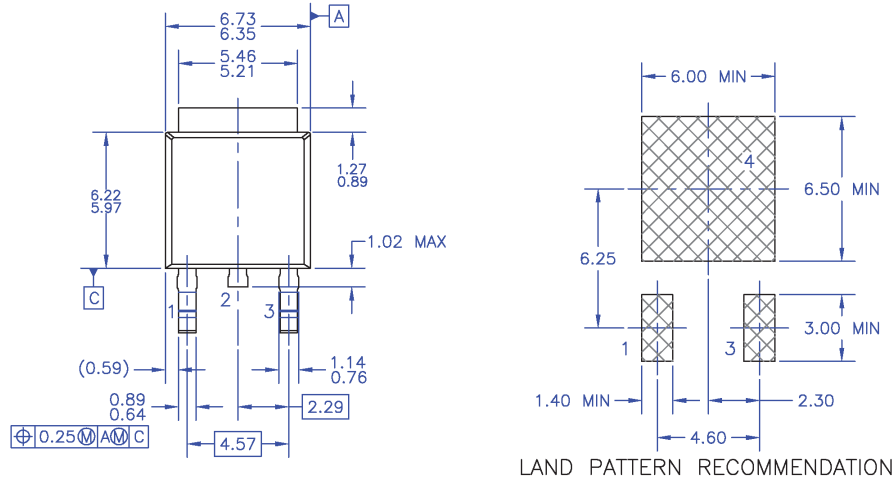


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT252-003

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor:](#)

[FDD7N60NZTM](#)