



# FDMC7680

## N-Channel Power Trench<sup>®</sup> MOSFET

30 V, 14.8 A, 7.2 mΩ

### Features

- Max  $r_{DS(on)}$  = 7.2 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 14.8\text{ A}$
- Max  $r_{DS(on)}$  = 9.5 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 12.4\text{ A}$
- High performance technology for extremely low  $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant



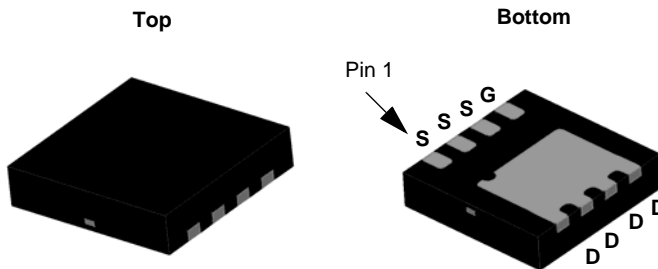
### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

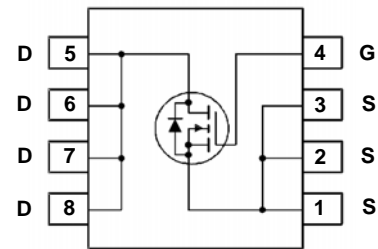
### Application

- DC - DC Buck Converters
- Notebook battery power management
- Load switch in Notebook

FDMC7680 N-Channel Power Trench<sup>®</sup> MOSFET



MLP 3.3x3.3



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$	A
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	
	-Pulsed		
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	mJ
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	W
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a) 53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7680	FDMC7680	MLP 3.3x3.3	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		15		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$ $T_J = 125\text{ }^\circ\text{C}$			1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.2	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 14.8\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 12.4\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 14.8\text{ A}$ $T_J = 125\text{ }^\circ\text{C}$		5.8 7.3 7.4	7.2 9.5 9.2	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}$ , $I_D = 14.8\text{ A}$		68		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		2145	2855	pF
$C_{oss}$	Output Capacitance			770	1020	pF
$C_{rss}$	Reverse Transfer Capacitance			75	115	pF
$R_g$	Gate Resistance			0.5	1.6	$\Omega$

### Switching Characteristics

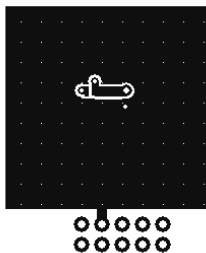
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 14.8\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		12	22	ns
$t_r$	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			25	40	ns
$t_f$	Fall Time			3	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		30	42
	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	$V_{DD} = 15\text{ V}$ $I_D = 14.8\text{ A}$	14	19	nC
$Q_{gs}$	Total Gate Charge			7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			4		nC

### Drain-Source Diode Characteristics

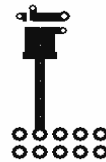
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 14.8\text{ A}$ (Note 2)		0.84	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 1.9\text{ A}$ (Note 2)		0.73	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 14.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		34	54	ns
$Q_{rr}$	Reverse Recovery Charge			15	24	nC

#### NOTES:

1:  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $53\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b.  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3:  $E_{AS}$  of 72 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 12\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

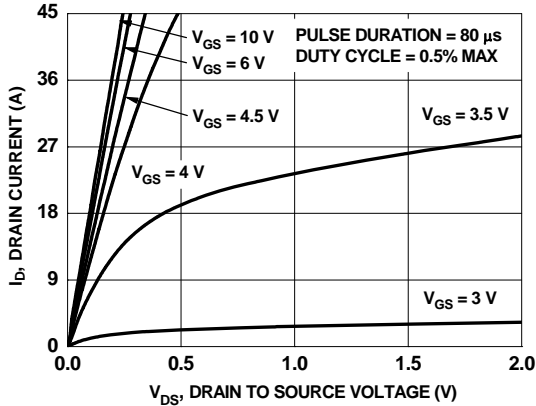


Figure 1. On-Region Characteristics

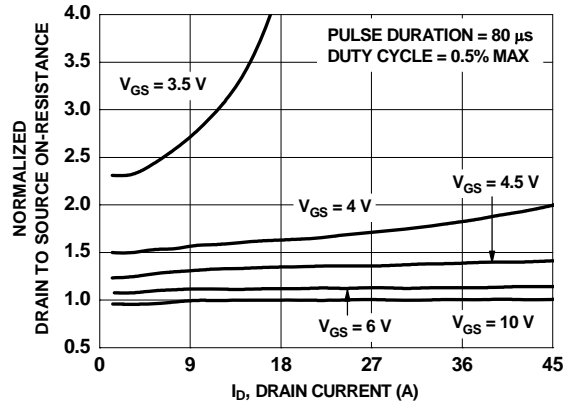


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

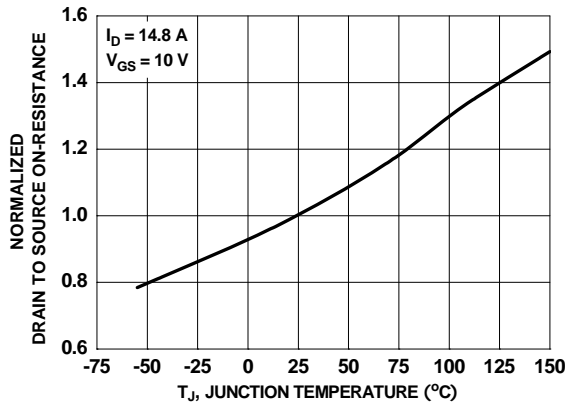


Figure 3. Normalized On-Resistance vs. Junction Temperature

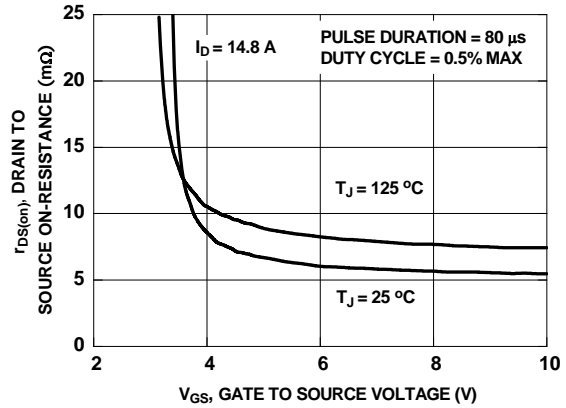


Figure 4. On-Resistance vs. Gate to Source Voltage

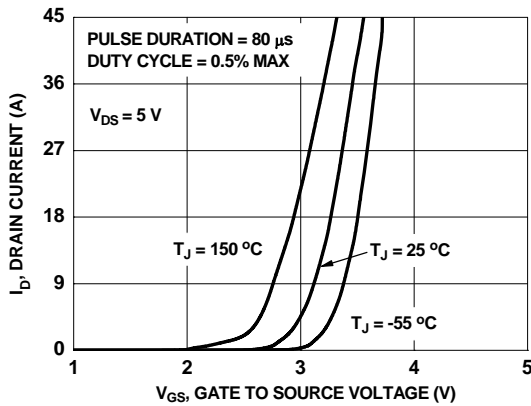


Figure 5. Transfer Characteristics

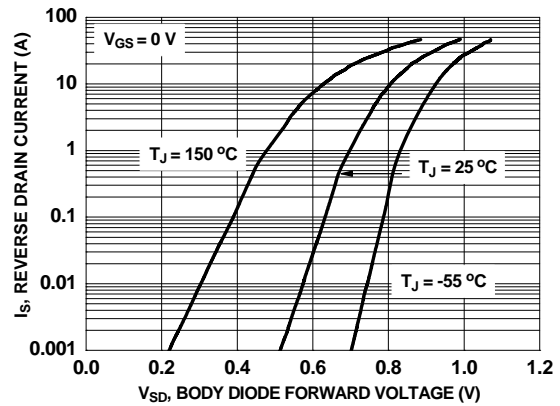
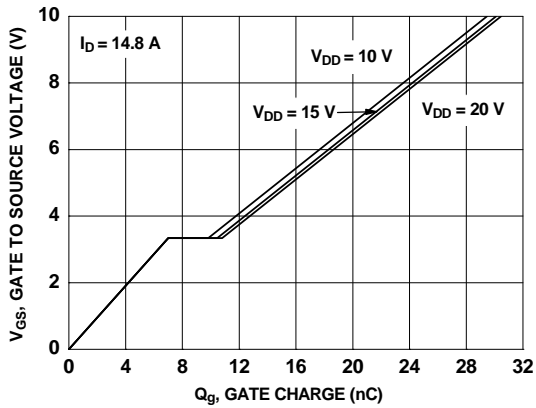
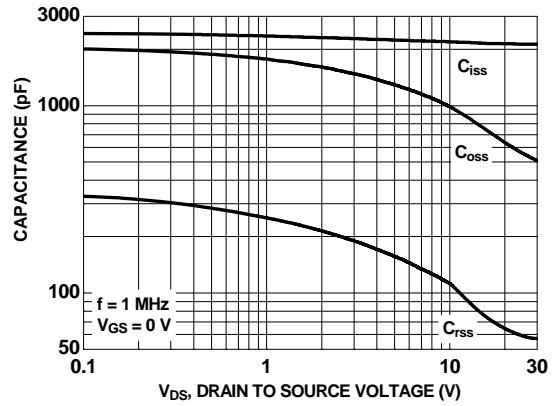


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

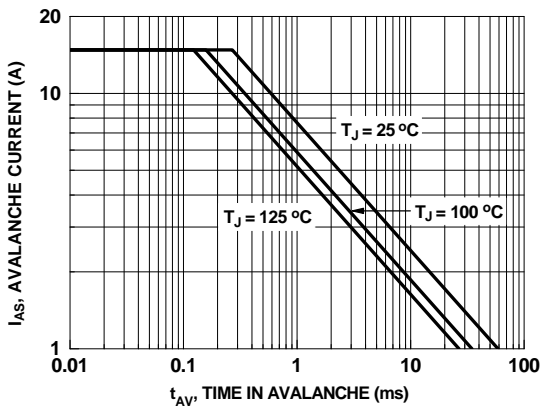
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



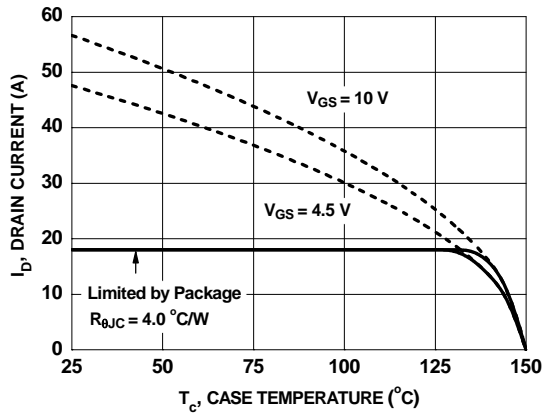
**Figure 7. Gate Charge Characteristics**



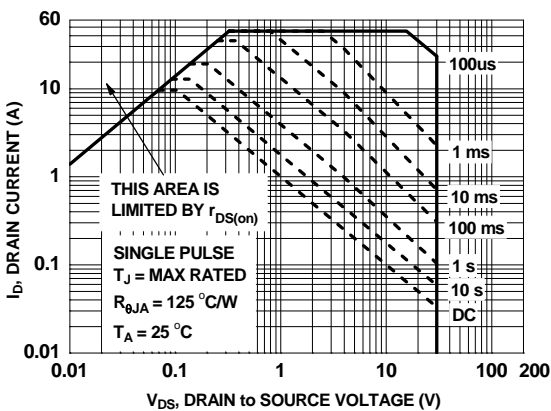
**Figure 8. Capacitance vs. Drain to Source Voltage**



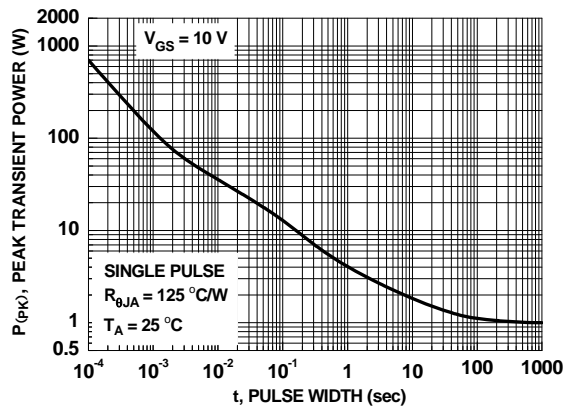
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

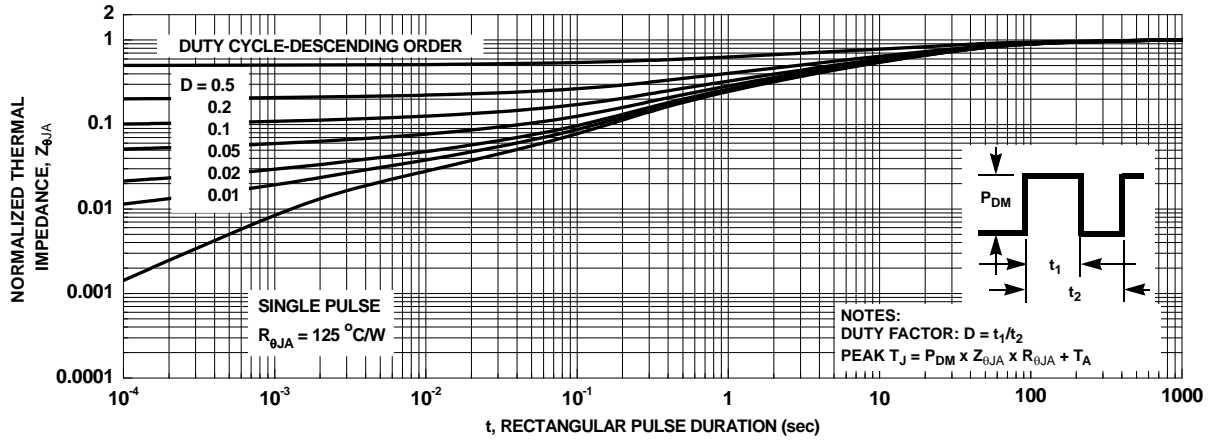


**Figure 11. Forward Bias Safe Operating Area**



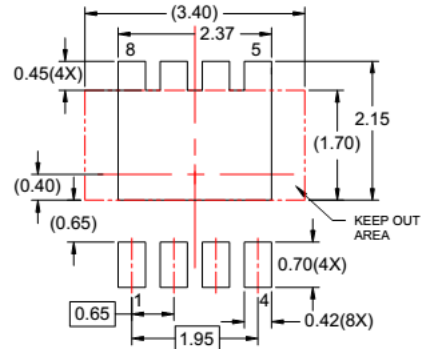
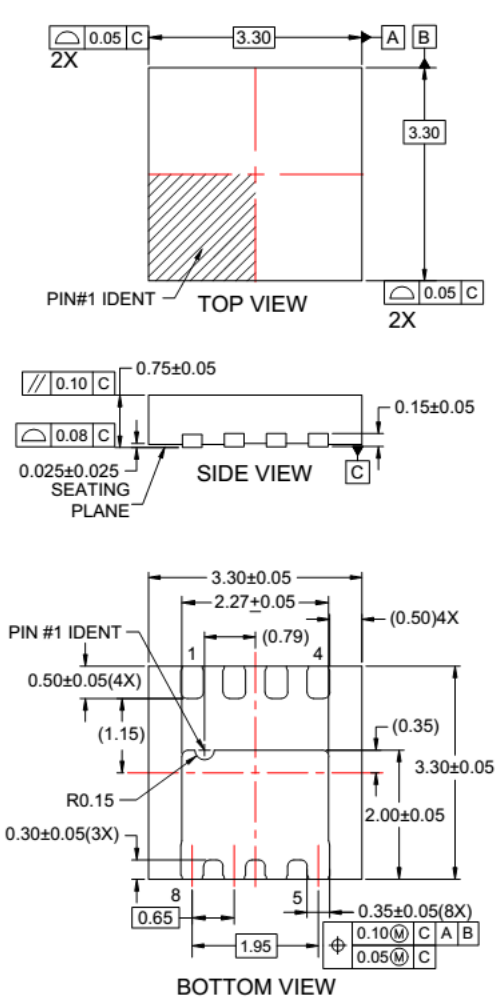
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN

### NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.








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