

# FDMC86259P

## P-Channel PowerTrench® MOSFET

-150 V, -13 A, 107 mΩ

### Features

- Max  $r_{DS(on)}$  = 107 mΩ at  $V_{GS} = -10$  V,  $I_D = -3$  A
- Max  $r_{DS(on)}$  = 137 mΩ at  $V_{GS} = -6$  V,  $I_D = -2.7$  A
- Very low RDS-on mid voltage P channel silicon technology optimised for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL Tested
- RoHS Compliant

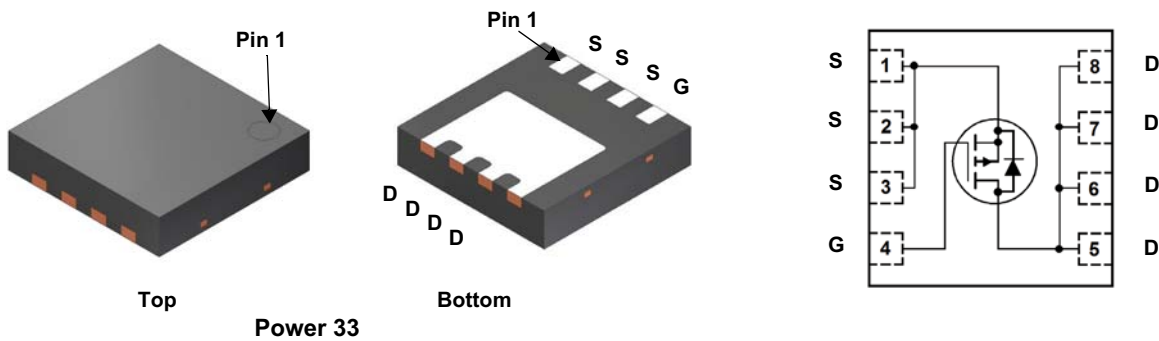


### General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Applications

- Active Clamp Switch
- Load Switch



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-150	V
$V_{GS}$	Gate to Source Voltage	±25	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	-13	A
	-Continuous $T_A = 25$ °C (Note 1a)	-3.2	
	-Pulsed	-20	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	181	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	62	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to + 150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86259P	FDMC86259P	Power 33	13"	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-88		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -120\ \text{V}, V_{GS} = 0\ \text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-2	-2.8	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\ \text{V}, I_D = -3\ \text{A}$		87	107	m $\Omega$
		$V_{GS} = -6\ \text{V}, I_D = -2.7\ \text{A}$		99	137	
		$V_{GS} = -10\ \text{V}, I_D = -3\ \text{A}, T_J = 125^\circ\text{C}$		145	178	
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\ \text{V}, I_D = -3\ \text{A}$		12		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -75\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		1535	2045	pF
$C_{oss}$	Output Capacitance			125	170	pF
$C_{rss}$	Reverse Transfer Capacitance			6	10	pF
$R_g$	Gate Resistance		0.1	1.4	3	$\Omega$

### Switching Characteristics

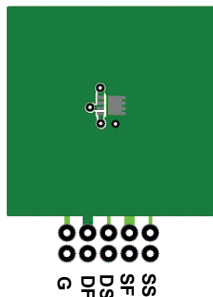
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -75\ \text{V}, I_D = -3\ \text{A}, V_{GS} = -10\ \text{V}, R_{GEN} = 6\ \Omega$		12	23	ns	
$t_r$	Rise Time			3.3	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			22	36	ns	
$t_f$	Fall Time			9.6	20	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V to } -10\ \text{V}$		22	32	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V to } -6\ \text{V}$	$V_{DD} = -75\ \text{V}, I_D = -3\ \text{A}$		14	20	nC
$Q_{gs}$	Total Gate Charge				5.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				4.3		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = -3\ \text{A}$ (Note 2)		-0.80	-1.3	V
		$V_{GS} = 0\ \text{V}, I_S = -1.9\ \text{A}$ (Note 2)		-0.78	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -3\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		77	123	ns
$Q_{rr}$	Reverse Recovery Charge			208	333	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 53  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper

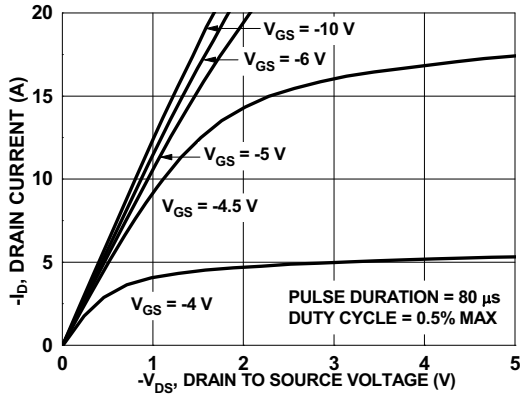


b) 125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

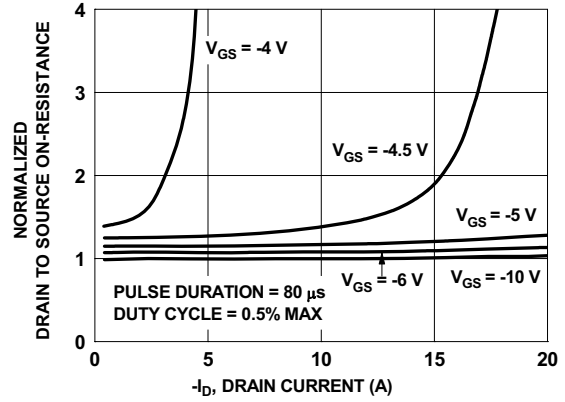
2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25^\circ\text{C}$ ; P-ch: L = 3 mH,  $I_{AS} = -11\ \text{A}$ ,  $V_{DD} = -150\ \text{V}$ ,  $V_{GS} = -10\ \text{V}$ . 100% test at L = 0.1 mH,  $I_{AS} = -34\ \text{A}$ .

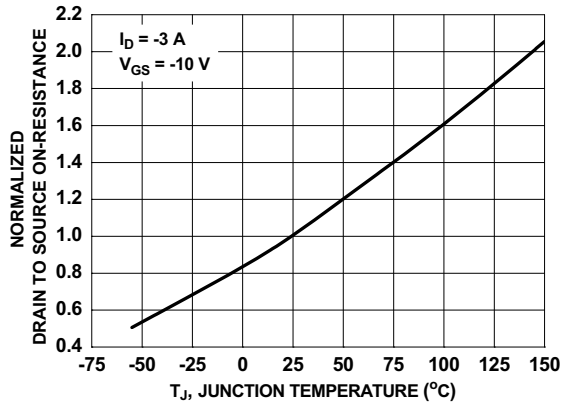
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



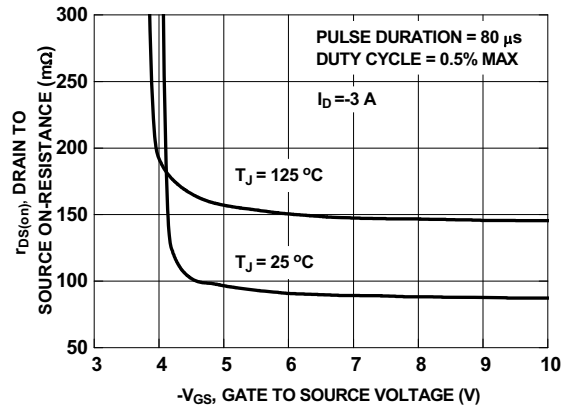
**Figure 1. On Region Characteristics**



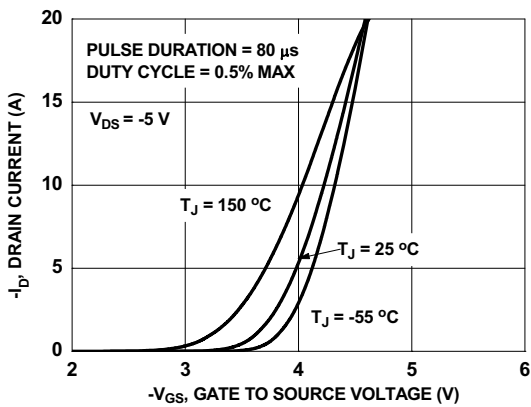
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



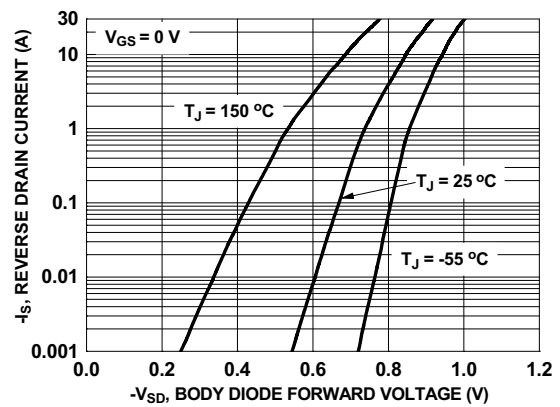
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

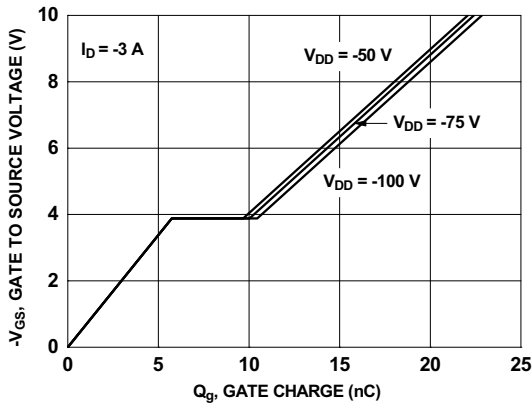


**Figure 5. Transfer Characteristics**

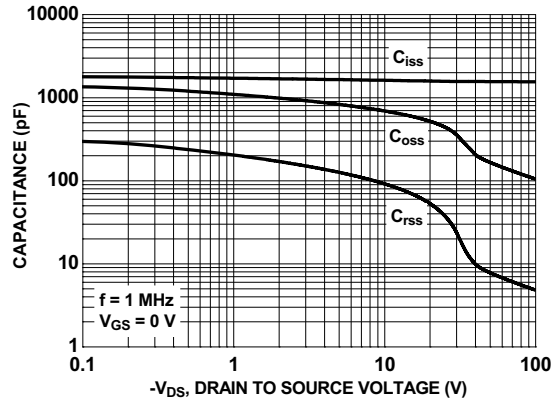


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

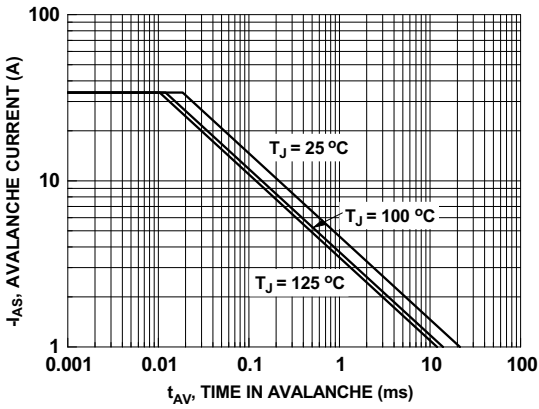
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



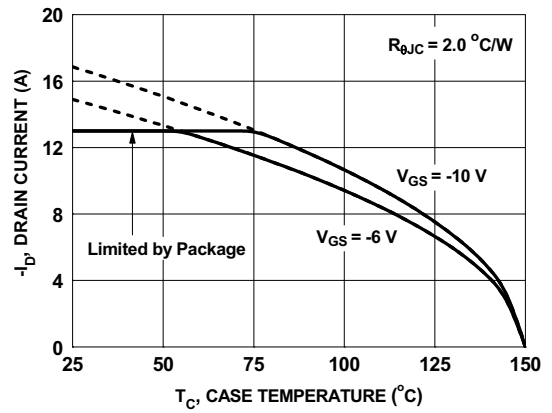
**Figure 7. Gate Charge Characteristics**



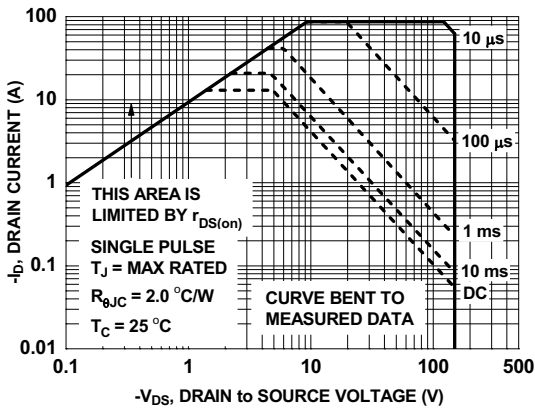
**Figure 8. Capacitance vs Drain to Source Voltage**



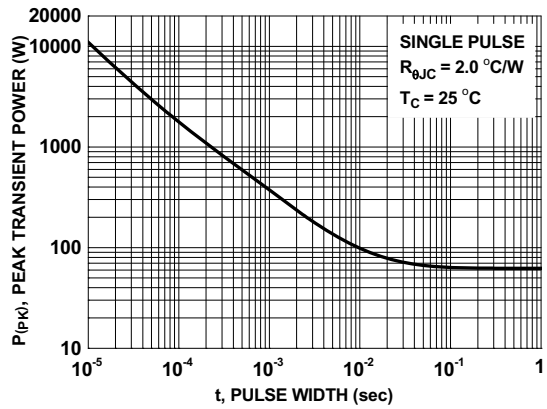
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**



**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

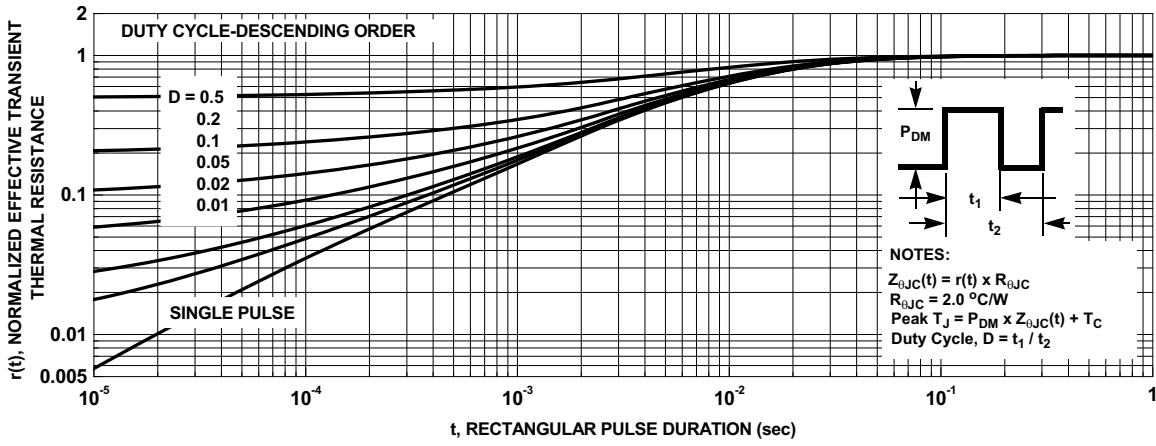
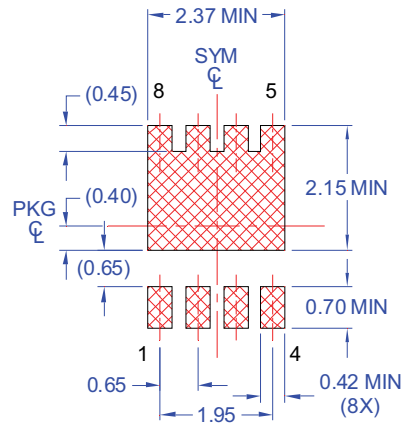
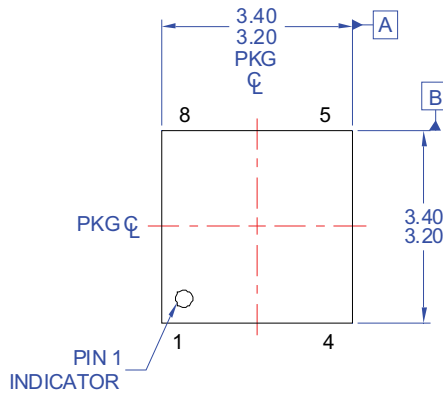
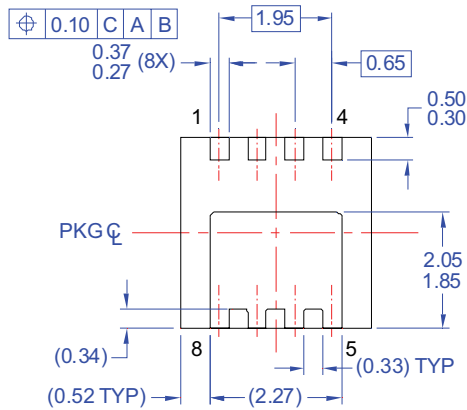
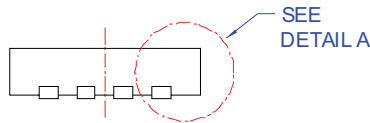


Figure 13. Junction-to-Case Transient Thermal Response Curve

## Dimensional Outline and Pad Layout

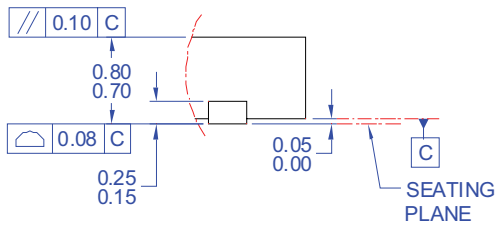


LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08HREV1



DETAIL A  
SCALE: 2X





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| BitSiC™  | Global Power ResourceSM                         | Programmable Active Droop™  | TinyBoost®   |
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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