



FDMS7556S

N-Channel PowerTrench[®] SyncFET[™] 25 V, 130 A, 1.2 mΩ

Features

- Max $r_{DS(on)}$ = 1.2 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 35\text{ A}$
- Max $r_{DS(on)}$ = 1.65 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 31\text{ A}$
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- SyncFET Schottky Body Diode
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

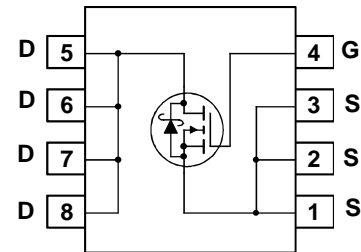
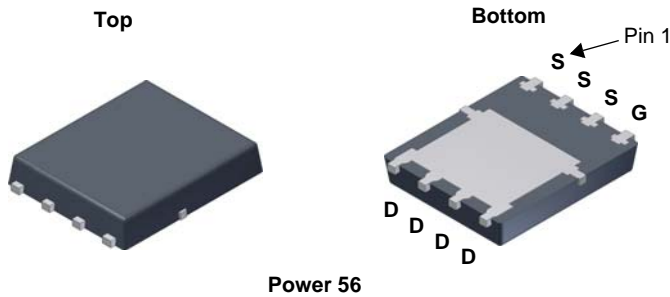


General Description

The FDMS7556S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Applications

- Synchronous Rectifier for Synchronous Buck Converters
- Notebook
- Server
- Telecom
- High Efficiency DC-DC Switch Mode Power Supplies



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$	130	A
	-Continuous (Silicon limited) $T_C = 25\text{ °C}$	222	
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	35	
	-Pulsed	200	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	312	mJ
P_D	Power Dissipation $T_C = 25\text{ °C}$	96	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7556S	FDMS7556S	Power 56	13"	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$		22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$	1.2	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 35\text{ A}$		0.95	1.2	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 31\text{ A}$		1.3	1.65	
		$V_{GS} = 10\text{ V}, I_D = 35\text{ A}, T_J = 125\text{ }^\circ\text{C}$		1.2	1.6	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 35\text{ A}$		212		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		6740	8965	pF
C_{oss}	Output Capacitance			1940	2580	pF
C_{rss}	Reverse Transfer Capacitance			314	475	pF
R_g	Gate Resistance			0.6	1.3	Ω

Switching Characteristics

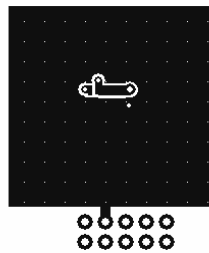
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{ V}, I_D = 35\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		20	36	ns	
t_r	Rise Time			9	18	ns	
$t_{d(off)}$	Turn-Off Delay Time			48	77	ns	
t_f	Fall Time			5.3	11	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 13\text{ V}$ $I_D = 35\text{ A}$	95	133	nC
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to }4.5\text{ V}$		43	60	nC
Q_{gs}	Gate to Source Gate Charge		18.6			nC	
Q_{gd}	Gate to Drain "Miller" Charge		8.8			nC	

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.37	0.7	V
		$V_{GS} = 0\text{ V}, I_S = 35\text{ A}$ (Note 2)		0.74	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 35\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		44	71	ns
Q_{rr}	Reverse Recovery Charge			68	109	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. E_{AS} of 312 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 25\text{ A}$, $V_{DD} = 23\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.3\text{ mH}$, $I_{AS} = 38\text{ A}$.

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

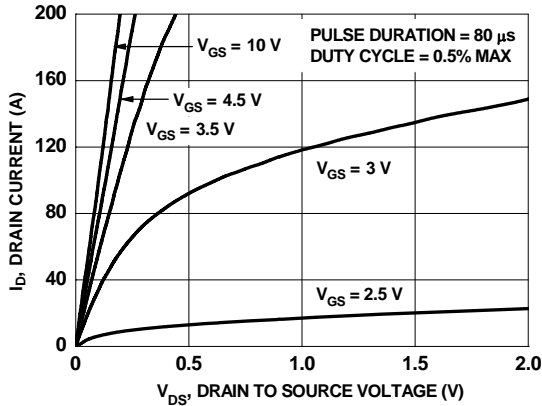


Figure 1. On-Region Characteristics

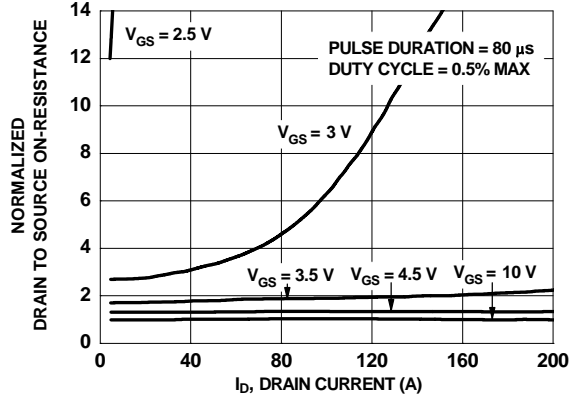


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

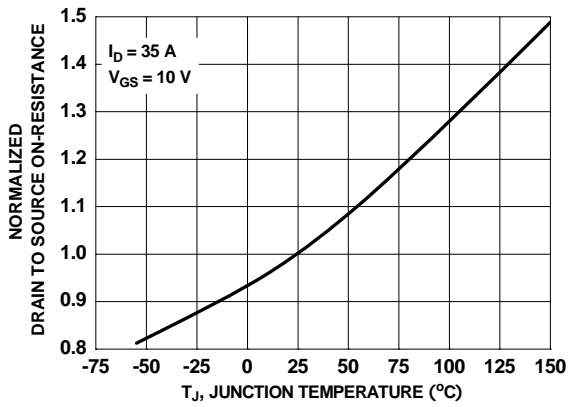


Figure 3. Normalized On-Resistance vs Junction Temperature

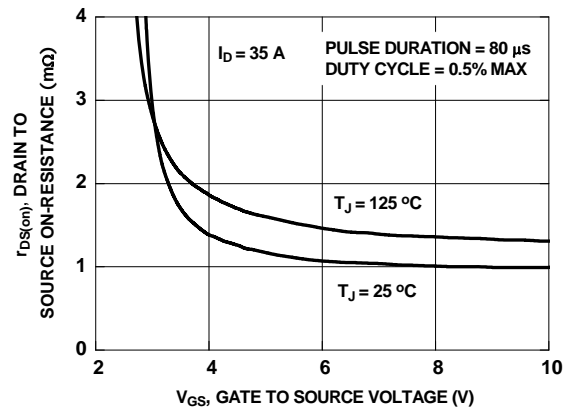


Figure 4. On-Resistance vs Gate to Source Voltage

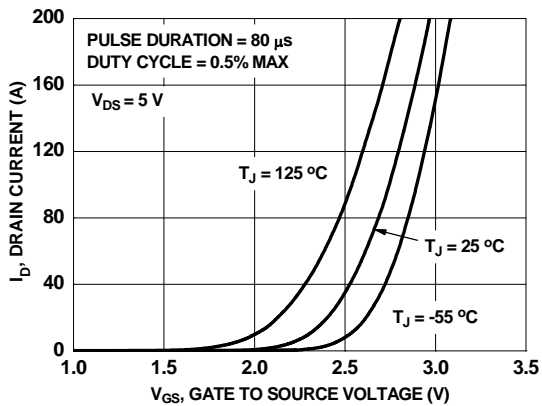


Figure 5. Transfer Characteristics

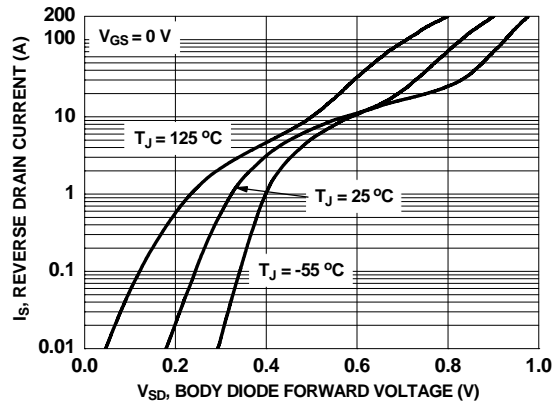


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

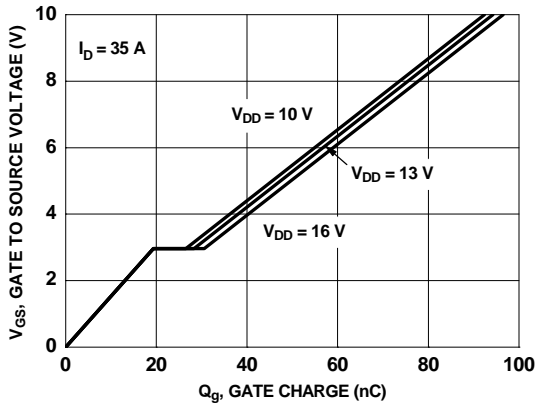


Figure 7. Gate Charge Characteristics

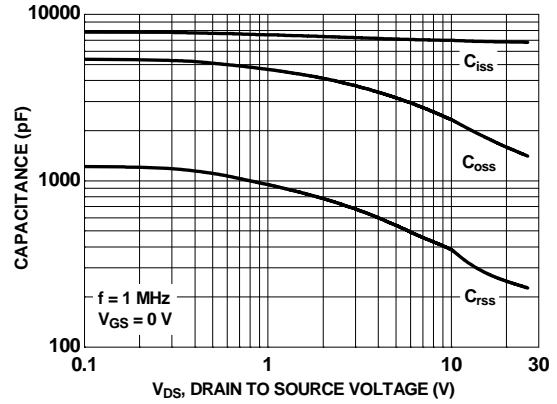


Figure 8. Capacitance vs Drain to Source Voltage

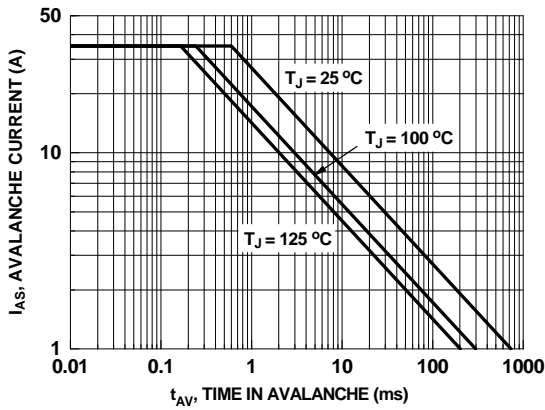


Figure 9. Unclamped Inductive Switching Capability

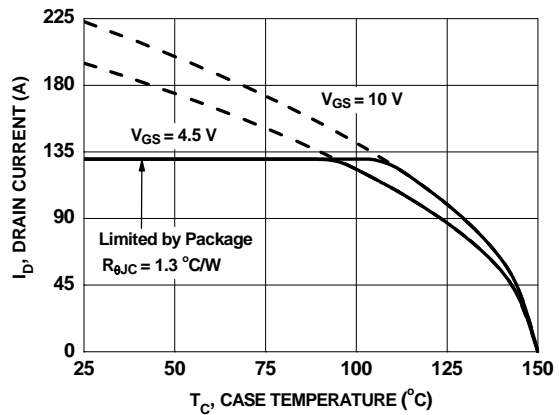


Figure 10. Maximum Continuous Drain Current vs Case Temperature

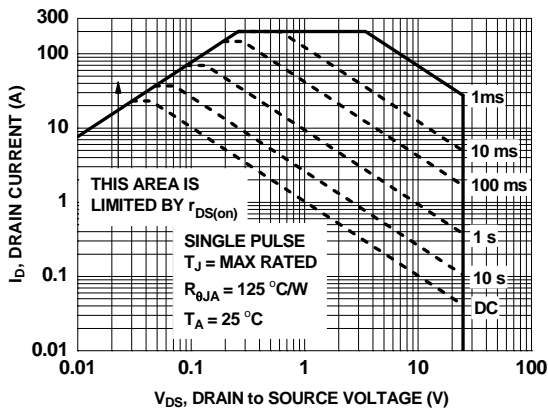


Figure 11. Forward Bias Safe Operating Area

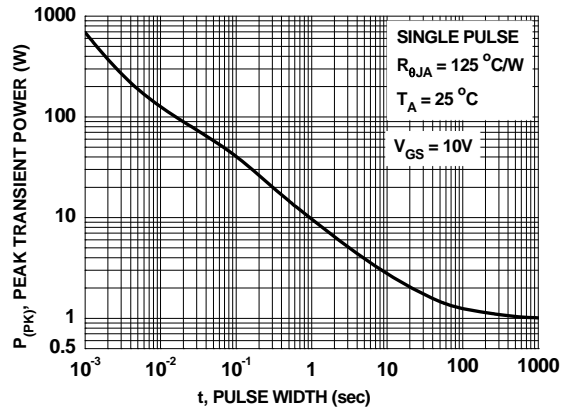
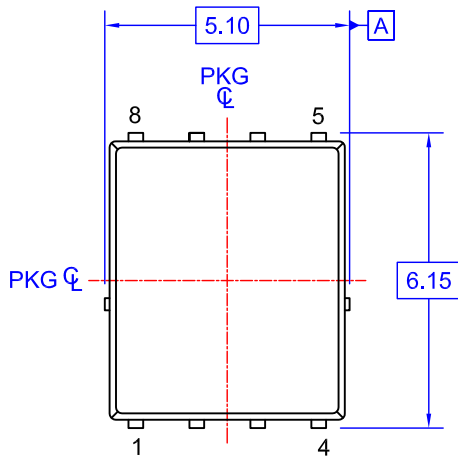
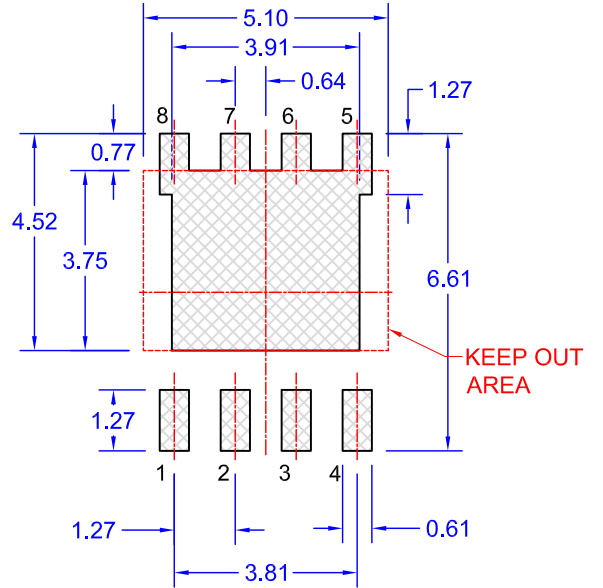
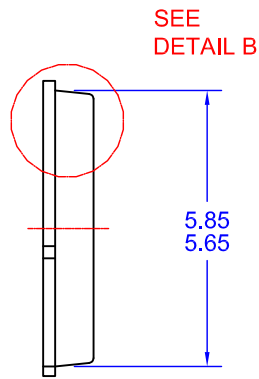


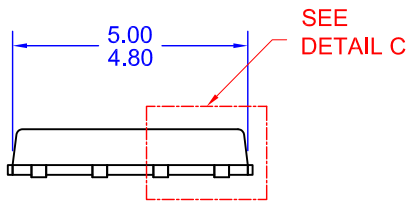
Figure 12. Single Pulse Maximum Power Dissipation



TOP VIEW

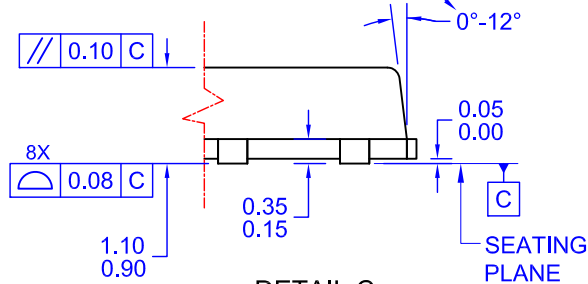


LAND PATTERN RECOMMENDATION

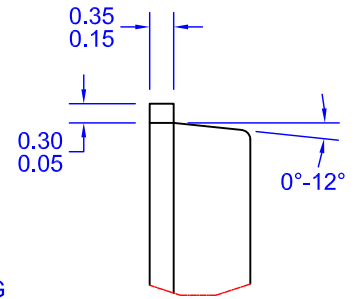


SIDE VIEW

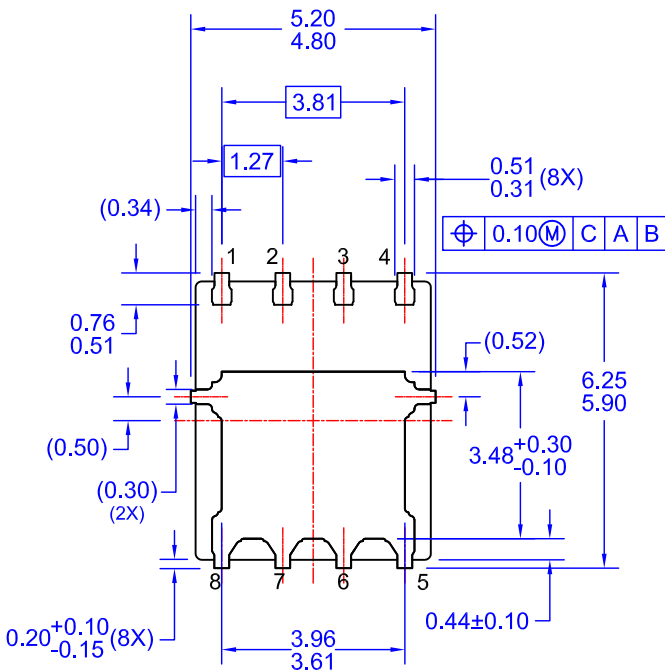
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV10





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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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