



# FDMS86152

## N-Channel PowerTrench<sup>®</sup> MOSFET

100 V, 45 A, 6 mΩ

### Features

- Max  $r_{DS(on)}$  = 6 mΩ at  $V_{GS} = 10$  V,  $I_D = 14$  A
- Max  $r_{DS(on)}$  = 11 mΩ at  $V_{GS} = 6$  V,  $I_D = 11.5$  A
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

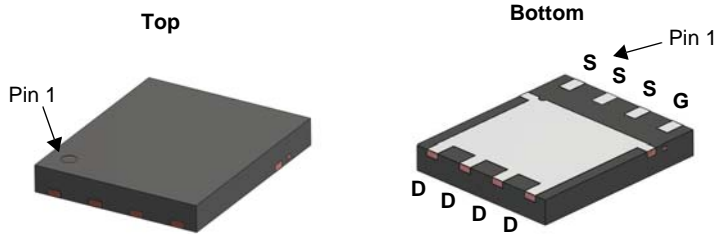


### General Description

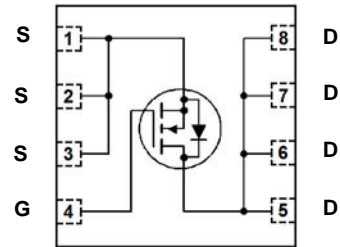
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Applications

- Primary DC-DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch



Power 56



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Conditions	Rated Value	Units
$V_{DS}$	Drain to Source Voltage		100	V
$V_{GS}$	Gate to Source Voltage		±20	V
$I_D$	Drain Current	-Continuous $T_C = 25$ °C	45	A
		-Continuous $T_A = 25$ °C (Note 1a)	14	
		-Pulsed	260	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	541	mJ
$P_D$	Power Dissipation	$T_C = 25$ °C	125	W
		$T_A = 25$ °C (Note 1a)	2.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	45	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86152	FDMS86152	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		90		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-10		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 14\text{ A}$		5.2	6	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 11.5\text{ A}$		7.3	11	
		$V_{GS} = 10\text{ V}$ , $I_D = 14\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		8.7	10	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 14\text{ A}$		42		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		2530	3370	pF
$C_{oss}$	Output Capacitance			595	795	pF
$C_{rss}$	Reverse Transfer Capacitance			22	35	pF
$R_g$	Gate Resistance			0.9		$\Omega$

### Switching Characteristics

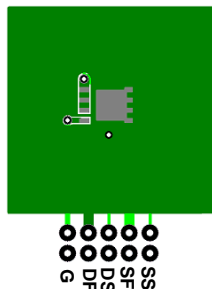
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$ , $I_D = 14\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		17	30	ns	
$t_r$	Rise Time			6	12	ns	
$t_{d(off)}$	Turn-Off Delay Time			25	39	ns	
$t_f$	Fall Time			5	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		36	50	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 6\text{ V}$	$V_{DD} = 50\text{ V}$ , $I_D = 14\text{ A}$		23	33	nC
$Q_{gs}$	Gate to Source Charge				10.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				7.2		nC

### Drain-Source Diode Characteristics

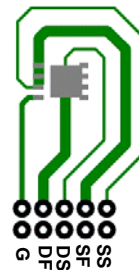
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$ (Note 2)		0.70	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 14\text{ A}$ (Note 2)		0.78	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 14\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		59	94	ns
$Q_{rr}$	Reverse Recovery Charge			74	119	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $45\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



b.  $115\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 19\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 42\text{ A}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

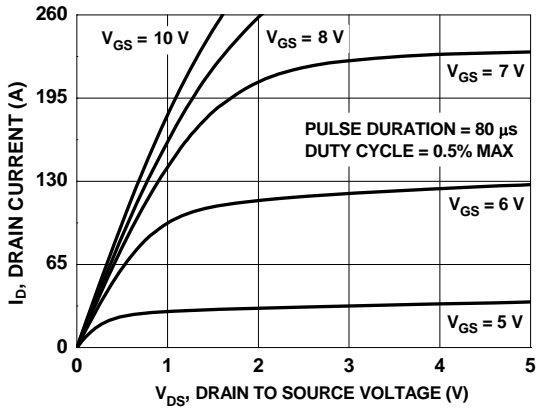


Figure 1. On-Region Characteristics

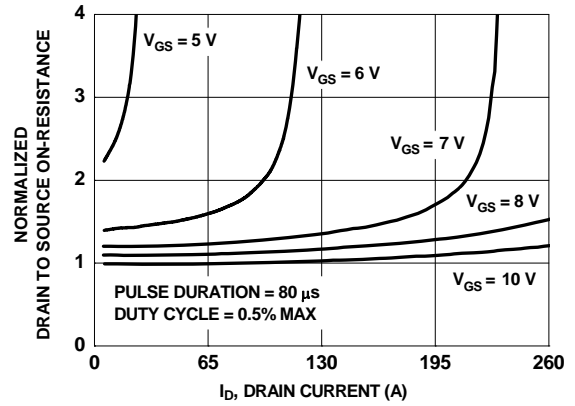


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

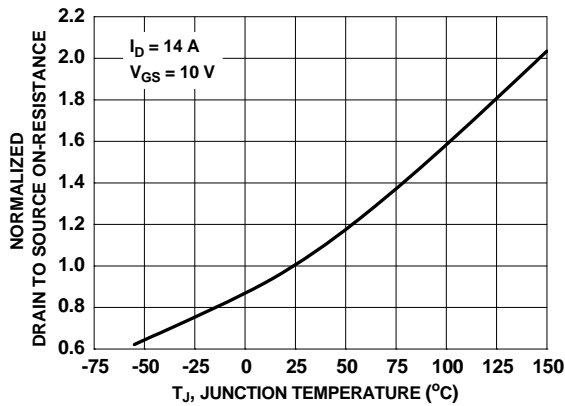


Figure 3. Normalized On-Resistance vs Junction Temperature

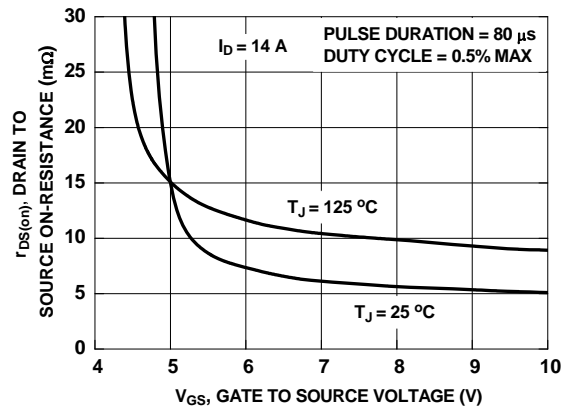


Figure 4. On-Resistance vs Gate to Source Voltage

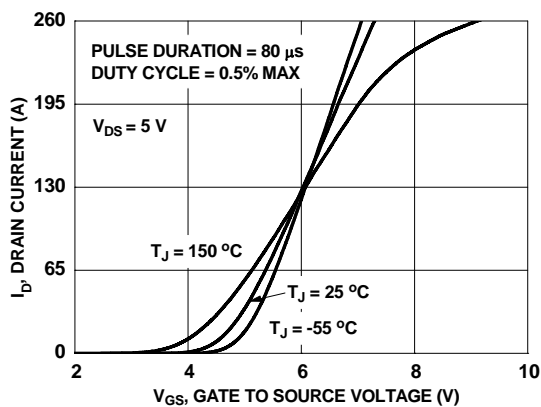


Figure 5. Transfer Characteristics

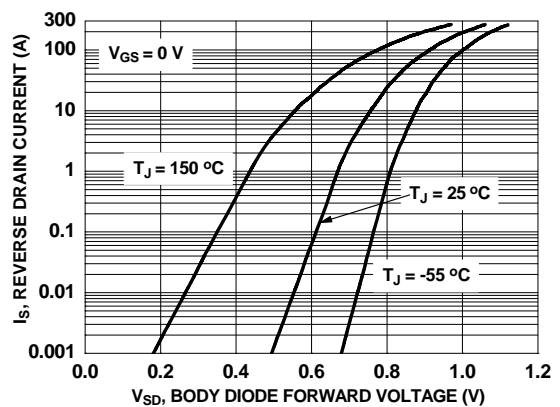
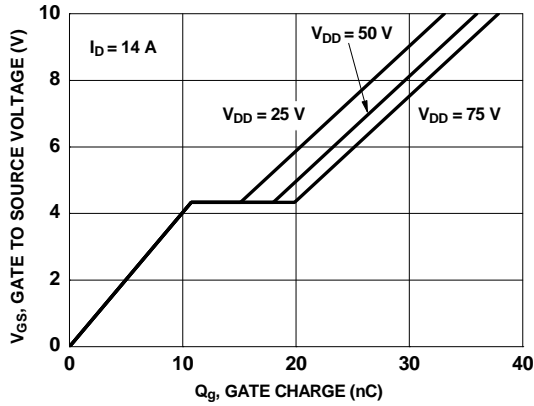
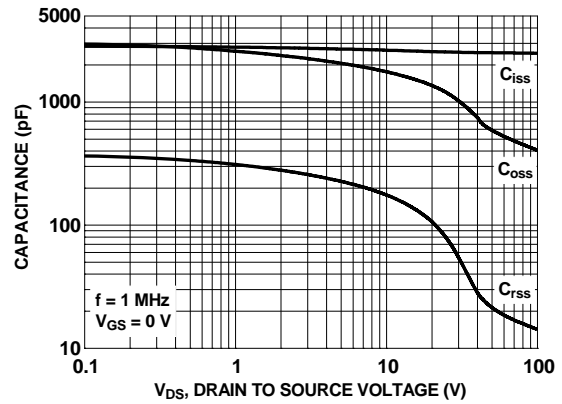


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

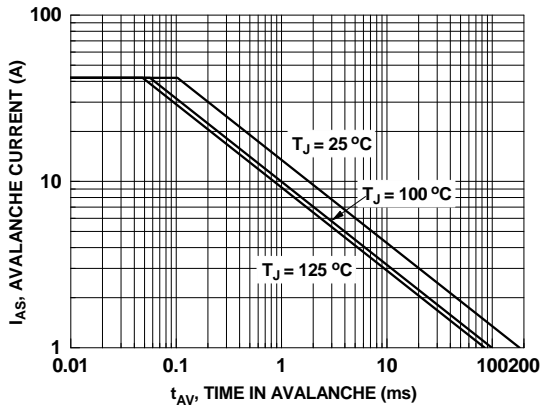
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



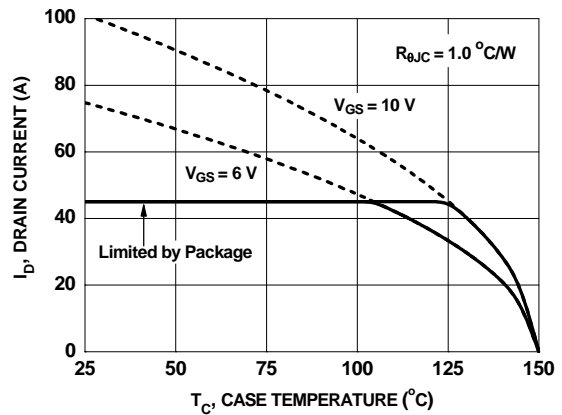
**Figure 7. Gate Charge Characteristics**



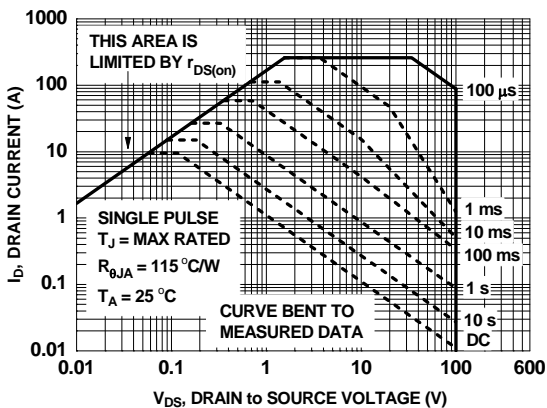
**Figure 8. Capacitance vs Drain to Source Voltage**



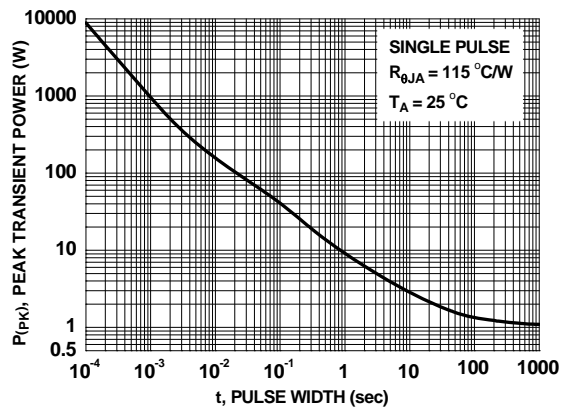
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

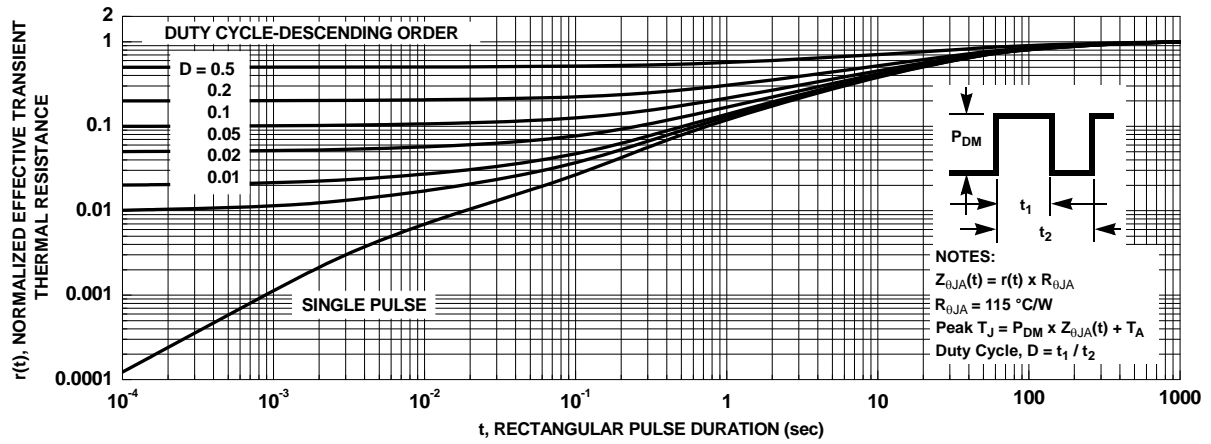


**Figure 11. Forward Bias Safe Operating Area**

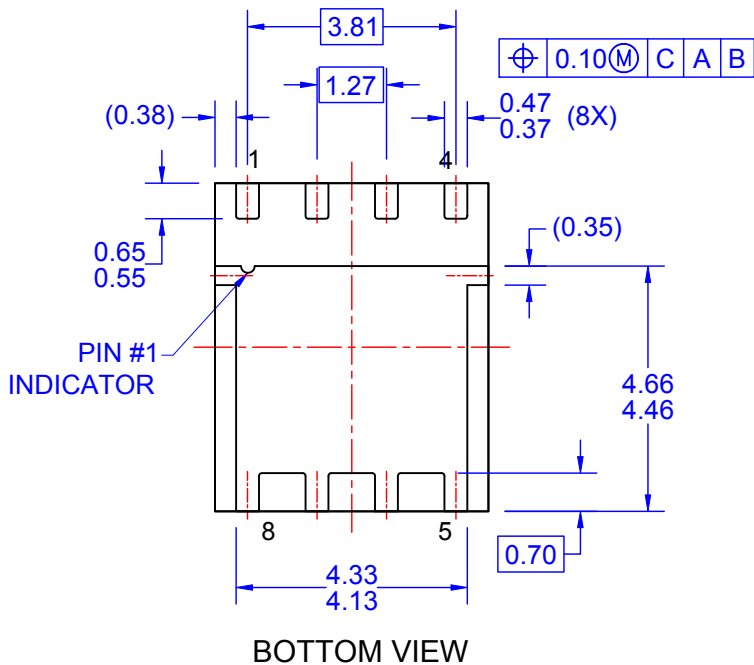
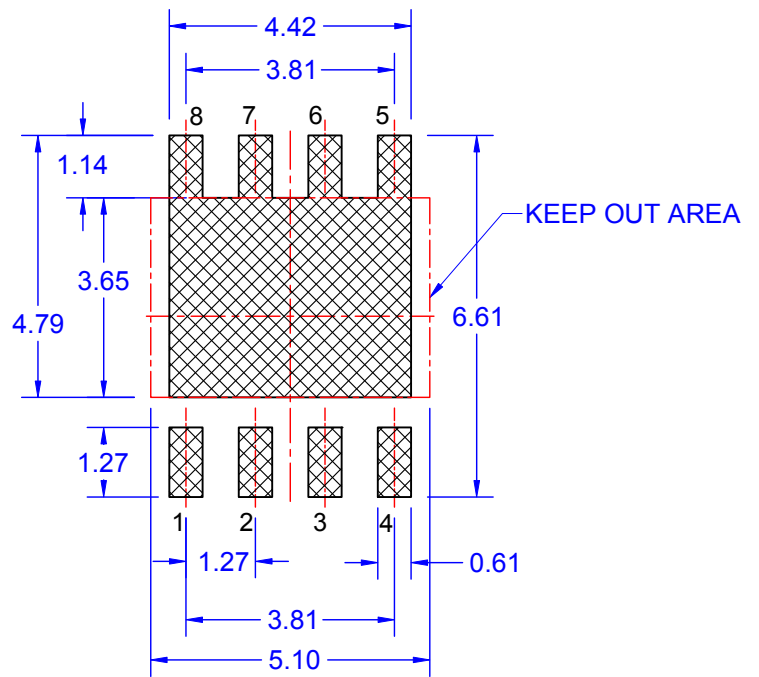
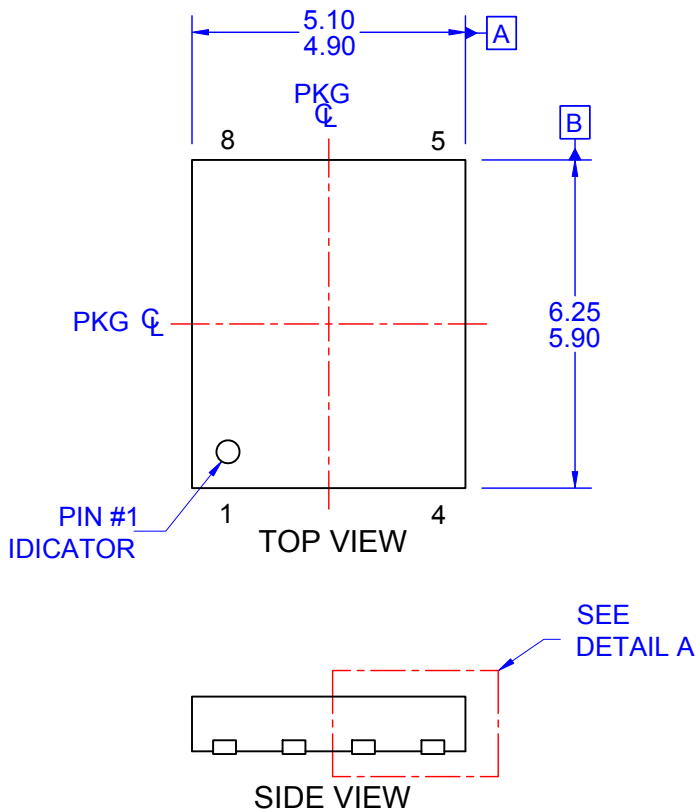


**Figure 12. Single Pulse Maximum Power Dissipation**

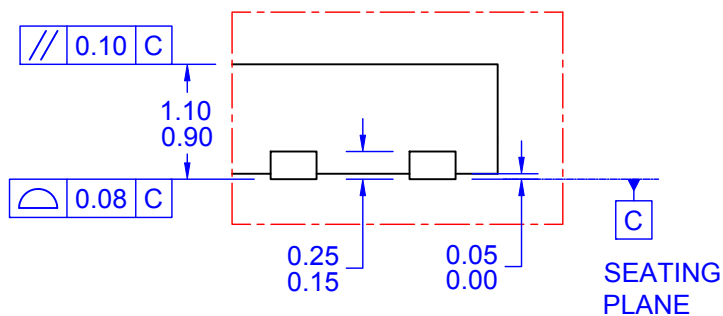
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: PQFN08JREV3.







**DETAIL A**  
SCALE: 2:1





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- ™
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- STEALTH™
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- SuperSOT™-6
- SuperSOT™-8
- SupreMOS®
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- TinyBoost®
- TinyBuck®
- TinyCalc™
- TinyLogic®
- TINYOPTO™
- TinyPower™
- TinyPWM™
- TinyWire™
- TranSiC™
- TriFault Detect™
- TRUECURRENT®\*
- μSerDes™
- ™
- UHC®
- Ultra FRFET™
- UniFET™
- VcX™
- VisualMax™
- VoltagePlus™
- XS™
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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