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FSBF10CH60B

Motion SPM® 3 Series

Features

- UL Certified No. E209204 (UL1557)
- 600 V - 10 A 3-Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low-Loss, Short-Circuit Rated IGBTs
- Built-In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply
- Isolation Rating: 2500 V_{rms} / min.

Applications

- Motion Control - Home Appliance / Industrial Motor

Related Resources

- [AN-9044 - Motion SPM® 3 Series Users Guide](#)

General Description

FSBF10CH60B is an advanced Motion SPM® 3 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

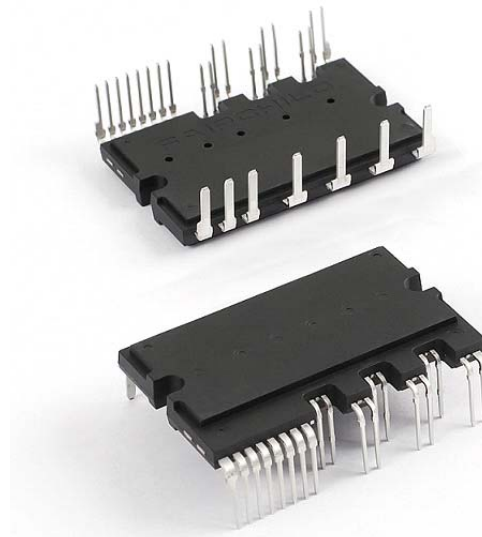


Figure 1. Package Overview

Package Marking and Ordering Information

| Device | Device Marking | Package | Packing Type | Quantity |
|-------------|----------------|-----------|--------------|----------|
| FSBF10CH60B | FSBF10CH60B | SPMJA-027 | RAIL | 10 |

Integrated Power Functions

- 600 V - 10 A IGBT inverter for three-phase DC / AC power conversion (please refer to Figure 3)

Integrated Drive, Protection, and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting control circuit Under-Voltage Lock-Out Protection (UVLO)
 Note: Available bootstrap circuit example is given in Figures 12 and 13.
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP) control supply circuit Under-Voltage Lock-Out Protection (UVLO)
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: active-HIGH interface, works with 3.3 / 5 V logic, Schmitt-trigger input

Pin Configuration

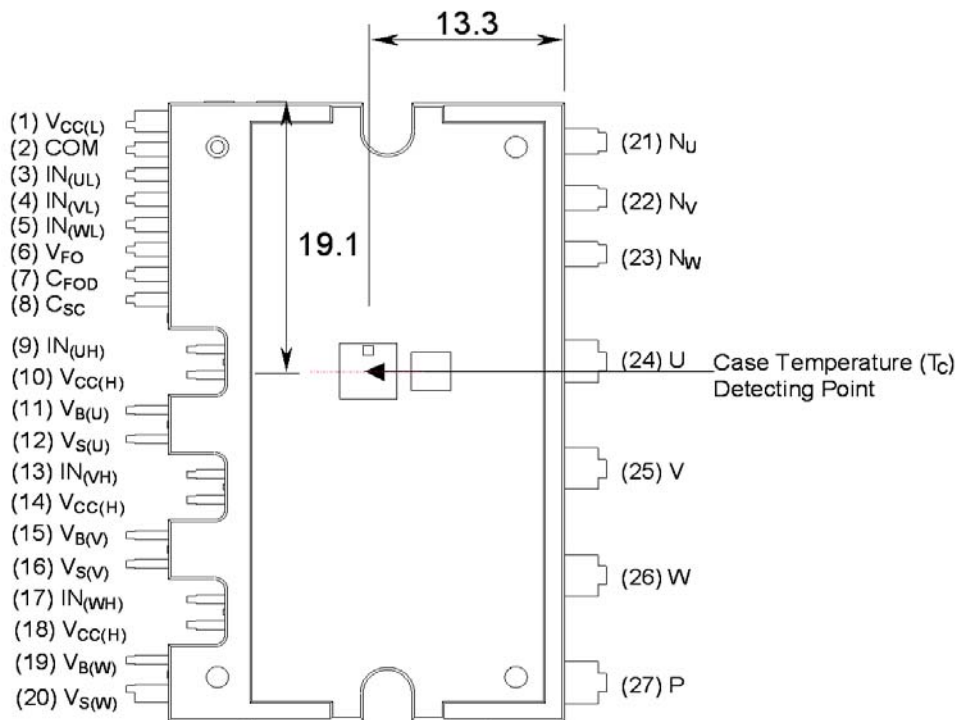


Figure 2. Top View

Pin Descriptions

| Pin Number | Pin Name | Pin Description |
|------------|-------------|---|
| 1 | $V_{CC(L)}$ | Low-Side Common Bias Voltage for IC and IGBTs Driving |
| 2 | COM | Common Supply Ground |
| 3 | $IN_{(UL)}$ | Signal Input for Low-Side U-Phase |
| 4 | $IN_{(VL)}$ | Signal Input for Low-Side V-Phase |
| 5 | $IN_{(WL)}$ | Signal Input for Low-Side W-Phase |
| 6 | V_{FO} | Fault Output |
| 7 | C_{FOD} | Capacitor for Fault Output Duration Selection |
| 8 | C_{SC} | Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input |
| 9 | $IN_{(UH)}$ | Signal Input for High-Side U-Phase |
| 10 | $V_{CC(H)}$ | High-Side Common Bias Voltage for IC and IGBTs Driving |
| 11 | $V_{B(U)}$ | High-Side Bias Voltage for U-Phase IGBT Driving |
| 12 | $V_{S(U)}$ | High-Side Bias Voltage Ground for U-Phase IGBT Driving |
| 13 | $IN_{(VH)}$ | Signal Input for High-Side V-Phase |
| 14 | $V_{CC(H)}$ | High-Side Common Bias Voltage for IC and IGBTs Driving |
| 15 | $V_{B(V)}$ | High-Side Bias Voltage for V-Phase IGBT Driving |
| 16 | $V_{S(V)}$ | High-Side Bias Voltage Ground for V Phase IGBT Driving |
| 17 | $IN_{(WH)}$ | Signal Input for High-Side W-Phase |
| 18 | $V_{CC(H)}$ | High-Side Common Bias Voltage for IC and IGBTs Driving |
| 19 | $V_{B(W)}$ | High-Side Bias Voltage for W-Phase IGBT Driving |
| 20 | $V_{S(W)}$ | High-Side Bias Voltage Ground for W-Phase IGBT Driving |
| 21 | N_U | Negative DC-Link Input for U-Phase |
| 22 | N_V | Negative DC-Link Input for V-Phase |
| 23 | N_W | Negative DC-Link Input for W-Phase |
| 24 | U | Output for U-Phase |
| 25 | V | Output for V-Phase |
| 26 | W | Output for W-Phase |
| 27 | P | Positive DC-Link Input |

Internal Equivalent Circuit and Input/Output Pins

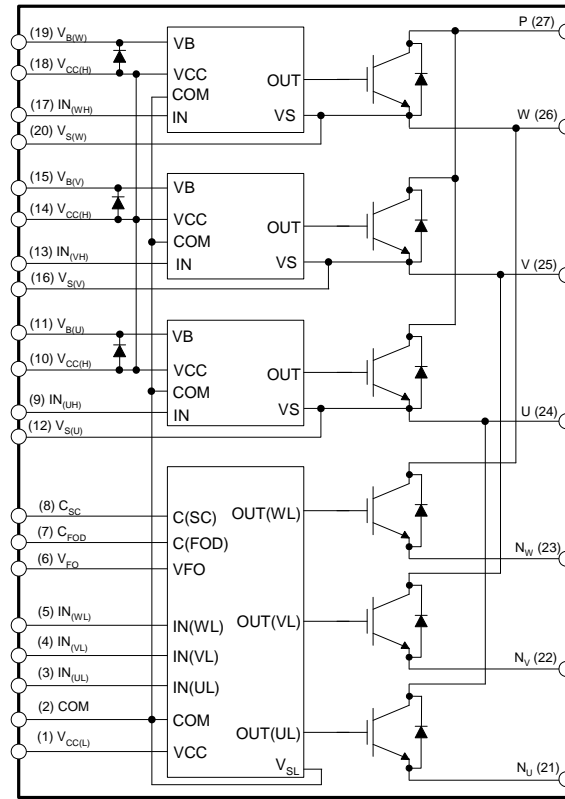


Figure 3. Internal Block Diagram

1st Notes:

1. Inverter low-side is composed of three IGBTs, freewheeling diodes for each IGBT, and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three IGBTs, freewheeling diodes, and three drive ICs for each IGBT.

Absolute Maximum Ratings ($T_J = 25^\circ\text{C}$, unless otherwise specified.)

Inverter Part

| Symbol | Parameter | Conditions | Rating | Unit |
|------------------------|------------------------------------|---|------------|------------------|
| V_{PN} | Supply Voltage | Applied between P - N_U, N_V, N_W | 450 | V |
| $V_{PN(\text{Surge})}$ | Supply Voltage (Surge) | Applied between P - N_U, N_V, N_W | 500 | V |
| V_{CES} | Collector - Emitter Voltage | | 600 | V |
| $\pm I_C$ | Each IGBT Collector Current | $T_C = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$ | 10 | A |
| $\pm I_{CP}$ | Each IGBT Collector Current (Peak) | $T_C = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$, Under 1 ms Pulse Width | 20 | A |
| P_C | Collector Dissipation | $T_C = 25^\circ\text{C}$ per Chip | 22 | W |
| T_J | Operating Junction Temperature | (2nd Note 1) | - 40 ~ 150 | $^\circ\text{C}$ |

2nd Notes:

- The maximum junction temperature rating of the power chips integrated within the Motion SPM® 3 product is 150°C (at $T_C \leq 125^\circ\text{C}$).

Control Part

| Symbol | Parameter | Conditions | Rating | Unit |
|----------|--------------------------------|--|-----------------------|------|
| V_{CC} | Control Supply Voltage | Applied between $V_{CC(H)}, V_{CC(L)}$ - COM | 20 | V |
| V_{BS} | High-Side Control Bias Voltage | Applied between $V_{B(U)} - V_{S(U)}, V_{B(V)} - V_{S(V)}, V_{B(W)} - V_{S(W)}$ | 20 | V |
| V_{IN} | Input Signal Voltage | Applied between $IN_{(UH)}, IN_{(VH)}, IN_{(WH)}, IN_{(UL)}, IN_{(VL)}, IN_{(WL)}$ - COM | -0.3 ~ $V_{CC} + 0.3$ | V |
| V_{FO} | Fault Output Supply Voltage | Applied between V_{FO} - COM | -0.3 ~ $V_{CC} + 0.3$ | V |
| I_{FO} | Fault Output Current | Sink Current at V_{FO} pin | 5 | mA |
| V_{SC} | Current-Sensing Input Voltage | Applied between C_{SC} - COM | -0.3 ~ $V_{CC} + 0.3$ | V |

Bootstrap Diode Part

| Symbol | Parameter | Conditions | Rating | Unit |
|-----------|------------------------------------|---|-----------|------------------|
| V_{RRM} | Maximum Repetitive Reverse Voltage | | 600 | V |
| I_F | Forward Current | $T_C = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$ | 0.5 | A |
| I_{FP} | Forward Current (Peak) | $T_C = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$ Under 1 ms Pulse Width | 2.0 | A |
| T_J | Operating Junction Temperature | | -40 ~ 150 | $^\circ\text{C}$ |

Total System

| Symbol | Parameter | Conditions | Rating | Unit |
|-----------------------|--|---|-----------|------------------|
| $V_{PN(\text{PROT})}$ | Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability) | $V_{CC} = V_{BS} = 13.5 \sim 16.5 \text{ V}$ $T_J = 150^\circ\text{C}$, Non-Repetitive, $< 2 \mu\text{s}$ | 400 | V |
| T_C | Module Case Operation Temperature | $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$, See Figure 2 | -40 ~ 125 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature | | -40 ~ 125 | $^\circ\text{C}$ |
| V_{ISO} | Isolation Voltage | 60 Hz, Sinusoidal, AC 1 Minute, Connect Pins to Heat Sink Plate | 2500 | V_{rms} |

Thermal Resistance

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------------|-------------------------------------|---------------------------------------|------|------|------|-----------------------------|
| $R_{th(j-c)Q}$ | Junction to Case Thermal Resistance | Inverter IGBT Part (per 1 / 6 module) | - | - | 5.5 | $^\circ\text{C} / \text{W}$ |
| $R_{th(j-c)F}$ | | Inverter FWDi Part (per 1 / 6 module) | - | - | 6.3 | $^\circ\text{C} / \text{W}$ |

2nd Notes:

- For the measurement point of case temperature (T_C), please refer to Figure 2.

Electrical Characteristics (T_J = 25°C, unless otherwise specified.)

Inverter Part

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit | |
|----------------------|---|---|---|------|------|------|----|
| V _{CE(SAT)} | Collector - Emitter Saturation Voltage | V _{CC} = V _{BS} = 15 V V _{IN} = 5 V | I _C = 10 A, T _J = 25°C | - | - | 2.0 | V |
| V _F | FWDI Forward Voltage | V _{IN} = 0 V | I _F = 10 A, T _J = 25°C | - | - | 2.1 | V |
| HS | t _{ON} t _{C(ON)} t _{OFF} t _{C(OFF)} t _{rr} | Switching Times | V _{PN} = 300 V, V _{CC} = V _{BS} = 15 V I _C = 10 A V _{IN} = 0 V ↔ 5 V, Inductive Load (2nd Note 3) | - | 0.75 | - | μs |
| | | | | - | 0.15 | - | μs |
| | | | | - | 0.60 | - | μs |
| | | | | - | 0.15 | - | μs |
| | | | | - | 0.10 | - | μs |
| LS | t _{ON} t _{C(ON)} t _{OFF} t _{C(OFF)} t _{rr} | Switching Times | V _{PN} = 300 V, V _{CC} = V _{BS} = 15 V I _C = 10 A V _{IN} = 0 V ↔ 5 V, Inductive Load (2nd Note 3) | - | 0.50 | - | μs |
| | | | | - | 0.20 | - | μs |
| | | | | - | 0.55 | - | μs |
| | | | | - | 0.15 | - | μs |
| | | | | - | 0.10 | - | μs |
| I _{CES} | Collector - Emitter Leakage Current | V _{CE} = V _{CES} | - | - | 1 | mA | |

2nd Notes:

3. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. t_{C(ON)} and t_{C(OFF)} are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

Control Part

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit | |
|----------------------|--|--|--|------|------|------|----|
| I _{QCCL} | Quiescent V _{CC} Supply Current | V _{CC} = 15 V I _{N(UL, VL, WL)} = 0 V | V _{CC(L)} - COM | - | - | 23 | mA |
| I _{QCCH} | | V _{CC} = 15 V I _{N(UH, VH, WH)} = 0 V | V _{CC(H)} - COM | - | - | 600 | μA |
| I _{QBS} | Quiescent V _{BS} Supply Current | V _{BS} = 15 V I _{N(UH, VH, WH)} = 0 V | V _{B(U)} - V _{S(U)} , V _{B(V)} - V _{S(V)} , V _{B(W)} - V _{S(W)} | - | - | 500 | μA |
| V _{FOH} | Fault Output Voltage | V _{SC} = 0 V, V _{FO} Circuit: 4.7 kΩ to 5 V Pull-up | | 4.5 | - | - | V |
| V _{FOL} | | V _{SC} = 1 V, V _{FO} Circuit: 4.7 kΩ to 5 V Pull-up | | - | - | 0.8 | V |
| V _{SC(ref)} | Short-Circuit Current Trip Level | V _{CC} = 15 V (2nd Note 4) | | 0.45 | 0.50 | 0.55 | V |
| TSD | Over-Temperature Protection | Temperature at LVIC | | - | 160 | - | °C |
| ΔTSD | Over-Temperature Protection Hysteresis | Temperature at LVIC | | - | 5 | - | °C |
| UV _{CCD} | Supply Circuit Under-Voltage Protection | Detection Level | | 10.7 | 11.9 | 13.0 | V |
| UV _{CCR} | | Reset Level | | 11.2 | 12.4 | 13.4 | V |
| UV _{BSD} | | Detection Level | | 10 | 11 | 12 | V |
| UV _{BSR} | | Reset Level | | 10.5 | 11.5 | 12.5 | V |
| t _{FOD} | Fault-Out Pulse Width | C _{FOD} = 33 nF (2nd Note 5) | | 1.0 | 1.8 | - | ms |
| V _{IN(ON)} | ON Threshold Voltage | Applied between I _{N(UH)} , I _{N(VH)} , I _{N(WH)} , I _{N(UL)} , I _{N(VL)} , I _{N(WL)} - COM | | 2.8 | - | - | V |
| V _{IN(OFF)} | OFF Threshold Voltage | | | - | - | 0.8 | V |

2nd Notes:

4. Short-circuit protection is functioning only at the low-sides.

5. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation: C_{FOD} = 18.3 x 10⁻⁶ x t_{FOD} [F]

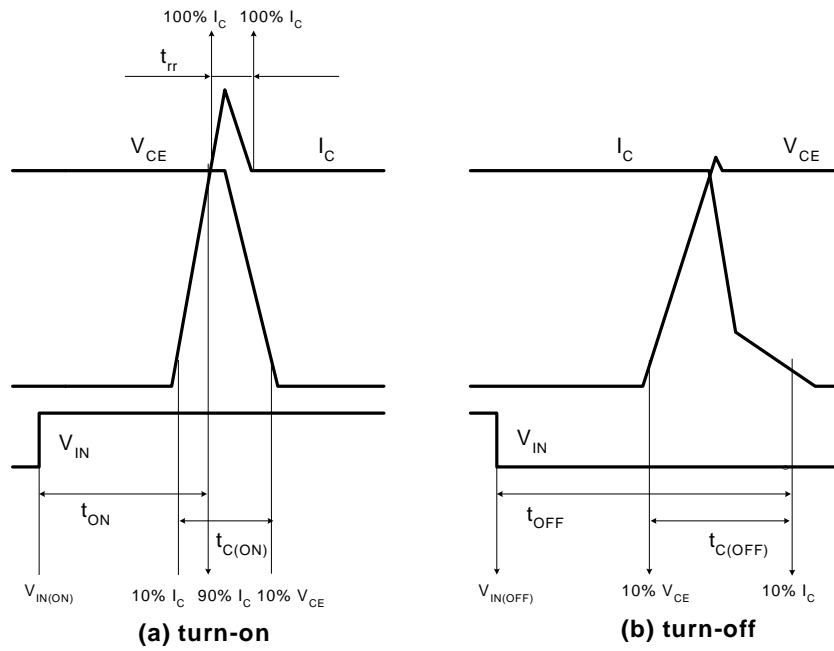


Figure 4. Switching Time Definition

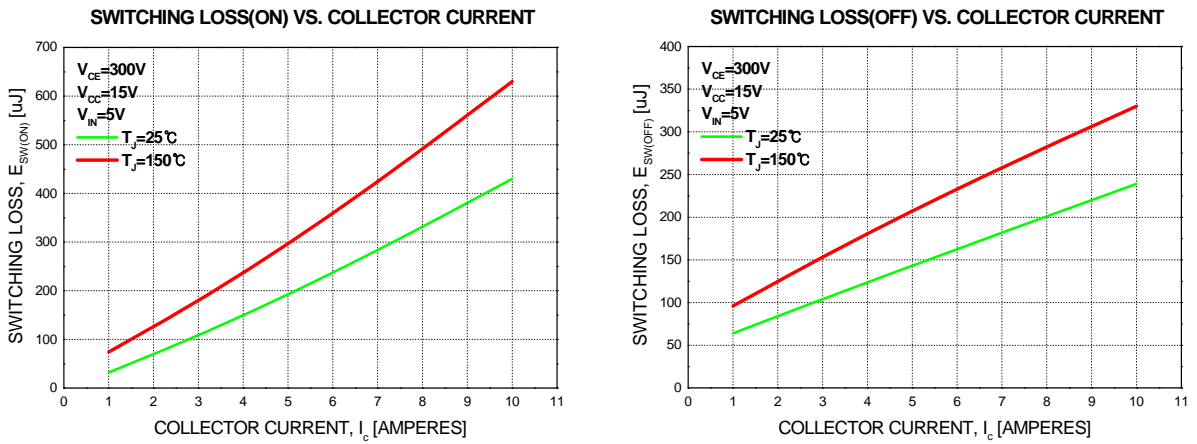


Figure 5. Switching Loss Characteristics (Typical)

Bootstrap Diode Part

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------|-----------------------|---|------|------|------|------|
| V_F | Forward Voltage | $I_F = 0.1 \text{ A}, T_C = 25^\circ\text{C}$ | - | 2.5 | - | V |
| t_{rr} | Reverse-Recovery Time | $I_F = 0.1 \text{ A}, T_C = 25^\circ\text{C}$ | - | 80 | - | ns |

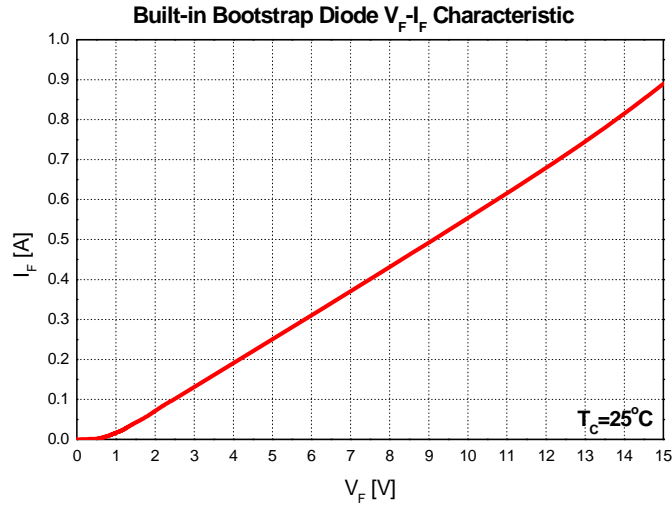


Figure 6. Built-in Bootstrap Diode Characteristics

2nd Notes:

6. Built-in bootstrap diode includes around 15 Ω resistance characteristic.

Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------------------------|--|--|------|------|------|-------------------|
| V_{PN} | Supply Voltage | Applied between P - N_U, N_V, N_W | - | 300 | 400 | V |
| V_{CC} | Control Supply Voltage | Applied between $V_{CC(H)}, V_{CC(L)}$ - COM | 13.5 | 15.0 | 16.5 | V |
| V_{BS} | High-Side Bias Voltage | Applied between $V_{B(U)} - V_{S(U)}, V_{B(V)} - V_{S(V)}, V_{B(W)} - V_{S(W)}$ | 13.0 | 15.0 | 18.5 | V |
| $dV_{CC} / dt, dV_{BS} / dt$ | Control Supply Variation | | -1 | - | 1 | V / μs |
| t_{dead} | Blanking Time for Preventing Arm-Short | Each Input Signal | 2 | - | - | μs |
| f_{PWM} | PWM Input Signal | $-40^\circ\text{C} \leq T_C \leq 125^\circ\text{C}, -40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ | - | - | 20 | kHz |
| V_{SEN} | Voltage for Current Sensing | Applied between N_U, N_V, N_W - COM (Including Surge Voltage) | -4 | | 4 | V |

Mechanical Characteristics and Ratings

| Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|----------------------|------|-------|------|------|
| Mounting Torque | Mounting Screw: M3 | Recommended 0.62 N•m | 0.51 | 0.62 | 1.00 | N•m |
| Device Flatness | | See Figure 7 | 0 | - | +120 | μm |
| Weight | | | - | 15.40 | - | g |

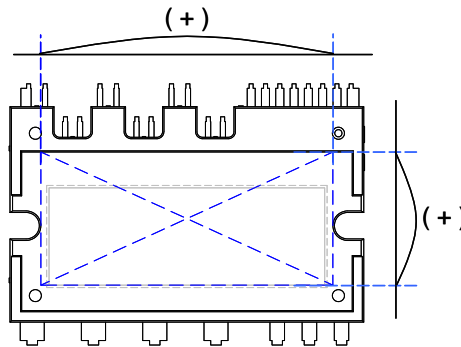
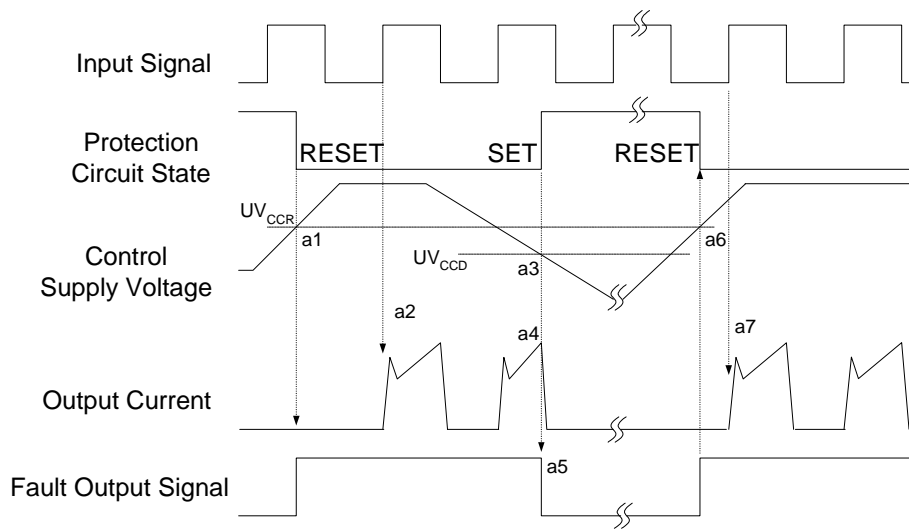


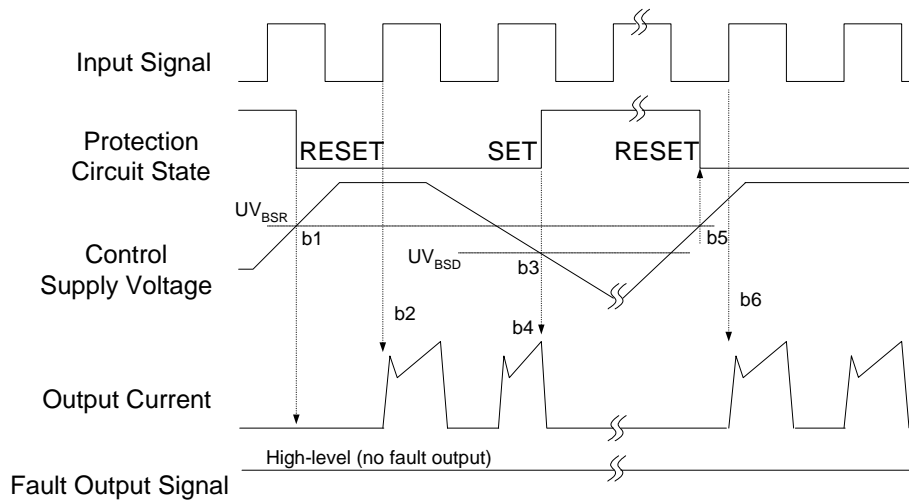
Figure 7. Flatness Measurement Position

Time Charts of Protective Function



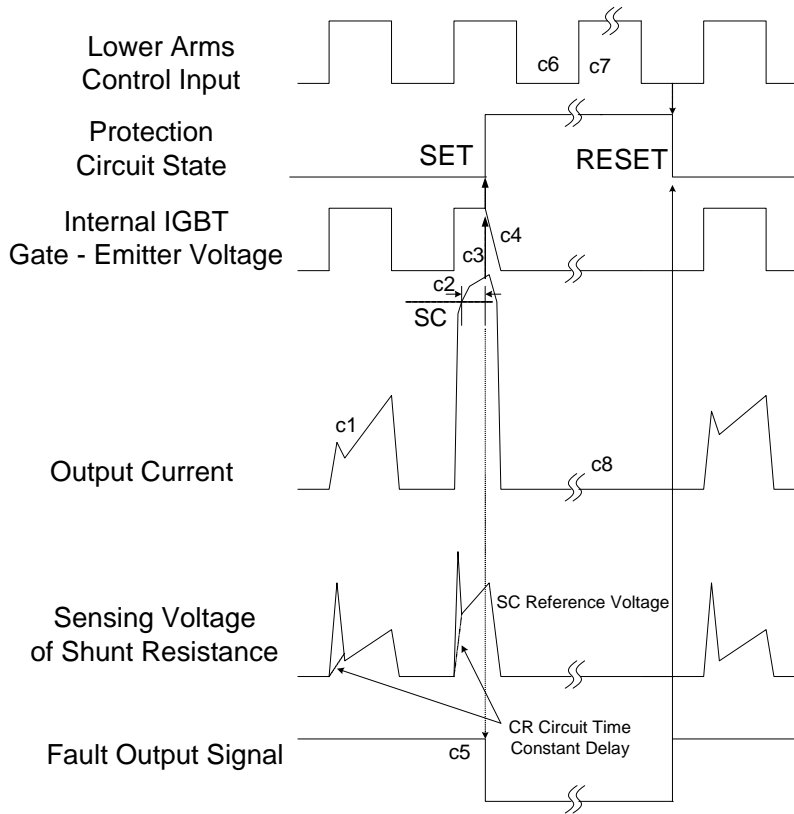
- a1 : Control supply voltage rises: after the voltage rises UV_{CCR} , the circuits start to operate when next input is applied.
- a2 : Normal operation: IGBT ON and carrying current.
- a3 : Under-voltage detection (UV_{CCD}).
- a4 : IGBT OFF in spite of control input condition.
- a5 : Fault output operation starts.
- a6 : Under-voltage reset (UV_{CCR}).
- a7 : Normal operation: IGBT ON and carrying current.

Figure 8. Under-Voltage Protection (Low-Side)



- b1 : Control supply voltage rises: after the voltage reaches UV_{BSR} , the circuits start to operate when next input is applied.
- b2 : Normal operation: IGBT ON and carrying current.
- b3 : Under-voltage detection (UV_{BSD}).
- b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5 : Under-voltage reset (UV_{BSR}).
- b6 : Normal operation: IGBT ON and carrying current.

Figure 9. Under-Voltage Protection (High-Side)



(with the external shunt resistance and CR connection)

- c1 : Normal operation: IGBT ON and carrying current.
- c2 : Short-circuit current detection (SC trigger).
- c3 : Hard IGBT gate interrupt.
- c4 : IGBT turns OFF.
- c5 : Fault output timer operation starts: the pulse width of the fault output signal is set by the external capacitor C_{FO} .
- c6 : Input "LOW": IGBT OFF state.
- c7 : Input "HIGH": IGBT ON state, but during the active period of fault output, the IGBT doesn't turn ON.
- c8 : IGBT OFF state.

Figure 10. Short-Circuit Protection (Low-Side Operation Only)

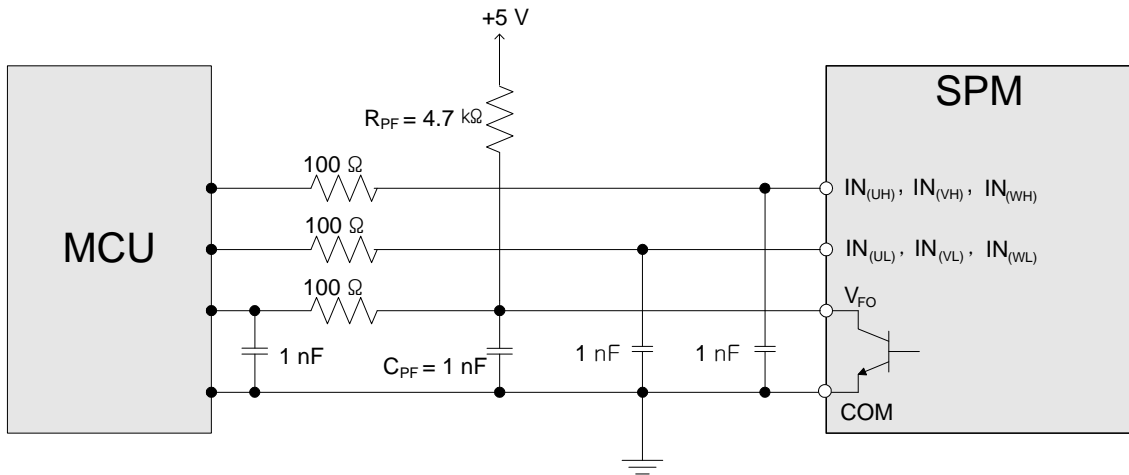


Figure 11. Recommended MCU I/O Interface Circuit

3rd Notes:

1. RC coupling at each input might change depending on the PWM control scheme in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM® 3 product integrates a 5 kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.
2. The logic input works with standard CMOS or LSTTL outputs.

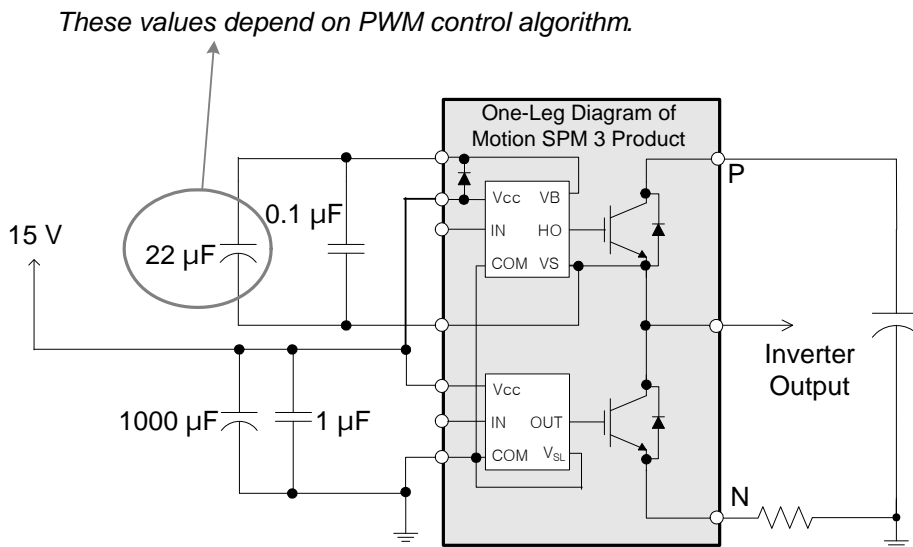


Figure 12. Recommended Bootstrap Operation Circuit and Parameters

3rd Notes:

3. The ceramic capacitor placed between V_{CC} - COM should be over 1 μF and mounted as close to the pins of the Motion SPM 3 product as possible.

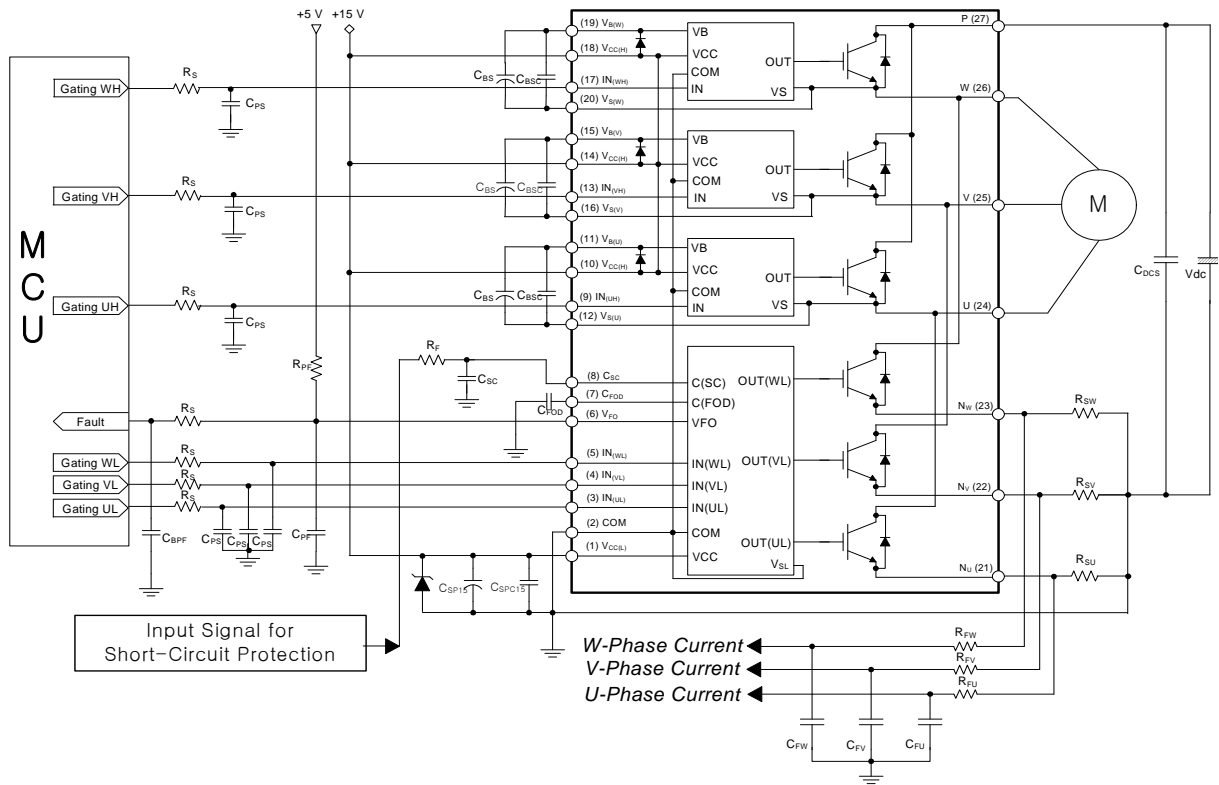
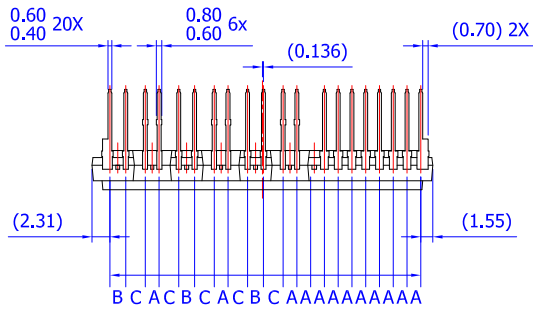


Figure 13. Typical Application Circuit

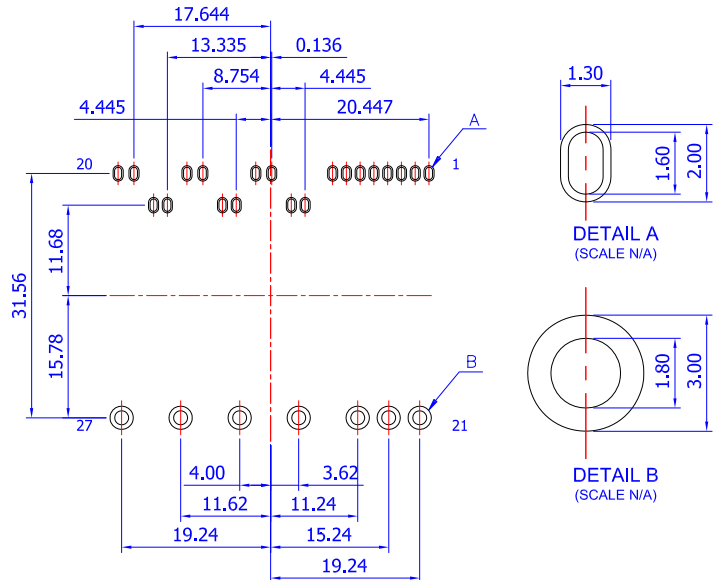
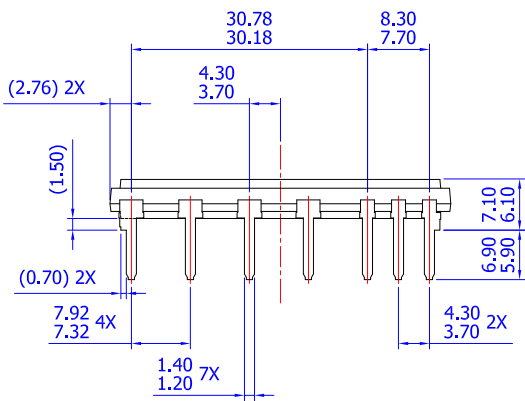
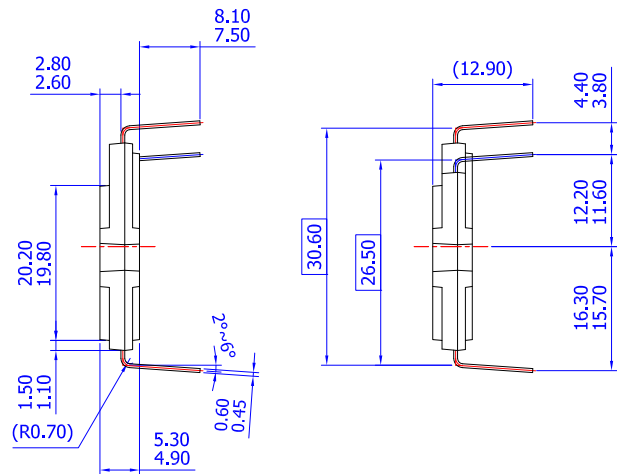
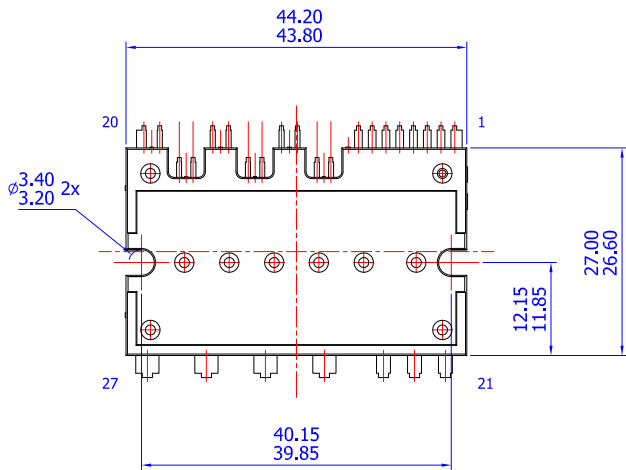
4th Notes:

1. To avoid malfunction, the wiring of each input should be as short as possible (less than 2 - 3cm).
2. By virtue of integrating an application-specific type of HVIC inside the Motion SPM® 3 product, direct coupling to MCU terminals without any optocoupler or transformer isolation is possible.
3. V_{FOD} output is open-collector type. This signal line should be pulled up to the positive side of the 5 V power supply with approximately 4.7 kΩ resistance (please refer to Figure11).
4. C_{SP15} of around seven times larger than bootstrap capacitor C_{BS} is recommended.
5. V_{FOD} output pulse width should be determined by connecting an external capacitor (C_{FOD}) between C_{FOD} (pin 7) and COM (pin 2). (Example: if C_{FOD} = 33 nF, then t_{FOD} = 1.8 ms (typ.)) Please refer to the 2nd note 5 for calculation method.
6. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull down each input signal line to GND. RC coupling circuits should be used to prevent input signal oscillation. R_SC_{PS} time constant should be selected in the range 50 ~ 150 ns. C_{PS} should not be less than 1 nF (recommended R_S = 100 Ω, C_{PS} = 1 nF).
7. To prevent errors of the protection function, the wiring around R_F and C_{SC} should be as short as possible.
8. In the short-circuit protection circuit, please select the R_FC_{SC} time constant in the range 1.5 ~ 2.0 μs.
9. Each capacitor should be mounted as close to the pins of the Motion SPM 3 product as possible.
10. To prevent surge destruction, the wiring between the smoothing capacitor and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 μF between the P & GND pins is recommended.
11. Relays are used in almost every systems of electrical equipment in home appliances. In these cases, there should be sufficient distance between the MCU and the relays.
12. C_{SP15} should be over 1 μF and mounted as close to the pins of the Motion SPM 3 product as possible.



LEAD PITCH (TOLERANCE : ±0.30)

- A : 1.778
- B : 2.050
- C : 2.531



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
 - B) ALL DIMENSIONS ARE IN MILLIMETERS
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D) () IS REFERENCE
 - E) [] IS ASS'Y QUALITY
 - F) DRAWING FILENAME: MOD27DAREV3.0
 - G) FAIRCHILD SEMICONDUCTOR

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