
**Is Now Part of**


**ON Semiconductor®**

**To learn more about ON Semiconductor, please visit our website at**
**www.onsemi.com**

February 2016

# HCPL3700M
# AC/DC to Logic Interface Optocoupler

## Features

- AC or DC Input
- Programmable Sense Voltage
- Logic Level Compatibility
- Threshold Guaranteed Over Temperature (0°C to 70°C)
- Safety and Regulatory Approvals
  - UL1577, 5,000 $VAC_{RMS}$ for 1 Minute
  - DIN EN/IEC60747-5-5

## Applications

- Low Voltage Detection
- 5 V to 240 V AC/DC Voltage Sensing
- Relay Contact Monitor
- Current Sensing
- Microprocessor Interface
- Industrial Controls

## Description

The HCPL3700M voltage/current threshold detection optocoupler consists of an AlGaAs LED connected to a threshold sensing input buffer IC which are optically coupled to a high gain darlington output. The input buffer chip is capable of controlling threshold levels over a wide range of input voltages with a single resistor. The output is TTL and CMOS compatible.

## Schematics

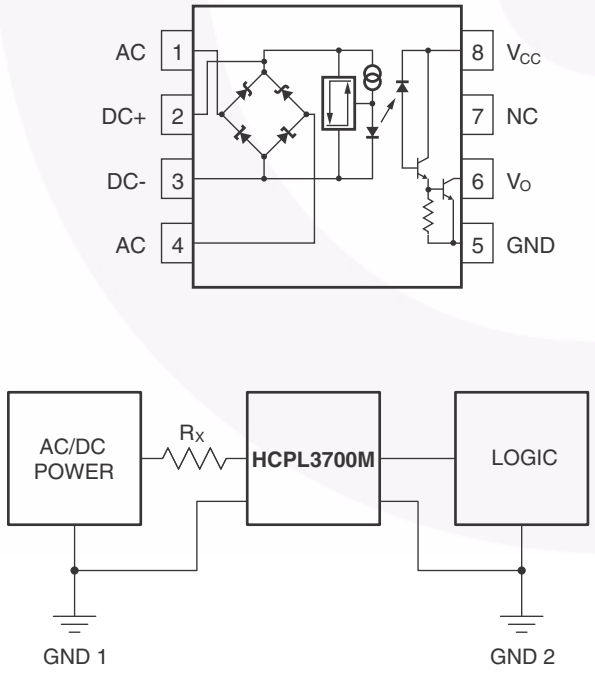



**Figure 1. Schematic**

## Package Outlines

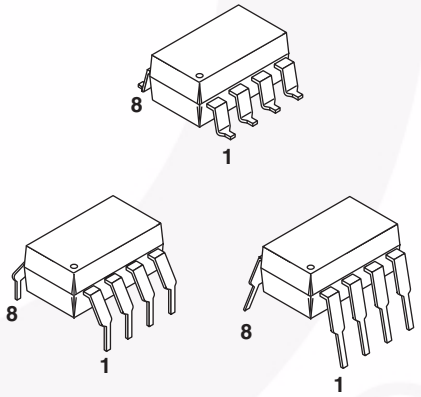



**Figure 2. Package Outlines**

**TRUTH TABLE**
(Positive Logic)

| Input | Output |
|---|---|
| H | L |
| L | H |

A 0.1µF bypass capacitor must be connected between pins 8 and 5.

## Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

| Parameter | | Characteristics |
|---|---|---|
| Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage | < 150 $V_{RMS}$ | I–IV |
| | < 300 $V_{RMS}$ | I–IV |
| | < 450 $V_{RMS}$ | I–III |
| | < 600 $V_{RMS}$ | I–III |
| | < 1000 $V_{RMS}$ (Option TV) | I–III |
| Climatic Classification | | 40/85/21 |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 |
| Comparative Tracking Index | | 175 |

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{PR}$ | Input-to-Output Test Voltage, Method A, $V_{IORM}$ x 1.6 = $V_{PR}$, Type and Sample Test with $t_m$ = 10 s, Partial Discharge < 5 pC | 2,262 | $V_{peak}$ |
| | Input-to-Output Test Voltage, Method B, $V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test with $t_m$ = 1 s, Partial Discharge < 5 pC | 2,651 | $V_{peak}$ |
| $V_{IORM}$ | Maximum Working Insulation Voltage | 1,414 | $V_{peak}$ |
| $V_{IOTM}$ | Highest Allowable Over-Voltage | 6,000 | $V_{peak}$ |
| | External Creepage | ≥ 8 | mm |
| | External Clearance | ≥ 7.4 | mm |
| | External Clearance (for Option TV, 0.4" Lead Spacing) | ≥ 10.16 | mm |
| DTI | Distance Through Insulation (Insulation Thickness) | ≥ 0.5 | mm |
| $T_S$ | Case Temperature(1) | 150 | °C |
| $I_{S,INPUT}$ | Input Current(1) | 25 | mA |
| $P_{S,OUTPUT}$ | Output Power (Duty Factor ≤ 2.7%)(1) | 250 | mW |
| $R_{IO}$ | Insulation Resistance at $T_S$, $V_{IO}$ = 500 V(1) | > $10^9$ | Ω |

**Note:**

1. Safety limit value - maximum values allowed in the event of a failure.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A$ = 25°C unless otherwise specified.

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | | -40 to +125 | °C |
| $T_{OPR}$ | Operating Temperature | | -40 to +85 | °C |
| $T_J$ | Junction Temperature | | -40 to +125 | °C |
| $T_{SOL}$ | Lead Solder Temperature | | 260 for 10 sec | °C |
| $P_T$ | Total Package Power Dissipation(2) | | 305 | mW |
| **EMITTER** | | | | |
| $I_{IN}$ | Input Current | Average | 50 | mA |
| | | Surge, 3 ms, 120 Hz Pulse Rate | 140 | |
| | | Transient, 10 µs, 120 Hz Pulse Rate | 500 | |
| $V_{IN}$ | Input Voltage (Pins 2-3) | | -0.5 | V |
| $P_{IN}$ | Input Power Dissipation(3) | | 230 | mW |
| **DETECTOR** | | | | |
| $I_O$ | Output Current (Average)(4) | | 30 | mA |
| $V_{CC}$ | Supply Voltage (Pins 8-5) | | -0.5 to 20 | V |
| $V_O$ | Output Voltage (Pins 6-5) | | -0.5 to 20 | V |
| $P_O$ | Output Power Dissipation(5) | | 210 | mW |

**Notes:**

2. Derate linearly above 70°C free-air temperature at a rate of 2.5 mW/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 1.8 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
5. Derate linearly above 70°C free-air temperature at a rate of 1.9 mW/°C.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 | 18 | V |
| $T_A$ | Ambient Operating Temperature | 0 | 70 | °C |
| f | Operating Frequency | 0 | 4 | kHz |

## Electrical Characteristics ($T_A$ = 0°C to 70°C Unless otherwise specified)

| Symbol | Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{TH+}$ | Input Threshold Current | | $V_{IN} = V_{TH+}$, $V_{CC}$ = 4.5 V | 1.96 | 2.40 | 3.11 | mA |
| $I_{TH-}$ | | | $V_O$ = 0.4 V, $I_O \geq$ 4.2 mA(6) | 1.00 | 1.20 | 1.62 | |
| $V_{TH+}$ | Input Threshold Voltage | DC (Pins 2, 3) | $V_{IN} = V_2 - V_3$ (Pins 1 & 4 Open) $V_{CC}$ = 4.5 V, $V_O$ = 0.4 V(6) $I_O \geq$ 4.2 mA | 3.35 | 3.80 | 4.05 | V |
| $V_{TH-}$ | | | $V_{IN} = V_2 - V_3$ (Pins 1 & 4 Open) $V_{CC}$ = 4.5 V, $V_O$ = 2.4 V(6) $I_O \geq$ 100 µA | 2.01 | 2.50 | 2.86 | V |
| $V_{TH+}$ | | AC (Pins 1, 4) | $\lvert V_{IN} \rvert = \lvert V_1 - V_4 \rvert$ (Pins 2 & 3 Open) $V_{CC}$ = 4.5 V, $V_O$ = 0.4 V(6) $I_O \geq$ 4.2 mA | 4.23 | 5.00 | 5.50 | V |
| $V_{TH-}$ | | | $\lvert V_{IN} \rvert = \lvert V_1 - V_4 \rvert$ (Pins 2 & 3 Open) $V_{CC}$ = 4.5 V, $V_O$ = 2.4 V(6) $I_O \leq$ 100 µA | 2.87 | 3.70 | 4.20 | V |
| $I_{HYS}$ | Hysteresis | | $I_{HYS} = I_{TH+} - I_{TH-}$ | | 1.2 | | mA |
| $V_{HYS}$ | | | $V_{HYS} = V_{TH+} - V_{TH-}$ | | 1.3 | | V |
| $V_{IHC1}$ | Input Clamp Voltage | | $V_{IHC1} = V_2 - V_3$, $V_3$ = GND, $I_{IN}$ = 10 mA, Pins 1 & 4 connected to Pin 3 | 5.4 | 6.3 | 6.6 | V |
| $V_{IHC2}$ | | | $V_{IHC2} = \lvert V_1 - V_4 \rvert$, $\lvert I_{IN} \rvert$ = 10 mA (Pins 2 & 3 Open) | 6.1 | 7.0 | 7.3 | V |
| $V_{IHC3}$ | | | $V_{IHC3} = V_2 - V_3$, $V_3$ = GND, $I_{IN}$ = 15 mA (Pins 1 & 4 Open) | | 12.5 | 13.4 | V |
| $V_{ILC}$ | | | $V_{ILC} = V_2 - V_3$, $V_3$ = GND, $I_{IN}$ = -10 mA | | -0.75 | | V |
| $I_{IN}$ | Input Current | | $V_{IN} = V_2 - V_3$ = 5.0 V (Pins 1 & 4 Open) | 3.0 | 3.7 | 4.4 | mA |
| $V_{D1,2}$ | Bridge Diode Forward Voltage | | $I_{IN}$ = 3 mA | | 0.65 | | V |
| $V_{D3,4}$ | | | $I_{IN}$ = 3 mA | | 0.65 | | V |
| $V_{OL}$ | Logic LOW Output Voltage | | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.2 mA(6) | | 0.04 | 0.40 | V |
| $I_{OH}$ | Logic HIGH Output Current | | $V_{OH} = V_{CC}$ = 18 V(6) | | | 100 | µA |
| $I_{CCL}$ | Logic LOW Supply Current | | $V_2 - V_3$ = 5.0 V, $V_O$ = Open, $V_{CC}$ = 5 V | | 1.0 | 4 | mA |
| $I_{CCH}$ | Logic HIGH Supply Current | | $V_{CC}$ = 18 V, $V_O$ = Open | | 0.01 | 4 | µA |
| $C_{IN}$ | Input Capacitance | | f = 1 MHz, $V_{IN}$ = 0 V (Pins 2 & 3, Pins 1 & 4 Open) | | 50 | | pF |

**Note:**

6. Logic LOW output level at pin 6 occurs when $V_{IN} \geq V_{TH+}$ and when $V_{IN} > V_{TH-}$ once $V_{IN}$ exceeds $V_{TH+}$. Logic HIGH output level at pin 6 occurs when $V_{IN} \leq V_{TH-}$ and when $V_{IN} < V_{TH+}$ once decreases below $V_{TH-}$.

## Switching Characteristics ($T_A$ = 25°C, $V_{CC}$ = 5 V unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time (to Output Low Level) | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF(7) | | 6.0 | 15 | µs |
| $t_{PLH}$ | Propagation Delay Time (to Output High Level) | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF(7) | | 25.0 | 40 | µs |
| $t_R$ | Output Rise Time (10–90%) | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF | | 45 | | µs |
| $t_F$ | Output Fall Time (90–10%) | $R_L$ = 4.7 kΩ, $C_L$ = 30 pF | | 0.5 | | µs |
| $\|CM_H\|$ | Common Mode Transient Immunity (at Output High Level) | $I_{IN}$ = 0 mA, $R_L$ = 4.7 kΩ, $V_{O\ min}$ = 2.0 V, $V_{CM}$ = 1400 V(8)(9) | | 4000 | | V/µs |
| $\|CM_L\|$ | Common Mode Transient Immunity (at Output Low Level) | $I_{IN}$ = 3.11 mA, $R_L$ = 4.7 kΩ, $V_{O\ max}$ = 0.8 V, $V_{CM}$ = 1400 V(8)(9) | | 600 | | V/µs |

## Isolation Characteristics ($T_A$ = 25°C unless otherwise specified.)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{ISO}$ | Withstand Isolation Voltage | RH ≤ 50%, $I_{I-O}$ ≤ 10 µA, t = 1 minute, f = 50 Hz(10)(11) | 5000 | | | $VAC_{RMS}$ |
| $R_{I-O}$ | Resistance (Input to Output) | $V_{IO}$ = 500 $V_{DC}$(10) | | $10^{12}$ | | Ω |
| $C_{I-O}$ | Capacitance (Input to Output) | f = 1 MHz, $V_{IO}$ = 0 $V_{DC}$ | | 0.6 | | pF |

**Notes:**

7. $T_{PHL}$ propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 µs rise time) to the 1.5 V level on the leading edge of the output pulse. $T_{PLH}$ propagation delay is measured on the trailing edges of the input and output pulse. (Refer to Fig. 11)
8. Common mode transient immunity in logic high level is the maximum tolerable (positive) $dV_{cm}/dt$ on the leading edge of the common mode pulse signal $V_{CM}$, to assure that the output will remain in a logic high state (i.e., $V_O$ > 2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) $dV_{cm}/dt$ on the trailing edge of the common mode pulse signal, $V_{CM}$, to assure that the output will remain in a logic low state (i.e., $V_O$ < 0.8 V). Refer to Fig. 12.
9. In applications where $dV_{cm}/dt$ may exceed 50,000 V/µs (Such as static discharge), a series resistor, $R_{CC}$, should be included to protect the detector chip from destructive surge currents. The recommended value for $R_{CC}$ is 240 V per volt of allowable drop in $V_{CC}$ (between pin 8 and $V_{CC}$) with a minimum value of 240 Ω.
10. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
11. The 5000 $VAC_{RMS}$/1 min. capability is validated by a 6000 $VAC_{RMS}$/1 sec. dielectric voltage withstand test.

## Typical Performance Curves

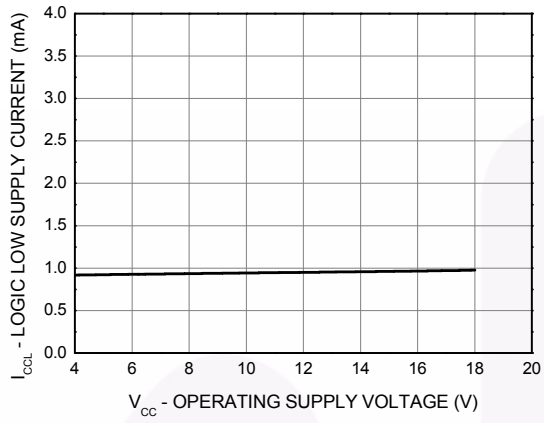



**Figure 3. Logic Low Supply Current vs. Operating Supply Voltage**

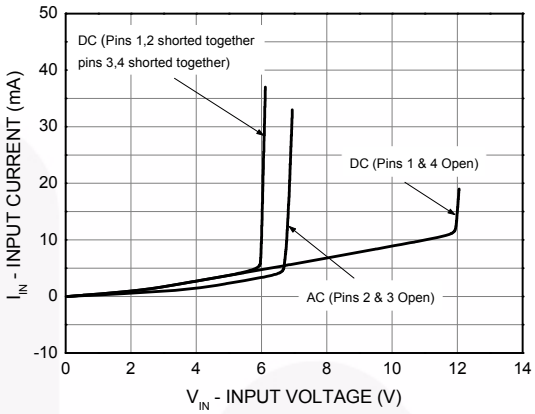



**Figure 4. Input Current vs. Input Voltage**

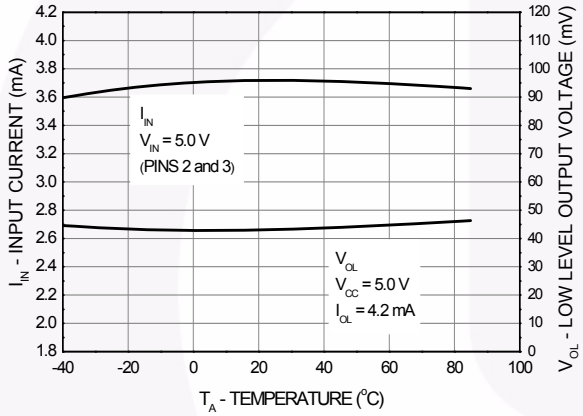



**Figure 5. Input Current/Low Level Output Voltage vs. Temperature**

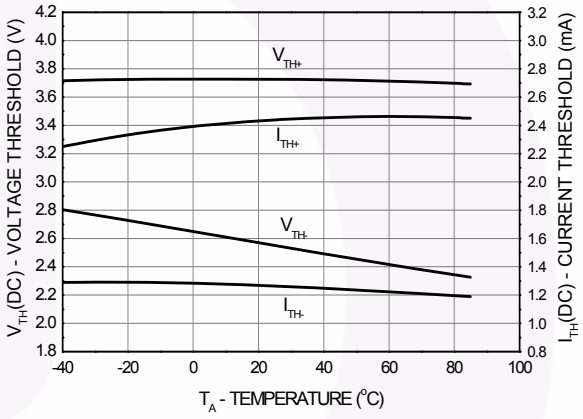



**Figure 6. Current Threshold/Voltage Threshold vs. Temperature**

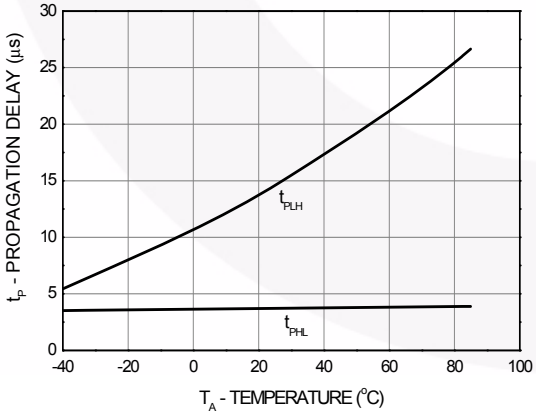



**Figure 7. Propagation Delay vs. Temperature**

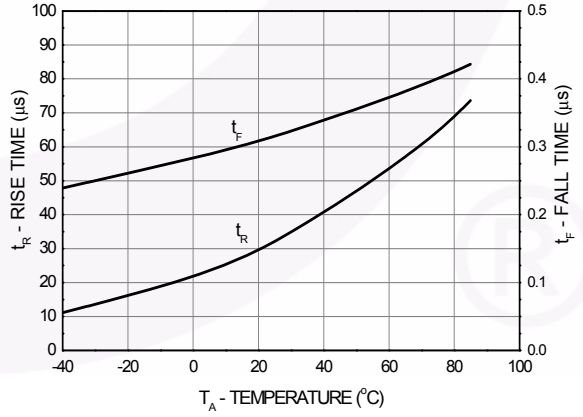



**Figure 8. Rise and Fall Time vs. Temperature**

## Typical Performance Curves (Continued)

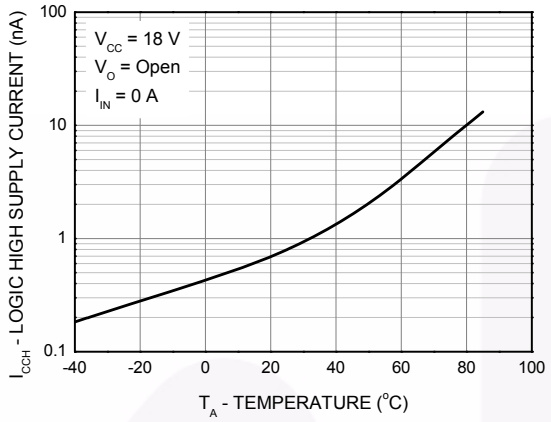



**Figure 9. Logic High Supply Current vs. Temperature**

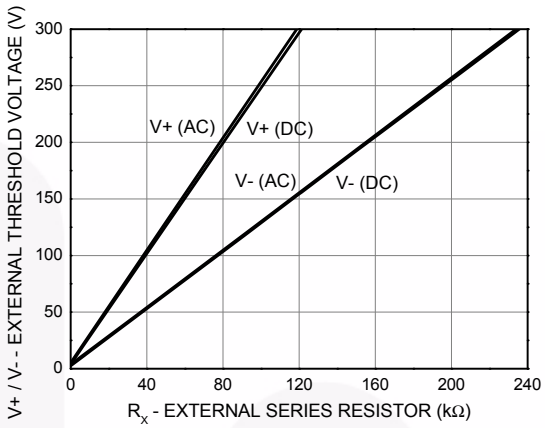
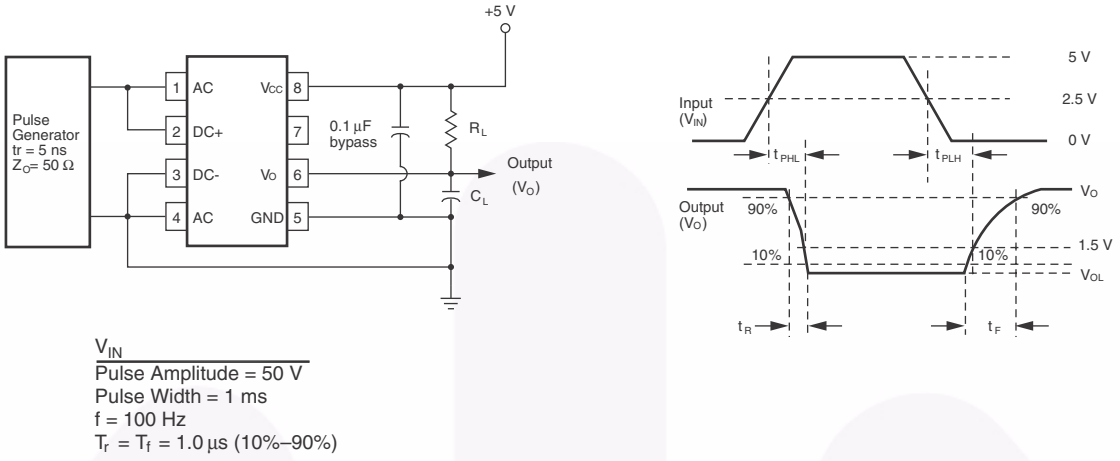



**Figure 10. External Threshold Characteristics V+/V- vs. Rx**

## Test Circuits




$V_{IN}$
Pulse Amplitude = 50 V
Pulse Width = 1 ms
f = 100 Hz
$T_r = T_f = 1.0\ \mu s$ (10%–90%)

**Fig. 11. Switching Test Circuit**

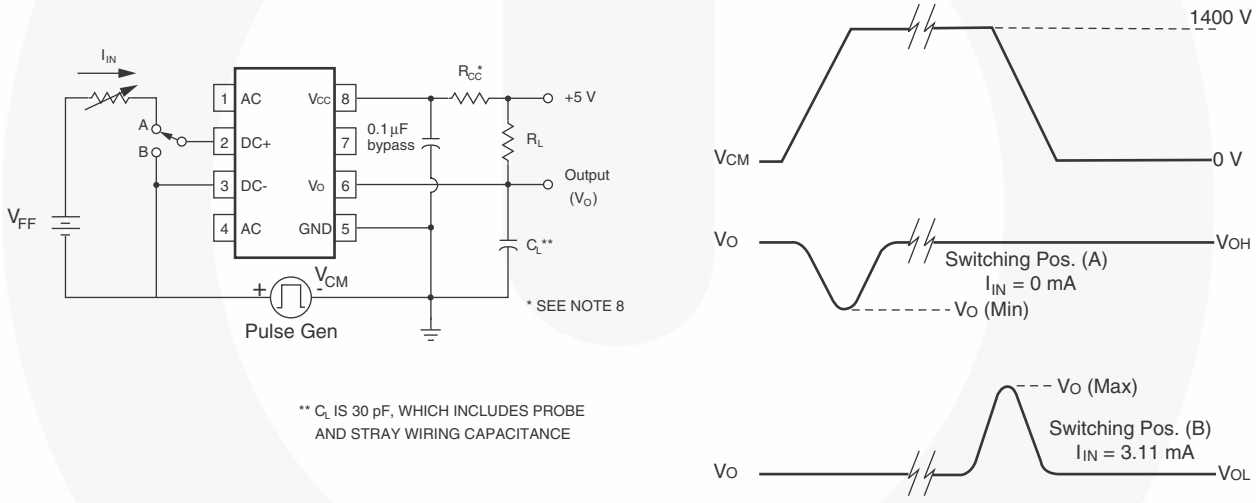
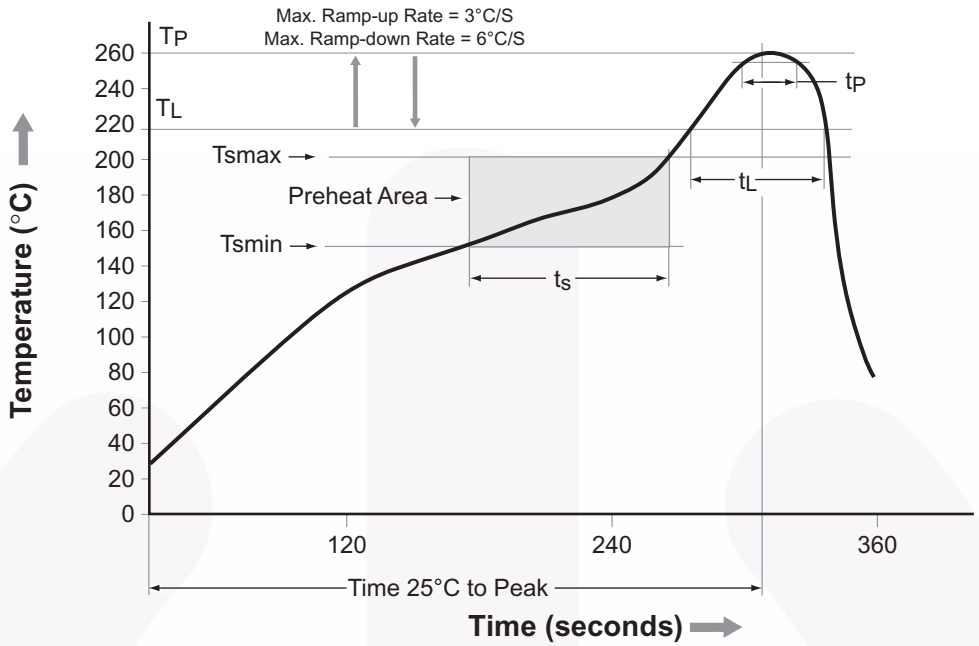



**Fig. 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms**

## Reflow Profile




| Profile Freature | Pb-Free Assembly Profile |
|---|---|
| Temperature Min. (Tsmin) | 150°C |
| Temperature Max. (Tsmax) | 200°C |
| Time ($t_S$) from (Tsmin to Tsmax) | 60–120 seconds |
| Ramp-up Rate ($t_L$ to $t_P$) | 3°C/second max. |
| Liquidous Temperature ($T_L$) | 217°C |
| Time ($t_L$) Maintained Above ($T_L$) | 60–150 seconds |
| Peak Body Package Temperature | 260°C +0°C / –5°C |
| Time ($t_P$) within 5°C of 260°C | 30 seconds |
| Ramp-down Rate ($T_P$ to $T_L$) | 6°C/second max. |
| Time 25°C to Peak Temperature | 8 minutes max. |

**Figure 13. Reflow Profile**

## Ordering Information

| Part Number | Package | Packing Method |
|---|---|---|
| HCPL3700M | DIP 8-Pin | Tube (50 units) |
| HCPL3700SM | SMT 8-Pin (Lead Bend) | Tube (50 units) |
| HCPL3700SDM | SMT 8-Pin (Lead Bend) | Tape and Reel (1,000 units) |
| HCPL3700VM | DIP 8-Pin, DIN EN/IEC60747-5-5 option | Tube (50 units) |
| HCPL3700SVM | SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option | Tube (50 units) |
| HCPL3700SDVM | SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option | Tape and Reel (1,000 units) |
| HCPL3700TVM | DIP 8-Pin, 0.4” Lead Spacing, DIN EN/IEC 60747-5-5 option | Tube (50 units) |

## Marking Information

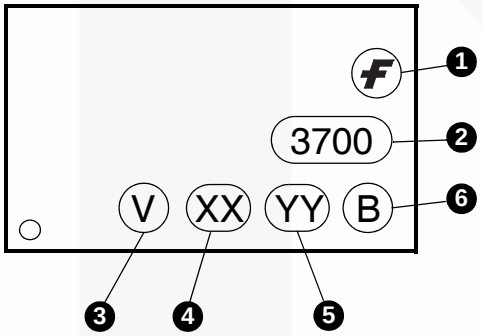
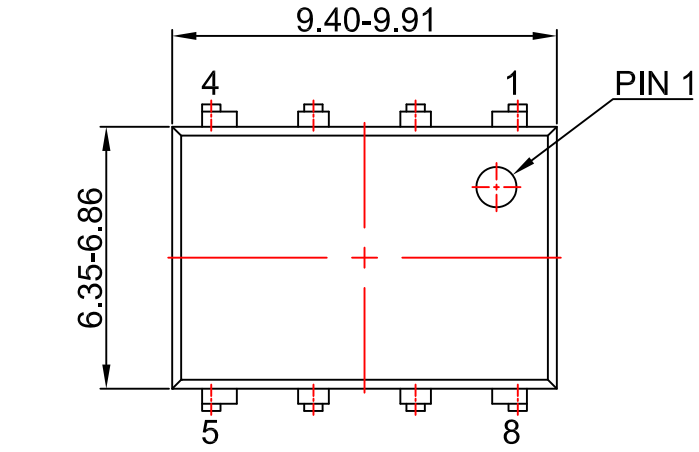
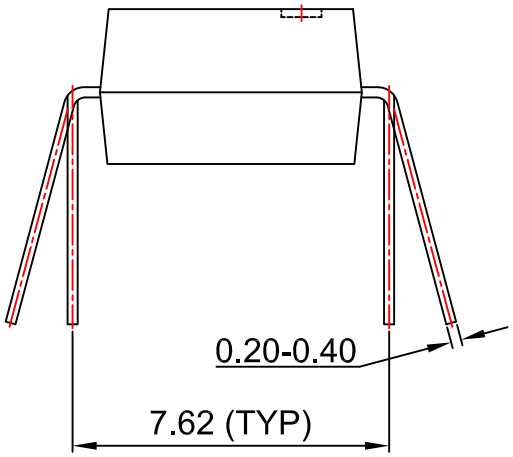
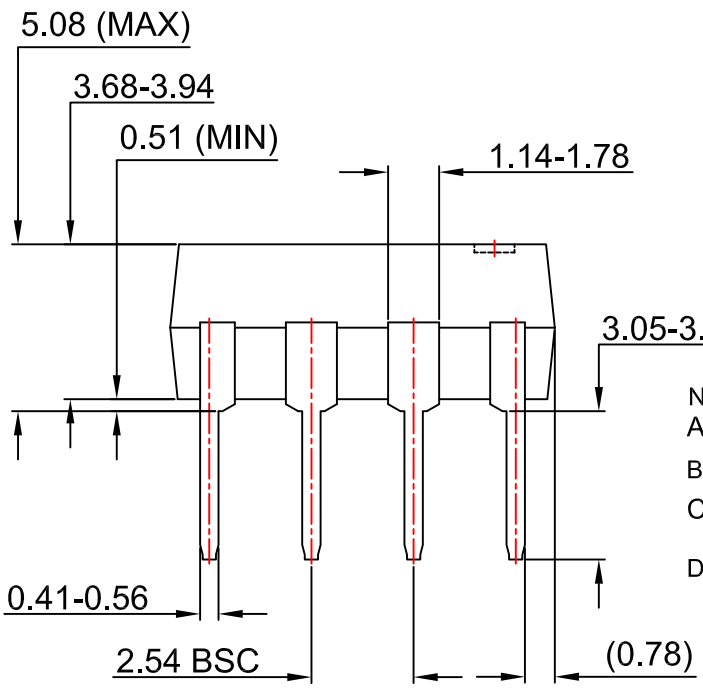



**Figure 14. Top Mark**

| Definitions | |
|---|---|
| 1 | Fairchild Logo |
| 2 | Device Number |
| 3 | DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option) |
| 4 | Two Digit Year Code, e.g., ‘15’ |
| 5 | Two Digit Work Week Ranging from ‘01’ to ‘53’ |
| 6 | Assembly Package Code |




NOTES:

A) NO STANDARD APPLIES TO THIS PACKAGE

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

D) DRAWING FILENAME AND REVSION: MKT-N08GREV7

FAIRCHILD

## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AttitudeEngine™
Awinda®
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
*CROSSVOLT*™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource SM
GreenBridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
MotionGrid®
MTi®
MTx®
MVN®
mWSaver®
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
®
Power Supply WebDesigner™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™
SerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™
Xsens™
仙童®

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT HTTP://WWW.FAIRCHILDSEMI.COM. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## AUTHORIZED USE

Unless otherwise specified in this data sheet, this product is a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability. This product may not be used in the following applications, unless specifically approved in writing by a Fairchild officer: (1) automotive or other transportation, (2) military/aerospace, (3) any safety critical application – including life critical medical equipment – where the failure of the Fairchild product reasonably would be expected to result in personal injury, death or property damage. Customer's use of this product is subject to agreement of this Authorized Use policy. In the event of an unauthorized use of Fairchild's product, Fairchild accepts no liability in the event of product failure. In other respects, this product shall be subject to Fairchild's Worldwide Terms and Conditions of Sale, unless a separate agreement has been signed by both Parties.

## ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Terms of Use

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only. |

Rev. I77

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Fairchild Semiconductor:

HCPL3700M