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1200 V NPT IGBT

HGTG18N120BND is based on Non- Punch Through (NPT) IGBT designs. The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: UPS, solar inverter, motor control and power supplies.

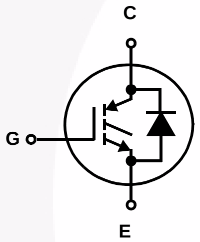
Formerly Developmental Type TA49304.

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTG18N120BND	TO-247	18N120BND

NOTE: When ordering, use the entire part number.

Symbol

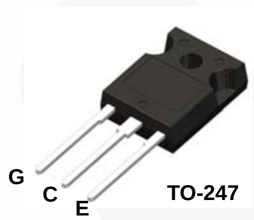


Features

- 26 A, 1200 V, T_C = 110°C
- Low Saturation Voltage: V_{CE}(sat) = 2.45 V @ I_C = 18 A
- Typical Fall Time . . . . 140ns at T_J = 150°C
- Short Circuit Rating
- Low Conduction Loss

Packaging

JEDEC STYLE TO-247



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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		Ratings	UNIT
Collector to Emitter Voltage	BV_{CES}	1200	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	54	A
At $T_C = 110^oC$	I_{C110}	26	A
Collector Current Pulsed (Note 1)	I_{CM}	160	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$ (Figure 2)	SSOA	100A at 1200V	
Power Dissipation Total at $T_C = 25^oC$	P_D	390	W
Power Dissipation Derating $T_C > 25^oC$		3.12	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15$ V	t_{SC}	8	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 12$ V	t_{SC}	15	µs

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 960$ V, $T_J = 125^oC$, $R_G = 3\ \Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Collector to Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\ \mu A$, $V_{GE} = 0$ V		1200	-	-	V
Emitter to Collector Breakdown Voltage	BV_{ECS}	$I_C = 10$ mA, $V_{GE} = 0$ V		15	-	-	V
Collector to Emitter Leakage Current	I_{CES}	$V_{CE} = 1200$ V	$T_C = 25^oC$	-	-	250	µA
			$T_C = 125^oC$	-	300	-	µA
			$T_C = 150^oC$	-	-	4	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 18$ A, $V_{GE} = 15$ V	$T_C = 25^oC$	-	2.45	2.7	V
			$T_C = 150^oC$	-	3.8	4.2	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 150\ \mu A$, $V_{CE} = V_{GE}$		6.0	7.0	-	V
Gate to Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20$ V		-	-	±250	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 3\Omega$, $V_{GE} = 15$ V, L = 200 µH, $V_{CE(PK)} = 1200$ V		100	-	-	A
Gate to Emitter Plateau Voltage	V_{GEP}	$I_C = 18$ A, $V_{CE} = 600$ V		-	10.5	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = 18$ A, $V_{CE} = 600$ V	$V_{GE} = 15$ V	-	165	200	nC
			$V_{GE} = 20$ V	-	220	250	nC
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 25^oC$ $I_{CE} = 18$ A $V_{CE} = 960$ V $V_{GE} = 15$ V $R_G = 3\ \Omega$ L = 1 mH Test Circuit (Figure 20)		-	23	28	ns
Current Rise Time	t_{rI}			-	17	22	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$			-	170	200	ns
Current Fall Time	t_{fI}			-	90	140	ns
Turn-On Energy	E_{ON}			-	1.9	2.4	mJ
Turn-Off Energy (Note 3)	E_{OFF}			-	1.8	2.2	mJ

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 150^oC$ $I_{CE} = 18$ A $V_{CE} = 960$ V $V_{GE} = 15$ V $R_G = 3\ \Omega$ L = 1 mH Test Circuit (Figure 20)	-	21	26	ns
Current Rise Time	t_{rI}		-	17	22	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	205	240	ns
Current Fall Time	t_{fI}		-	140	200	ns
Turn-On Energy	E_{ON}		-	3.7	4.9	mJ
Turn-Off Energy (Note 3)	E_{OFF}		-	2.6	3.1	mJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 18$ A	-	2.6	3.2	V
Diode Reverse Recovery Time	t_{rr}	$I_{EC} = 18$ A, $dI_{EC}/dt = 200$ A/μs	-	60	75	ns
		$I_{EC} = 2$ A, $dI_{EC}/dt = 200$ A/μs	-	44	55	ns
Thermal Resistance Junction To Case	$R_{\theta JC}$	IGBT	-	-	0.32	$^oC/W$
		Diode	-	-	0.75	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0$ A). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves Unless Otherwise Specified

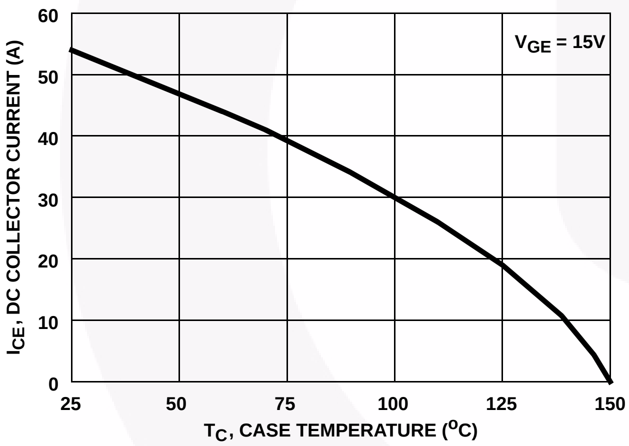

FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE

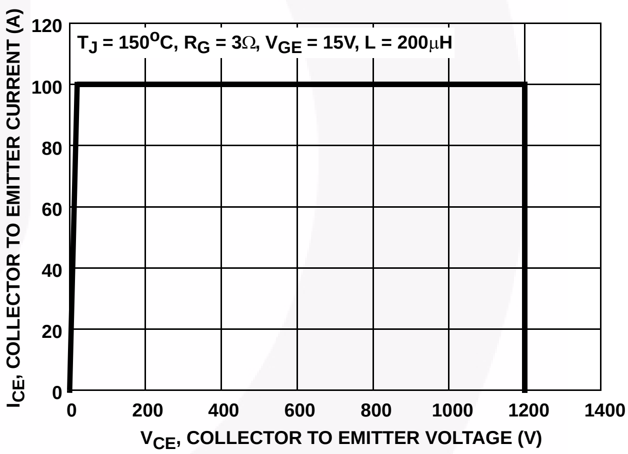

FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA

Typical Performance Curves Unless Otherwise Specified **(Continued)**

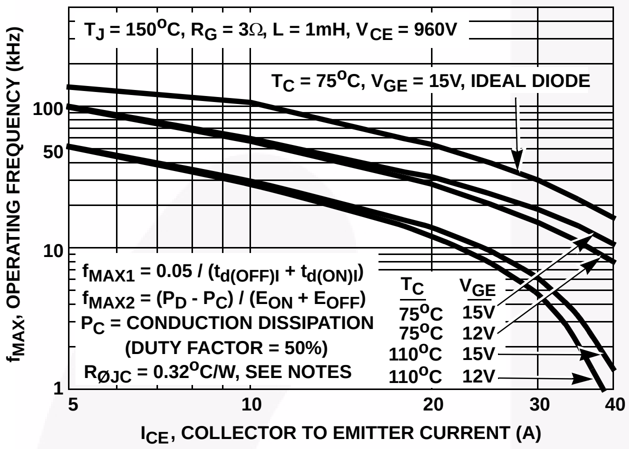

FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

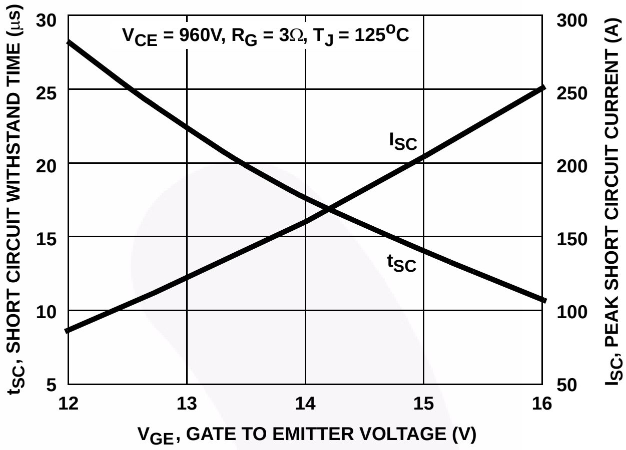

FIGURE 4. SHORT CIRCUIT WITHSTAND TIME

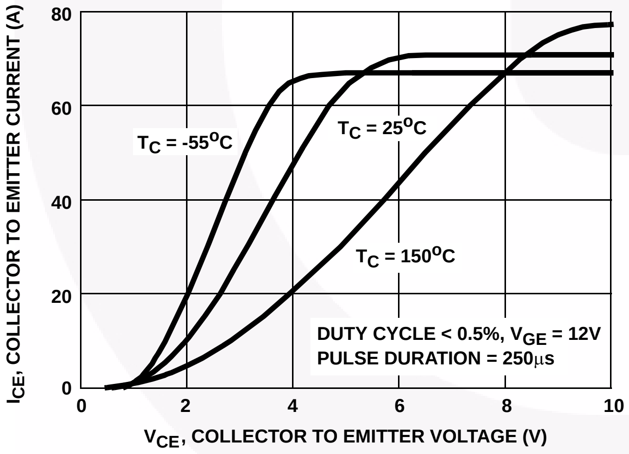

FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

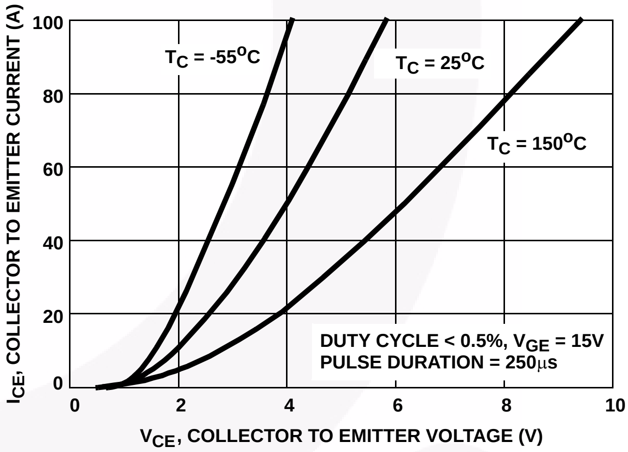

FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

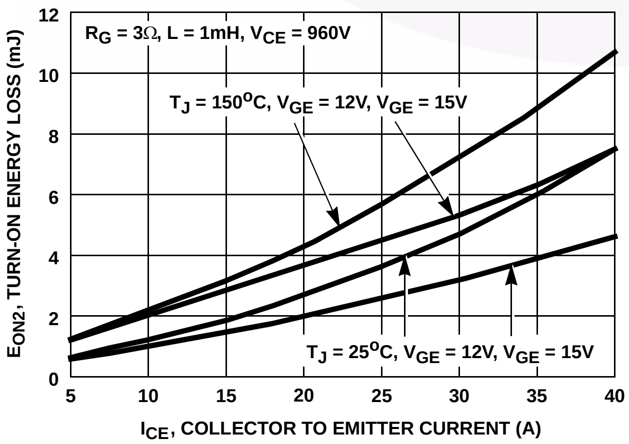

FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

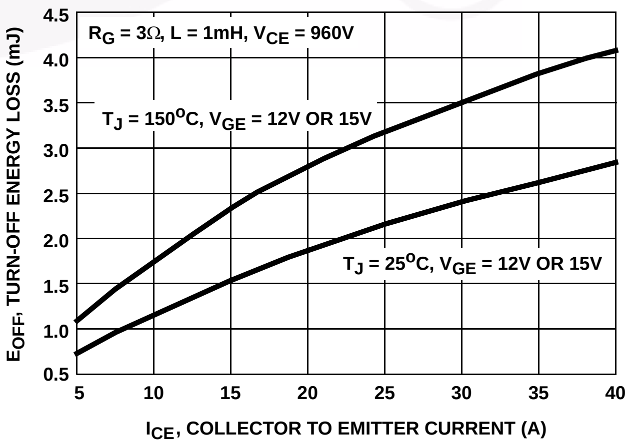

FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

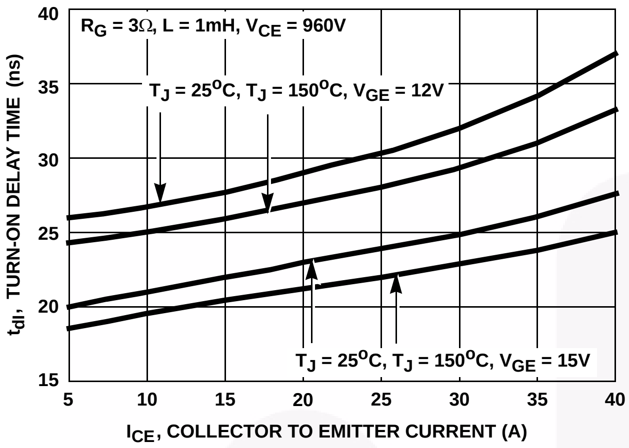

FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

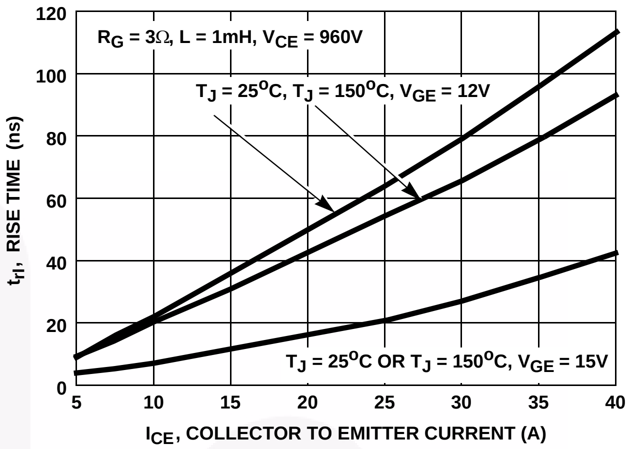

FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

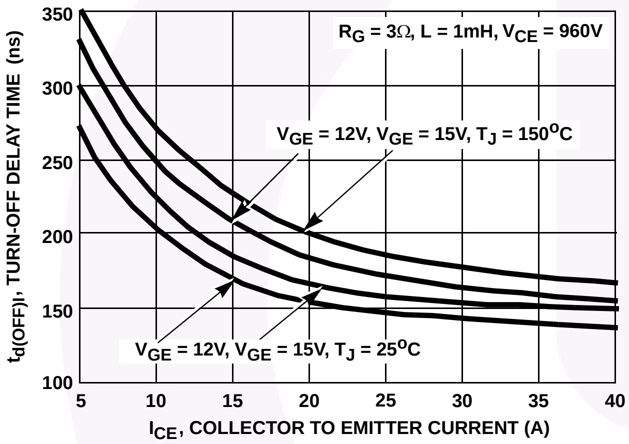

FIGURE 11. TURN-OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

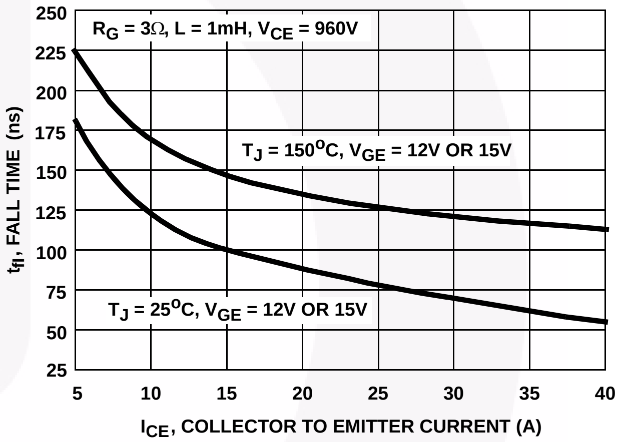

FIGURE 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT

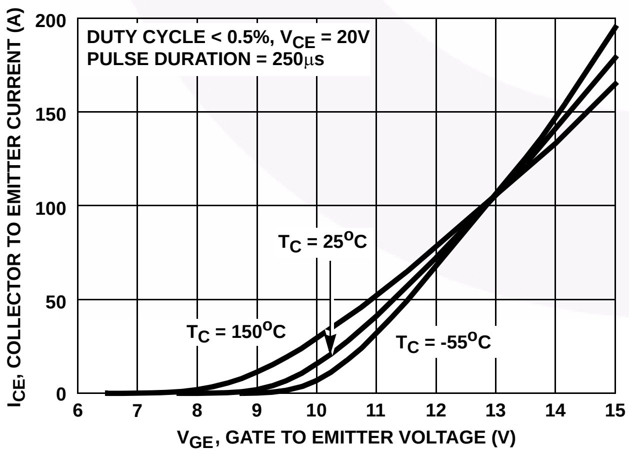

FIGURE 13. TRANSFER CHARACTERISTIC

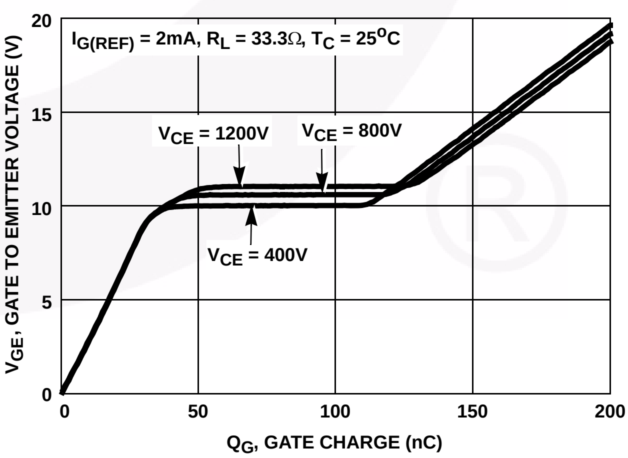

FIGURE 14. GATE CHARGE WAVEFORMS

Typical Performance Curves Unless Otherwise Specified **(Continued)**

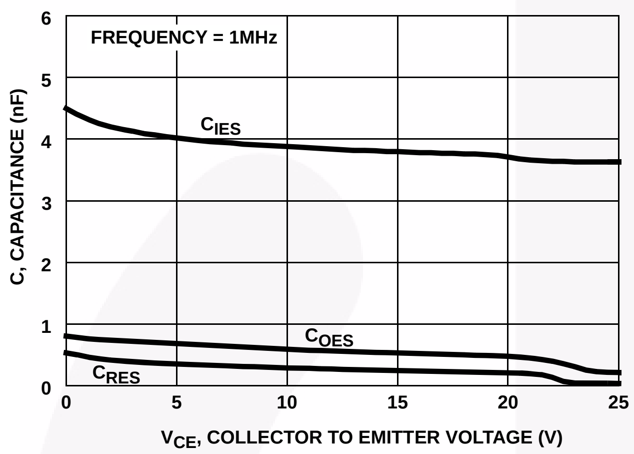

FIGURE 15. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

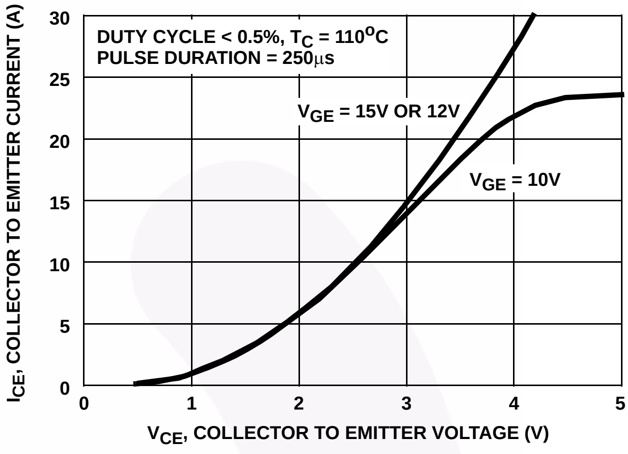

FIGURE 16. COLLECTOR TO EMITTER ON-STATE VOLTAGE

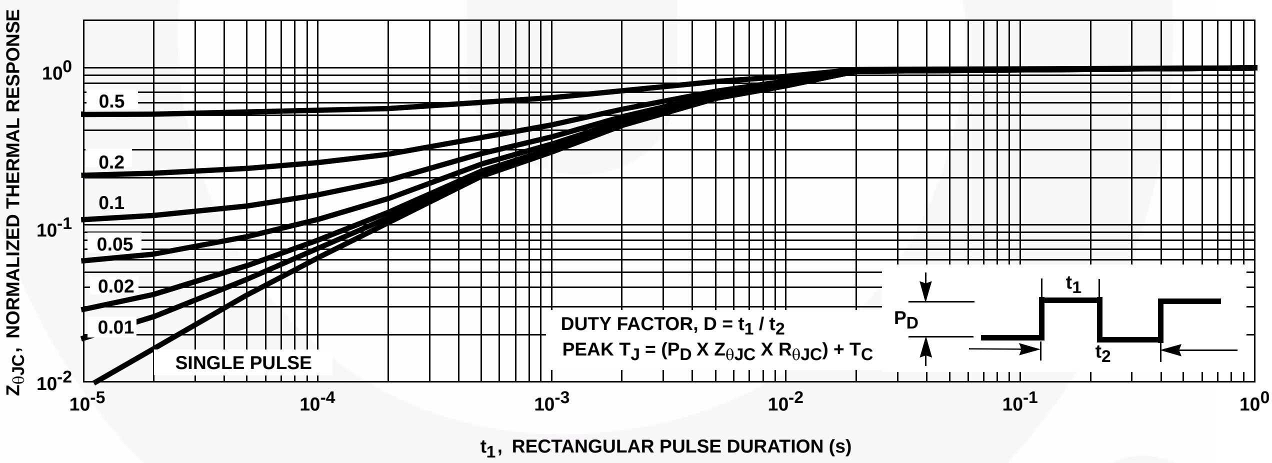

FIGURE 17. NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

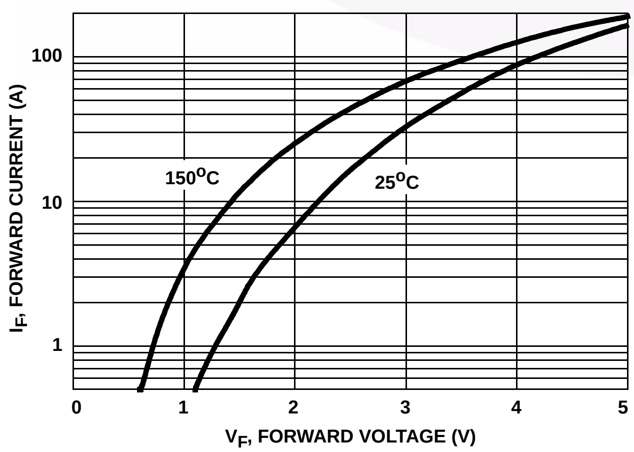

FIGURE 18. DIODE FORWARD CURRENT vs FORWARD VOLTAGE DROP

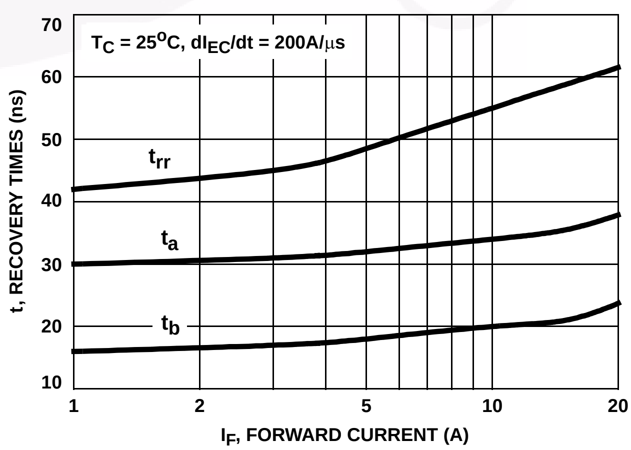

FIGURE 19. RECOVERY TIMES vs FORWARD CURRENT

Test Circuits and Waveforms

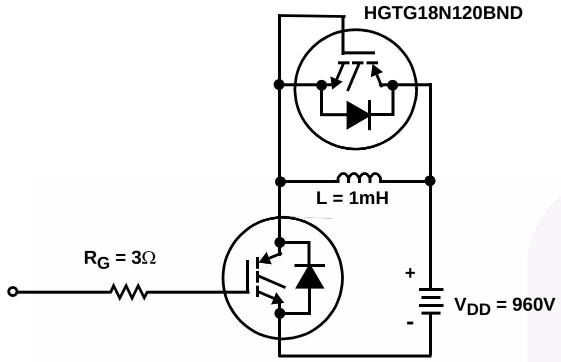

FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

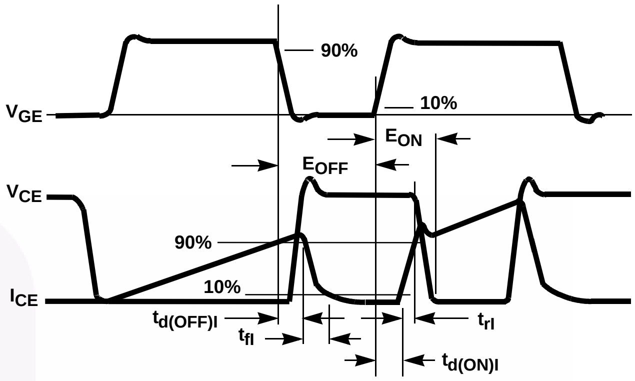

FIGURE 21. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 21. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 21. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

Mechanical Dimensions

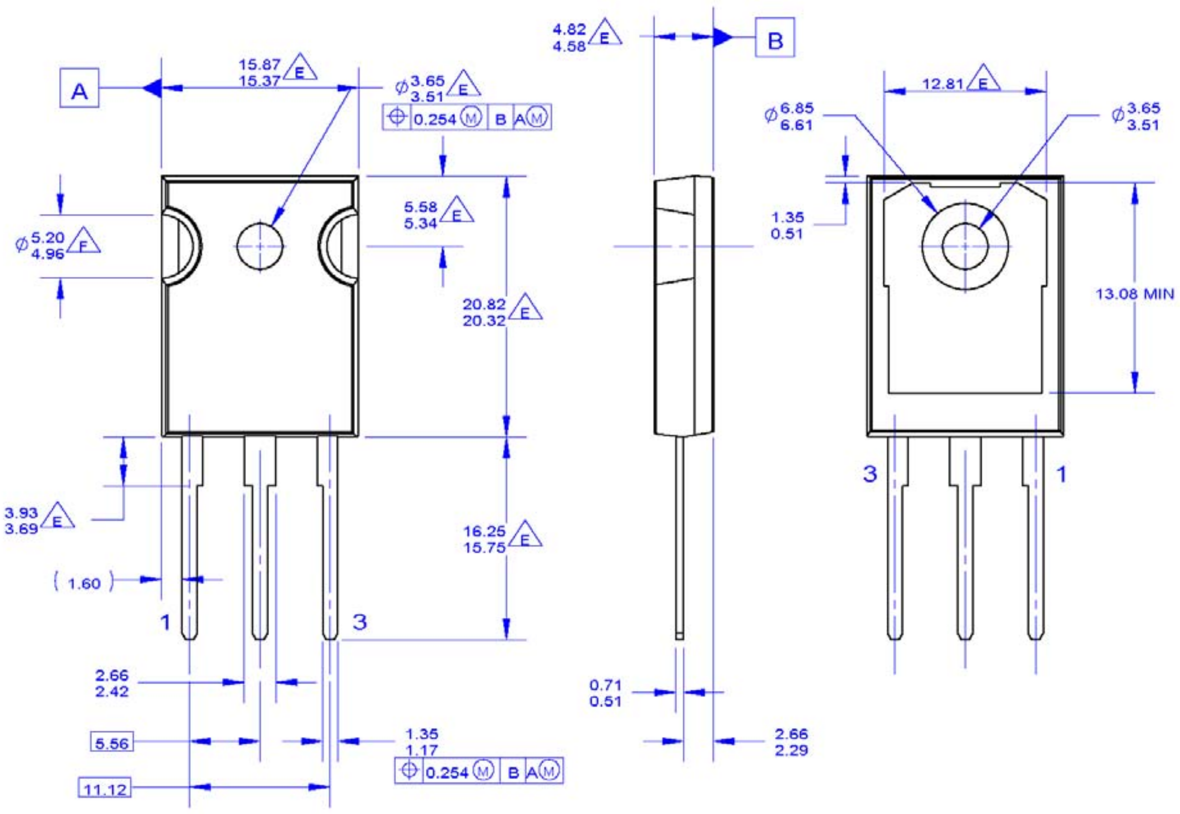

Figure 22. TO-247 3L - TO-247,MOLDED,3 LEAD,JEDEC VARIATION AB

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