

# J211 / MMBFJ211 N-Channel RF Amplifier

## Description

This device is designed for HF/VHF mixer/amplifier and applications where process 50 is not adequate. Sufficient gain and low-noise for sensitive receivers. Sourced from process 90.

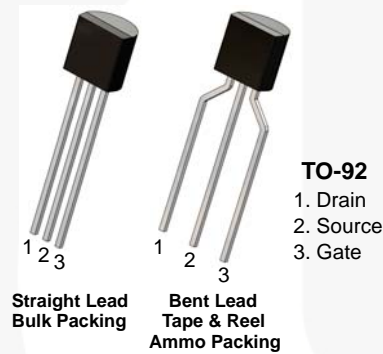


Figure 1. J211 Device Package

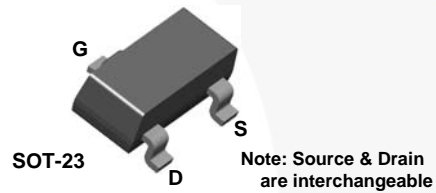


Figure 2. MMBFJ211 Device Package

## Ordering Information

Part Number	Top Mark	Package	Packing Method
J211_D74Z	J211	TO-92 3L	Ammo
MMBFJ211	62W	SOT-23 3L	Tape and Reel

## Absolute Maximum Ratings<sup>(1), (2)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{DG}$	Drain-Gate Voltage	25	V
$V_{GS}$	Gate-Source Voltage	-25	V
$I_{GF}$	Forward Gate Current	10	mA
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### Notes:

1. These ratings are based on a maximum junction temperature of  $150^\circ\text{C}$ .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

## Thermal Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Max.		Unit
		J211 <sup>(3)</sup>	MMBFJ211 <sup>(3)</sup>	
$P_D$	Total Device Dissipation	350	225	mW
	Derate Above $25^\circ\text{C}$	2.8	1.8	mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	125		$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	357	556	$^\circ\text{C}/\text{W}$

### Note:

3. Device mounted on FR-4 PCB 36mm x 18mm x 1.5mm; mounting pad for the collector lead minimum  $6\text{cm}^2$ .

## Electrical Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
<b>Off Characteristics</b>					
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = 1.0 \mu\text{A}, V_{DS} = 0$	-25		V
$I_{GSS}$	Gate Reverse Current	$V_{GS} = 15 \text{ V}, V_{DS} = 0$		-100	pA
$V_{GS(off)}$	Gate-Source Cut-Off Voltage	$V_{DS} = 15 \text{ V}, I_D = 1.0 \text{ nA}$	-2.5	-4.5	V
<b>On Characteristics</b>					
$I_{DSS}$	Zero-Gate Voltage Drain Current <sup>(4)</sup>	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	7.0	20	mA
<b>Small Signal Characteristics</b>					
$g_{fs}$	Common Source Forward Transconductance	$V_{DS} = 15 \text{ V}, V_{GS} = 0,$ $f = 1.0 \text{ kHz}$	7000	12000	$\mu\text{mhos}$
$g_{oss}$	Common Source Output Conductance	$V_{DS} = 15 \text{ V}, V_{GS} = 0,$ $f = 1.0 \text{ kHz}$		200	$\mu\text{mhos}$

### Note:

4. Pulse test: pulse width  $\leq 300 \mu\text{s}$

Typical Performance Characteristics

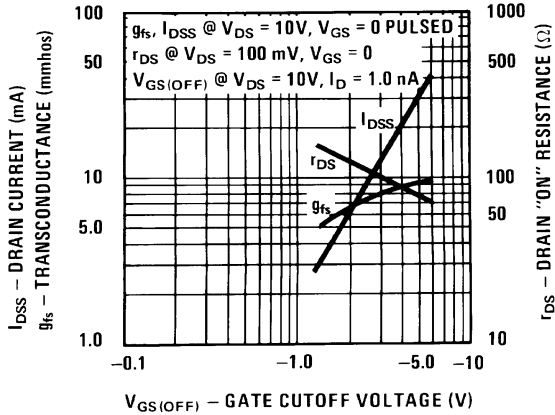


Figure 3. Parameter Interactions

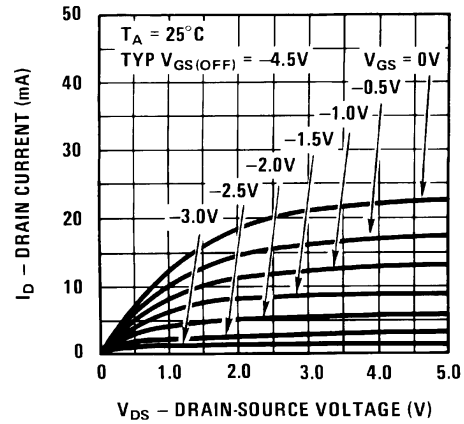


Figure 4. Common Drain-Source

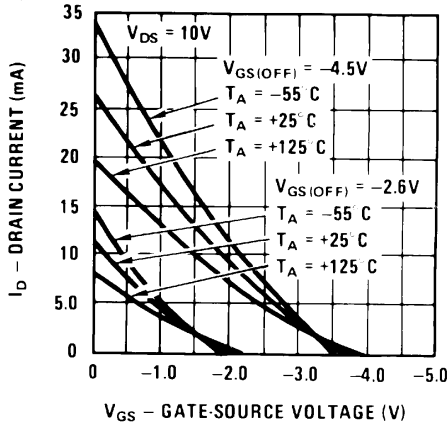


Figure 5. Transfer Characteristics

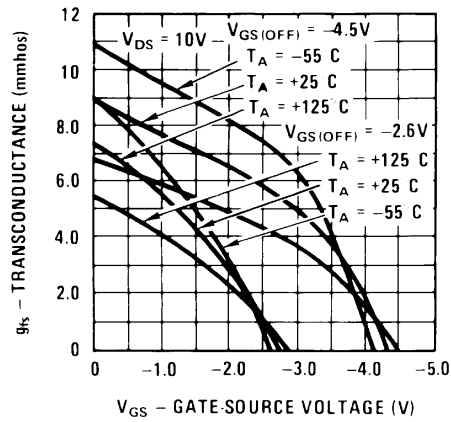


Figure 6. Transfer Characteristics

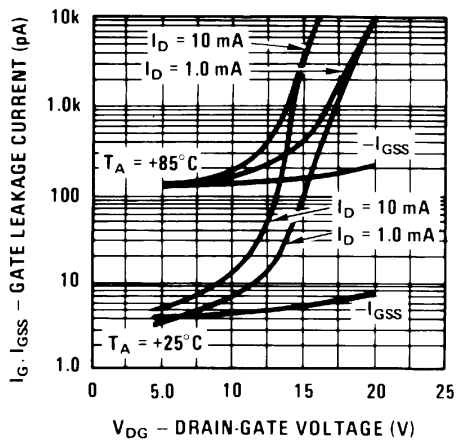


Figure 7. Leakage Current vs. Voltage

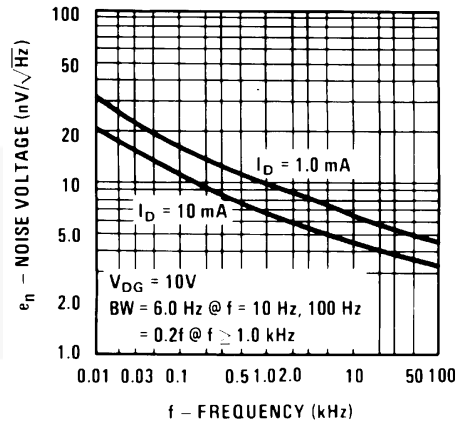


Figure 8. Noise Voltage vs. Frequency

Typical Performance Characteristics (Continued)

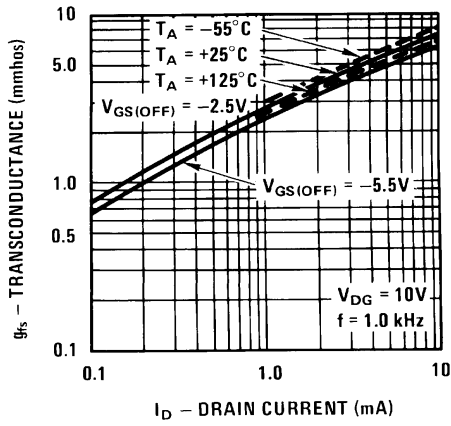


Figure 9. Transconductance vs. Drain Current

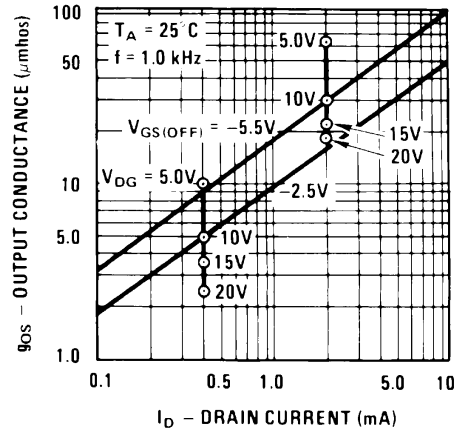


Figure 10. Output Conductance vs. Drain Current

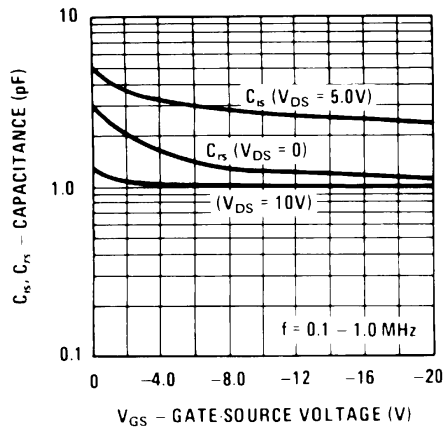


Figure 11. Capacitance vs. Voltage

Common Source Characteristics

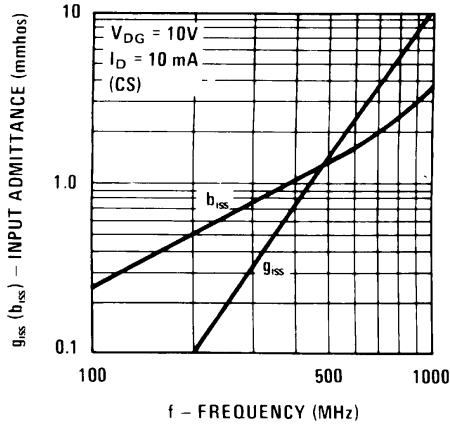


Figure 12. Input Admittance

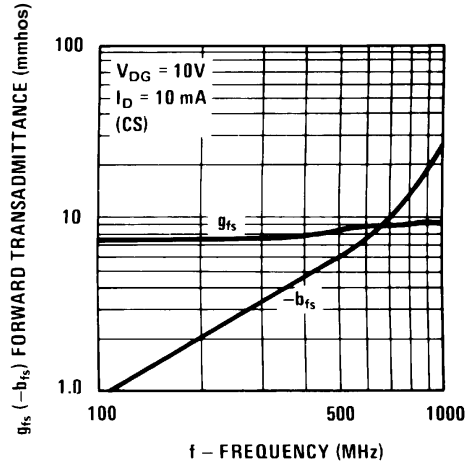


Figure 13. Forward Transadmittance

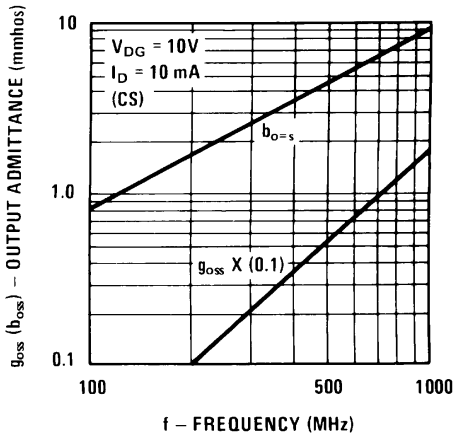


Figure 14. Output Admittance

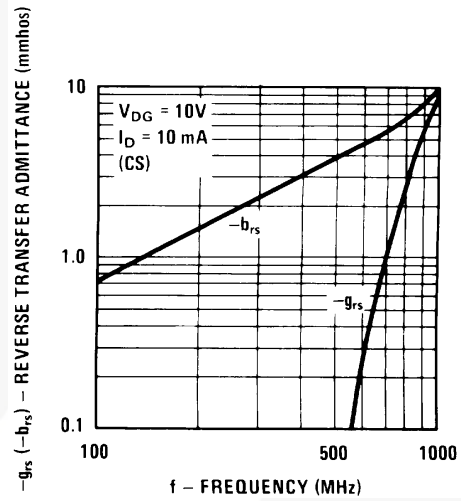


Figure 15. Reverse Transadmittance

Common Gate Characteristics

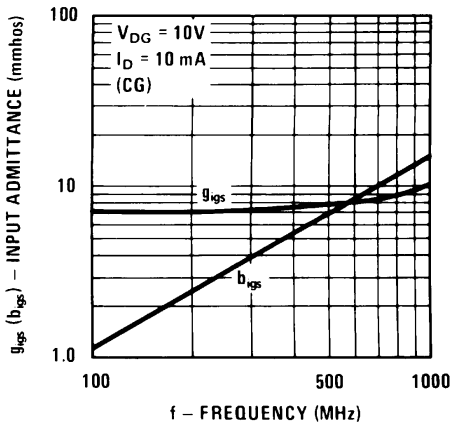


Figure 16. Input Admittance

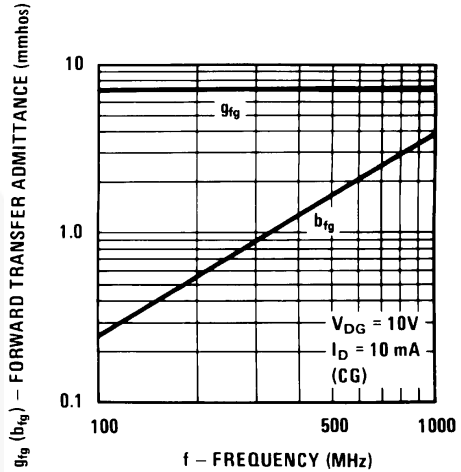


Figure 17. Forward Transadmittance

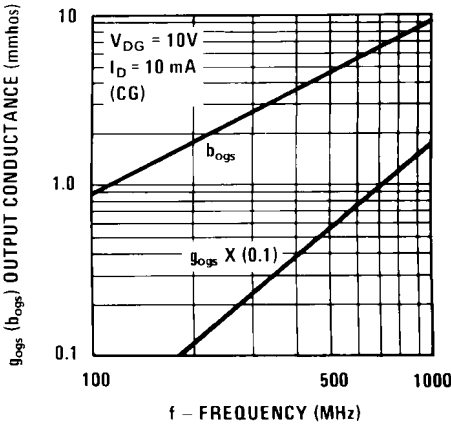


Figure 18. Output Admittance

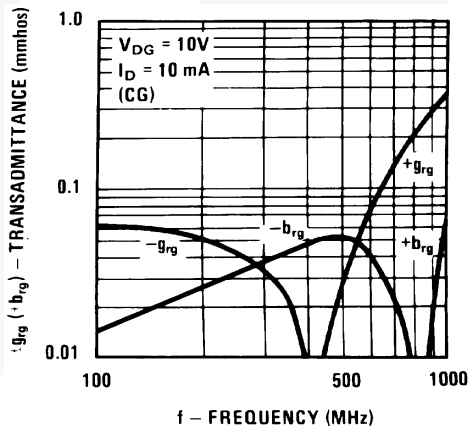
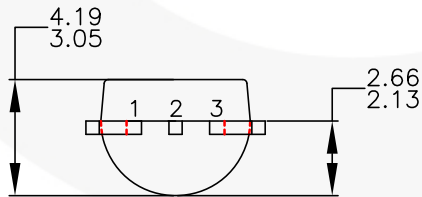
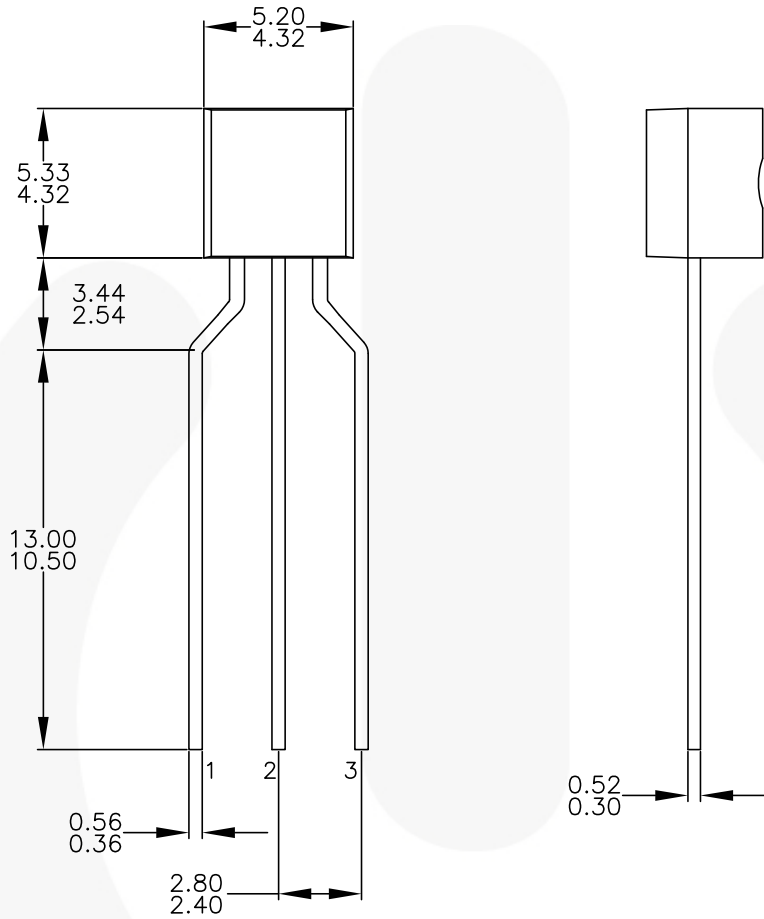


Figure 19. Reverse Transadmittance

Physical Dimensions

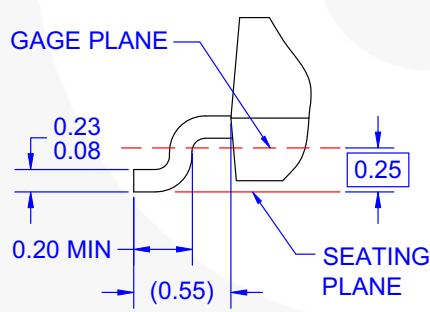
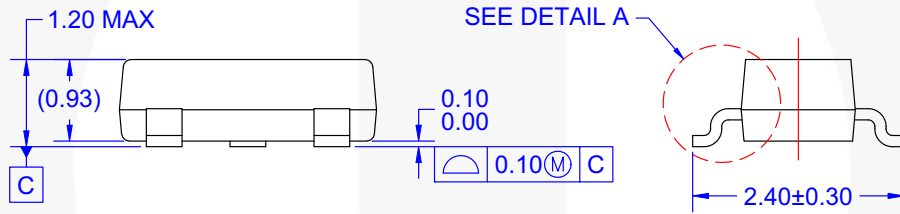
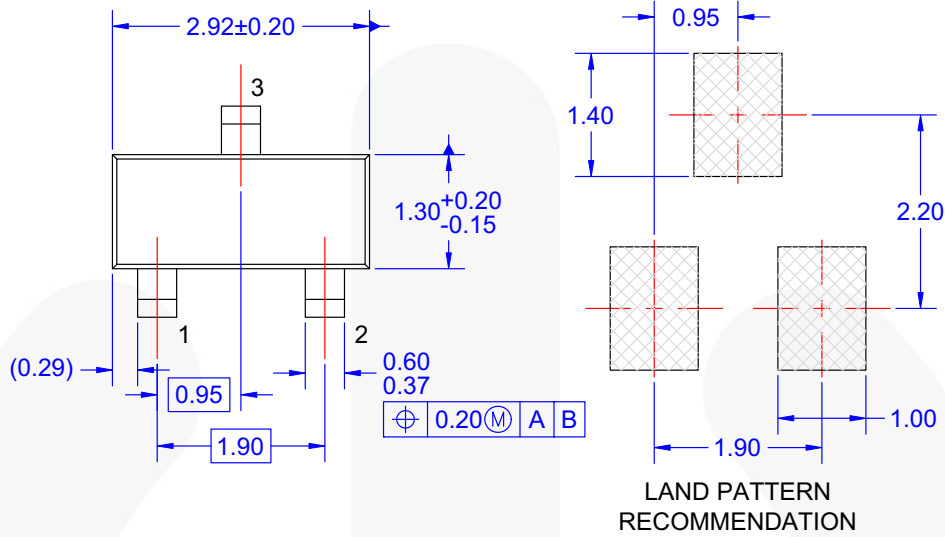


NOTES: UNLESS OTHERWISE SPECIFIED

- A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREV3.
- E. FAIRCHILD SEMICONDUCTOR.

Figure 20. 3-Lead, TO-92, Molded, 0.2 In Line Spacing Lead Form

Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
- E) DRAWING FILE NAME: MA03DREV10

**DETAIL A**  
SCALE: 2X






**Figure 21. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE**





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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