

# MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## CoolMOS™ CE

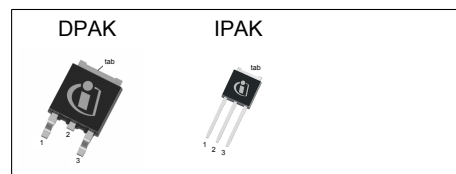
800V CoolMOS™ CE Power Transistor  
IPx80R2K8CE

## Data Sheet

Rev. 2.1  
Final

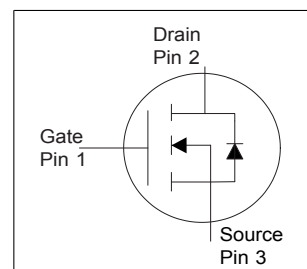
## 1 Description

CoolMOS™ CE is a revolutionary technology for high voltage power MOSFETs. The high voltage capability combines safety with performance and ruggedness to allow stable designs at highest efficiency level. CoolMOS™ 800V CE comes with a selected package choice offering the benefit of reduced system costs and higher power density designs.



### Features <sup>1)</sup>

- High voltage technology
- Extreme dv/dt rated
- High peak current capability
- Low gate charge
- Low effective capacitances
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- Pb-free lead plating; RoHS compliant; available with halogen free and non-halogen free mold compound<sup>1)</sup>



### Benefits

- Increased power density solutions due to smaller package
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to low operating temperatures



### Applications

- LED Lighting for retrofit applications in QR Flyback topology

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_j=25^{\circ}C$	800	V
$R_{DS(on),max}$	2.8	$\Omega$
$Q_{g,typ}$	12	nC
$I_{D,pulse}$	6	A
$V_{GS(th),typ}$	3	V
$C_{O(tr),typ}$	26	pF

Type / Ordering Code	Package	Marking	Related Links
IPD80R2K8CE	PG-TO 252	8R2K8CE	see Appendix A
IPU80R2K8CE	PG-TO 251		

<sup>1)</sup> Halogen free version is available with OPN: IPD80R2K8CEAT

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## 2 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	1.9 1.1	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	6	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	90	mJ	$I_D = 1\text{A}; V_{DD} = 50\text{V}$
Avalanche energy, repetitive	$E_{AR}$	-	-	0.05	mJ	$I_D = 1\text{A}; V_{DD} = 50\text{V}$
Avalanche current, repetitive	$I_{AR}$	-	-	1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 640\text{V}$
Gate source voltage	$V_{GS}$	-20 -30	-	20 30	V	static; AC ( $f > 1\text{ Hz}$ )
Power dissipation (non FullPAK) TO-252, TO-251	$P_{tot}$	-	-	42	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Continuous diode forward current	$I_S$	-	-	1.9	A	$T_C = 25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	6	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	4	V/ns	$V_{DS} = 0 \dots 400\text{V}, I_{SD} \leq I_S, T_j = 25^\circ\text{C}$
Maximum diode commutation speed	$di/dt$	-	-	400	A/ $\mu\text{s}$	$V_{DS} = 0 \dots 400\text{V}, I_{SD} \leq I_S, T_j = 25^\circ\text{C}$

## 3 Thermal characteristics

**Table 3 Thermal characteristics DPAK, IPAK**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	3	$^\circ\text{C}/\text{W}$	-
Thermal resistance, junction - ambient <sup>4)</sup>	$R_{thJA}$	-	- 35	62 -	$^\circ\text{C}/\text{W}$	SMD version, device on PCB, minimal footprint SMD version, device on PCB, 6cm <sup>2</sup> cooling area <sup>4)</sup>
Soldering temperature, wave- & reflowsoldering allowed	$T_{sold}$	-	-	260	$^\circ\text{C}$	reflow MSL 1

<sup>1)</sup> Limited by  $T_{j,max}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$ .

<sup>3)</sup> Identical low side and high side switch with identical  $R_G$ .

<sup>4)</sup> Device on 40mm\*40mm\*1.5mm one layer epoxy PCB FR4 with 6cm<sup>2</sup> copper area (thickness 70 $\mu\text{m}$ ) for drain connection. PCB is vertical without air stream cooling.

## 4 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS}=0V, I_D=0.25mA$
Gate threshold voltage	$V_{(GS)th}$	2.1	3	3.9	V	$V_{DS}=V_{GS}, I_D=0.12mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	5	$\mu A$	$V_{DS}=800V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=800V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.4 6.5	2.8 -	$\Omega$	$V_{GS}=10V, I_D=1.1A, T_j=25^\circ C$ $V_{GS}=10V, I_D=1.1A, T_j=150^\circ C$
Gate resistance	$R_G$	-	1.2	-	$\Omega$	$f=1\text{ MHz}, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	290	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	$C_{oss}$	-	13	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	11	-	pF	$V_{GS}=0V, V_{DS}=0\dots 480V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	26	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots 480V$
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	$V_{DD}=400V, V_{GS}=0/10V, I_D=1.9A, R_G=47\Omega$
Rise time	$t_r$	-	15	-	ns	$V_{DD}=400V, V_{GS}=0/10V, I_D=1.9A, R_G=47\Omega$
Turn-off delay time	$t_{d(off)}$	-	72	-	ns	$V_{DD}=400V, V_{GS}=0/10V, I_D=1.9A, R_G=47\Omega$
Fall time	$t_f$	-	18	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=1.9A, R_G=47\Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	1.5	-	nC	$V_{DD}=640V, I_D=1.9A, V_{GS}=0\text{ to }10V$
Gate to drain charge	$Q_{gd}$	-	6	-	nC	$V_{DD}=640V, I_D=1.9A, V_{GS}=0\text{ to }10V$
Gate charge total	$Q_g$	-	12	-	nC	$V_{DD}=640V, I_D=1.9A, V_{GS}=0\text{ to }10V$
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	$V_{DD}=640V, I_D=1.9A, V_{GS}=0\text{ to }10V$

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{(BR)DSS}$

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{(BR)DSS}$

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1	1.2	V	$V_{GS}=0V, I_F=1.9A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	520	-	ns	$V_R=400V, I_F=1.9A, di_F/dt=100A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	2	-	$\mu C$	$V_R=400V, I_F=1.9A, di_F/dt=100A/\mu s$
Peak reverse recovery current	$I_{rrm}$	-	6	-	A	$V_R=400V, I_F=1.9A, di_F/dt=100A/\mu s$

## 5 Electrical characteristics diagrams

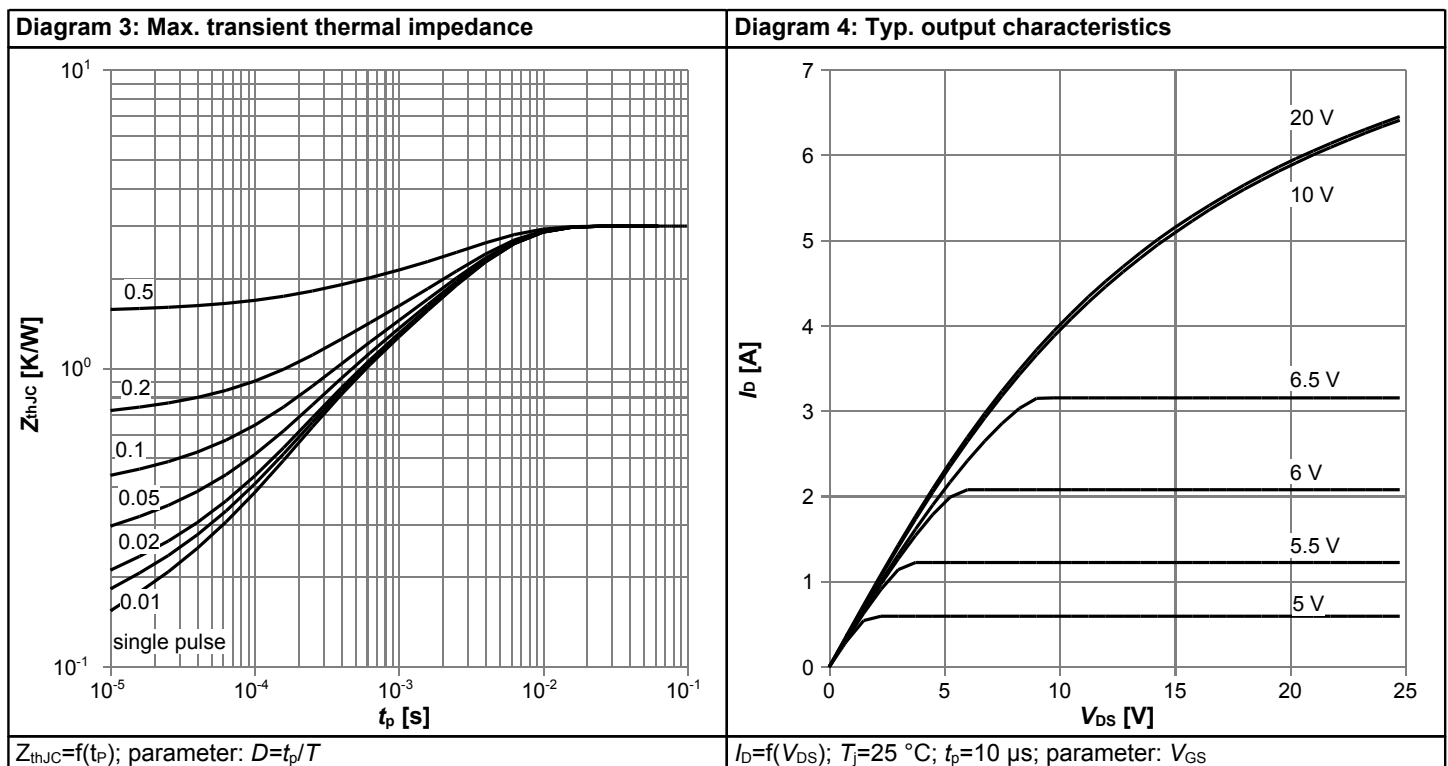
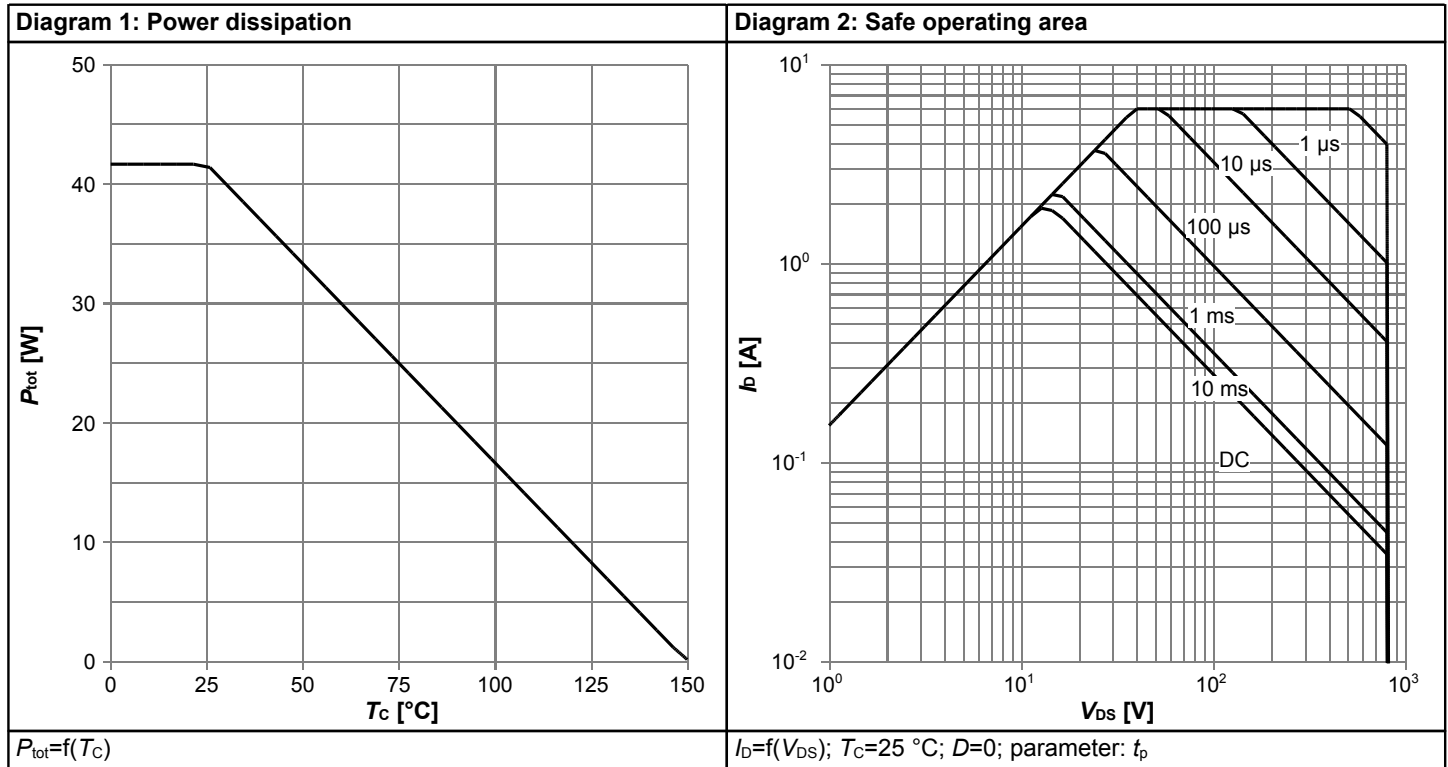
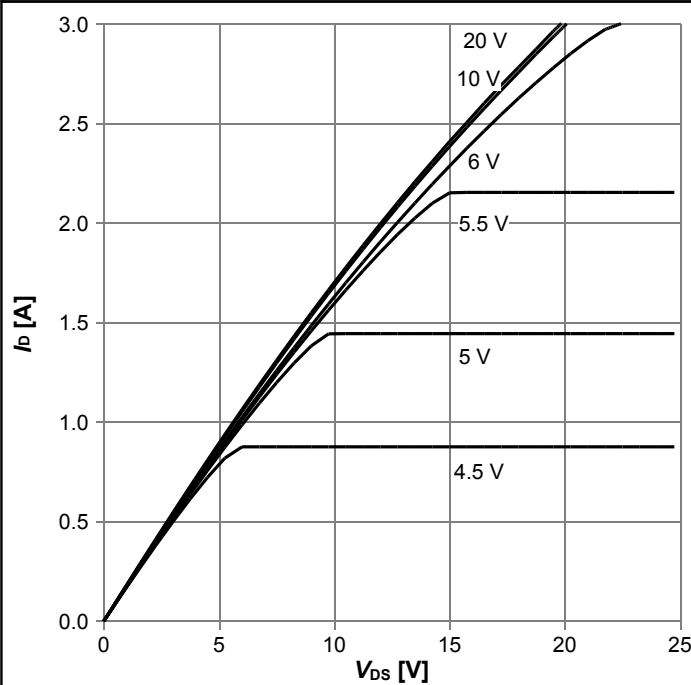
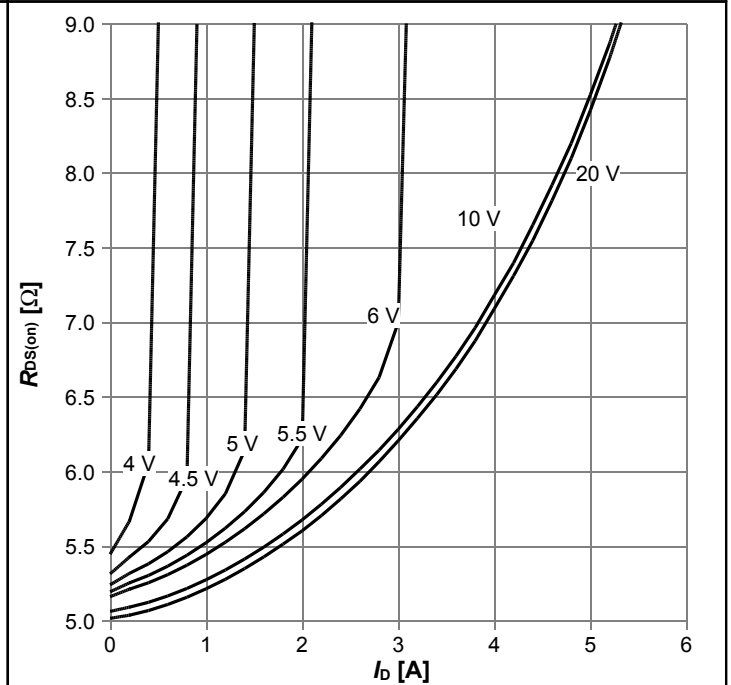


Diagram 5: Typ. output characteristics



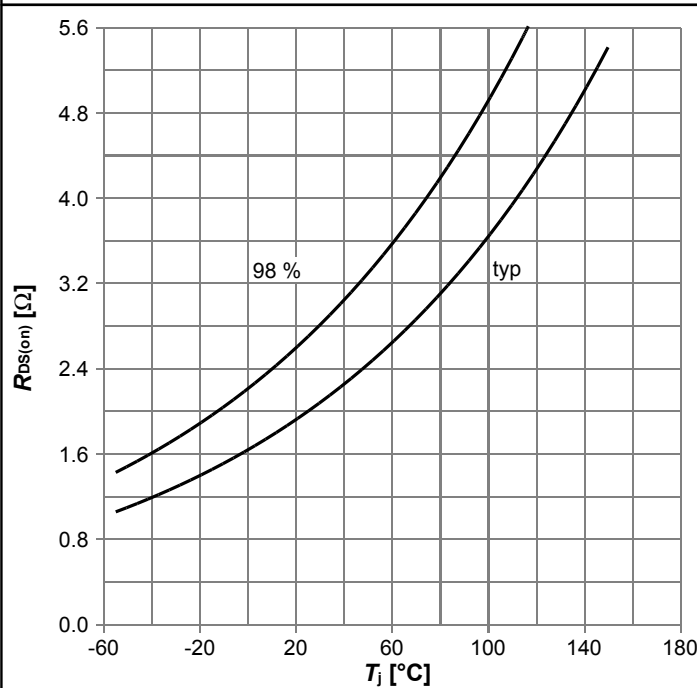
$I_D=f(V_{DS}); T_j=150\text{ }^\circ\text{C}; t_p=10\text{ }\mu\text{s};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on-state resistance



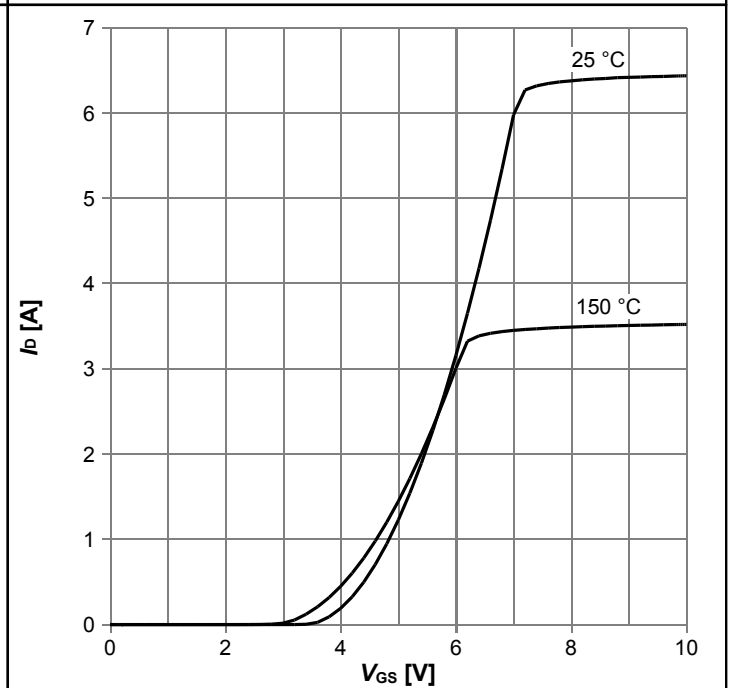
$R_{DS(on)}=f(I_D); T_j=150\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 7: Drain-source on-state resistance



$R_{DS(on)}=f(T_j); I_D=1.1\text{ A}; V_{GS}=10\text{ V}$

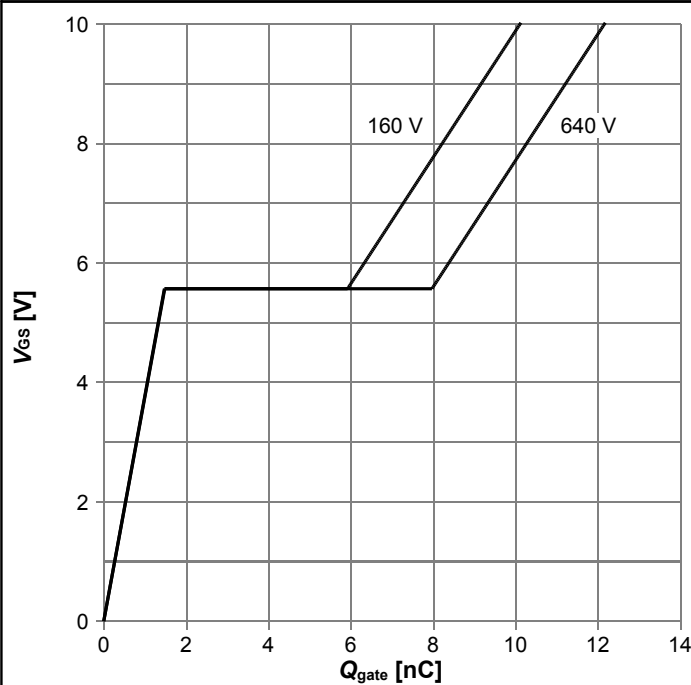
Diagram 8: Typ. transfer characteristics



$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}; t_p=10\text{ }\mu\text{s};$  parameter:  $T_j$

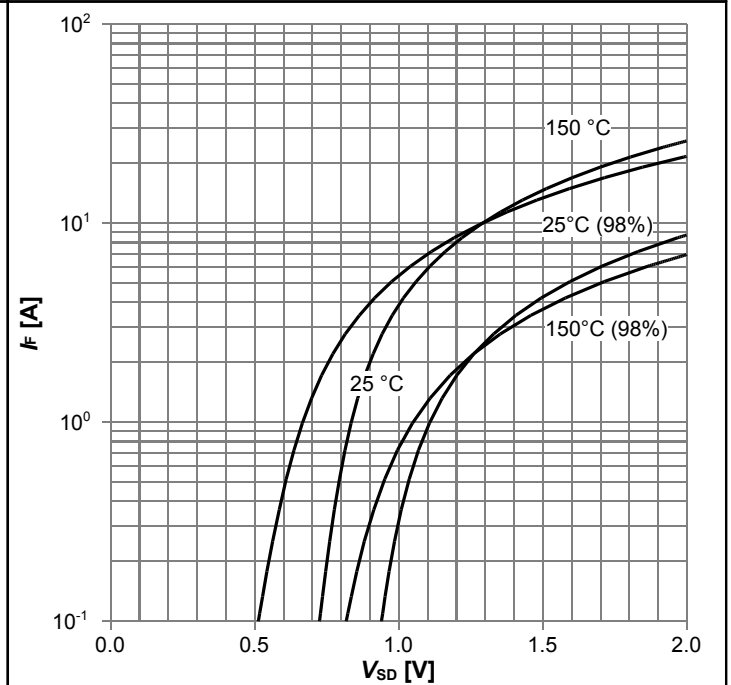


Diagram 9: Typ. gate charge



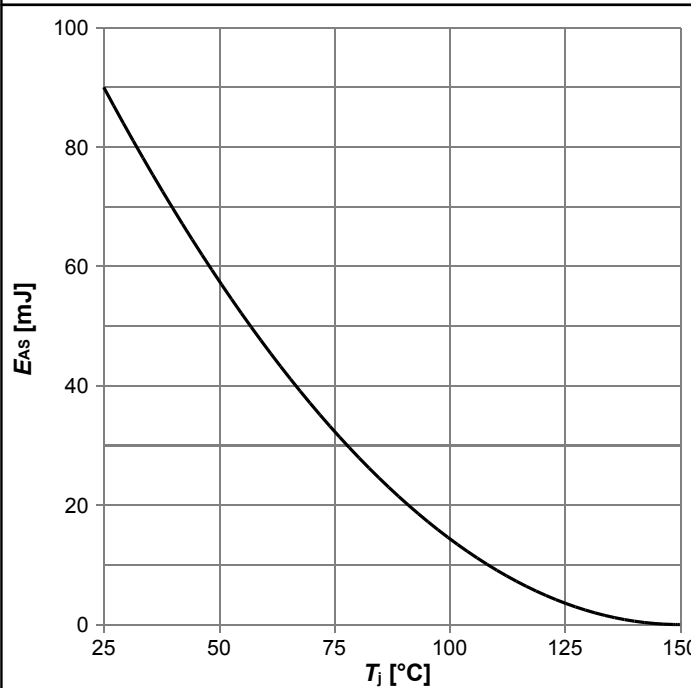
$V_{GS}=f(Q_{gate}); I_D=1.9 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 10: Forward characteristics of reverse diode



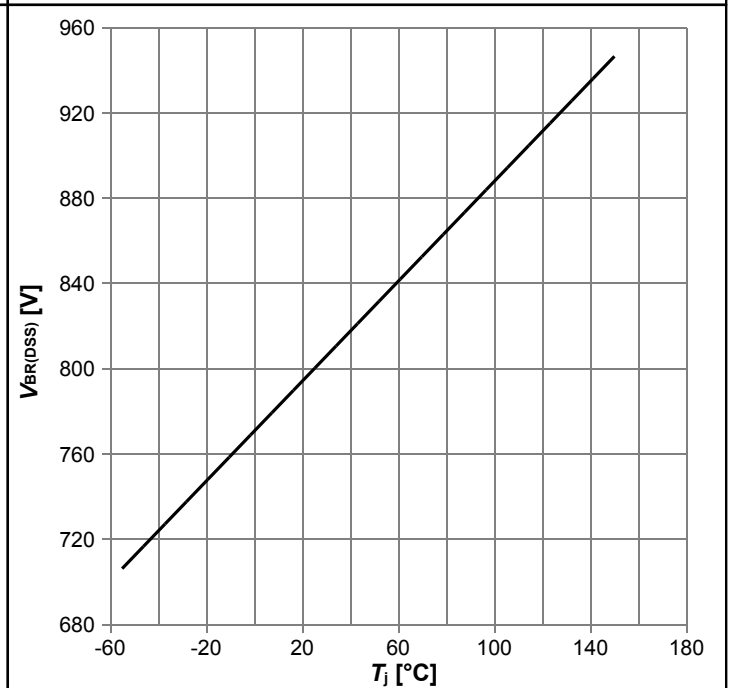
$I_F=f(V_{SD}); t_p=10 \mu\text{s}; \text{parameter: } T_j$

Diagram 11: Avalanche energy



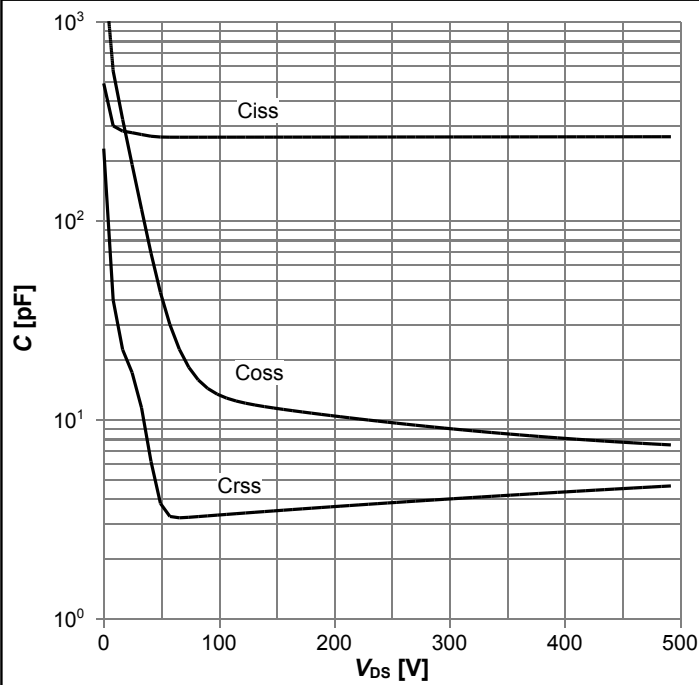
$E_{AS}=f(T_j); I_D=1 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 12: Drain-source breakdown voltage



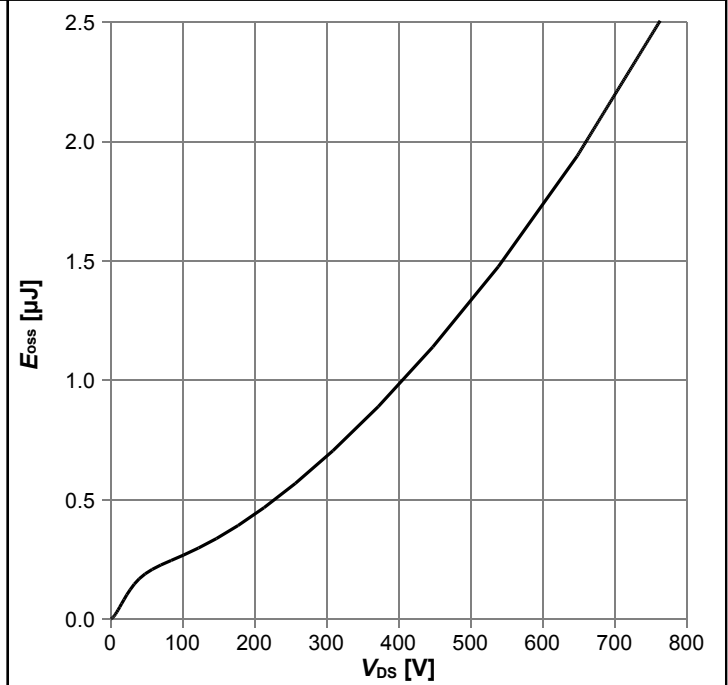
$V_{BR(DSS)}=f(T_j); I_D=0.25 \text{ mA}$

Diagram 13: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 14: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

## 6 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
<p style="text-align: center;"><math>R_{g1} = R_{g2}</math></p>	<p style="text-align: right;"> <math>t_{rr} = t_F + t_S</math>  <math>Q_{rr} = Q_F + Q_S</math> </p>

**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform

## 7 Package Outlines

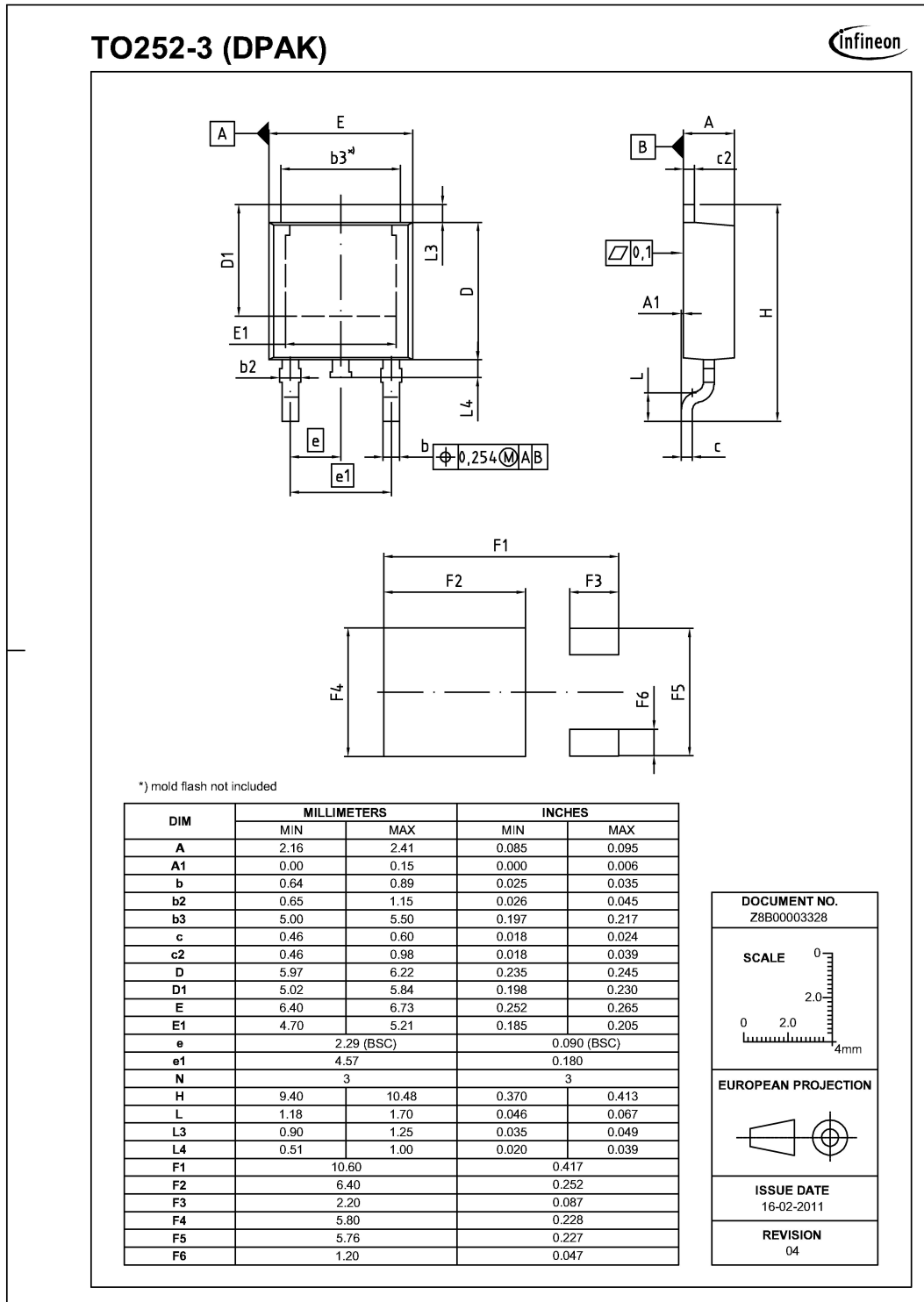
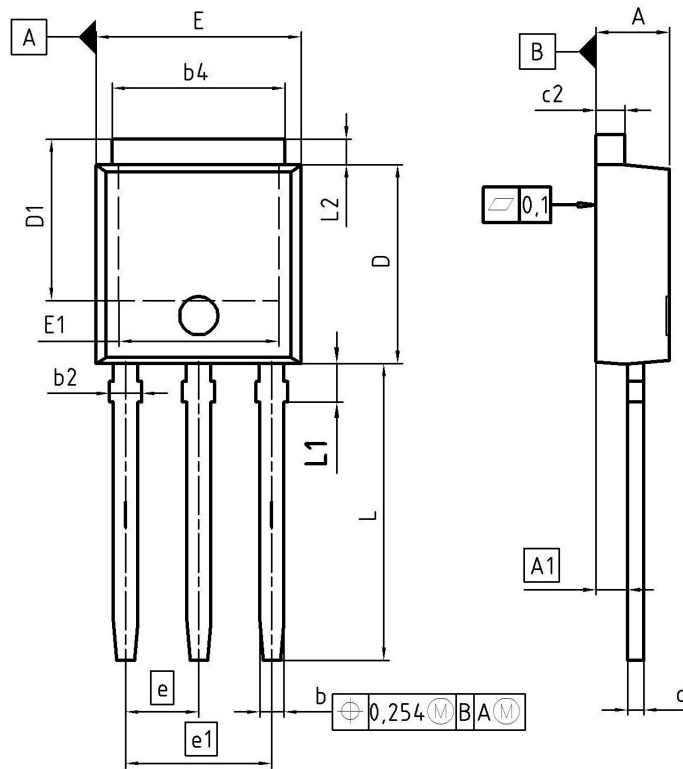


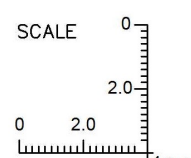
Figure 1 Outline PG-TO 252, dimensions in mm/inches




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.90	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.77	0.198	0.227
E	6.35	6.73	0.250	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	8.89	9.65	0.350	0.380
L1	1.90	2.29	0.075	0.090
L2	0.89	1.37	0.035	0.054

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Figure 2 Outline PG-TO 251, dimensions in mm/inches

## 8 Appendix A

### Table 11 Related Links

- IFX CoolMOS Webpage: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPD80R2K8CE, IPU80R2K8CE

**Revision: 2013-07-18, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-06-24	Release of final version
2.1	2013-07-18	update to halogen free mold compound

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