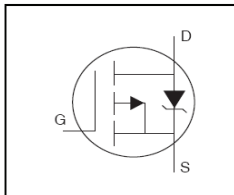


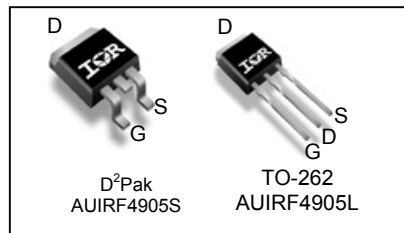
**Features**

- Advanced Planar Technology
- P-Channel MOSFET
- Low On-Resistance
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



HEXFET® Power MOSFET

<b>V<sub>DSS</sub></b>	<b>-55V</b>
<b>R<sub>DS(on)</sub> max.</b>	<b>20mΩ</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>-70A</b>
<b>I<sub>D</sub> (Package Limited)</b>	<b>-42A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Description**

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF4905L	TO-262	Tube	50	AUIRF4905L
AUIRF4905S	D²-Pak	Tube	50	AUIRF4905S
		Tape and Reel Left	800	AUIRF4905STRL

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	-70	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	-44	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	-42	
I <sub>DM</sub>	Pulsed Drain Current ①	-280	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②	140	mJ
E <sub>AS</sub> (tested)	Single Pulse Avalanche Energy Tested Value ⑥	790	
I <sub>AR</sub>	Avalanche Current ①	See Fig.15,16, 12a, 12b	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①		mJ
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ⑧	—	0.75	°C/W
R <sub>θJA</sub>	Junction-to-Ambient ( PCB Mount, steady state) ⑦⑧		40	

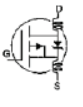
HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

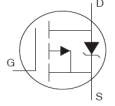
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-0.054	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	20	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -42A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
g <sub>fs</sub>	Forward Trans conductance	19	—	—	S	V <sub>DS</sub> = -25V, I <sub>D</sub> = -42A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-25	μA	V <sub>DS</sub> = -55V, V <sub>GS</sub> = 0V
		—	—	-250		V <sub>DS</sub> = -44V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> = 20V

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

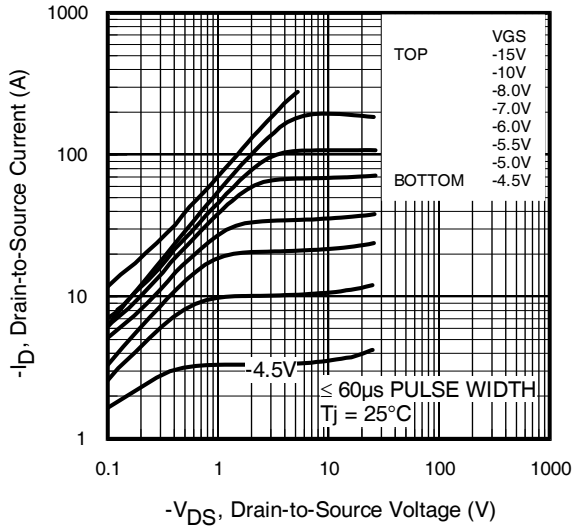
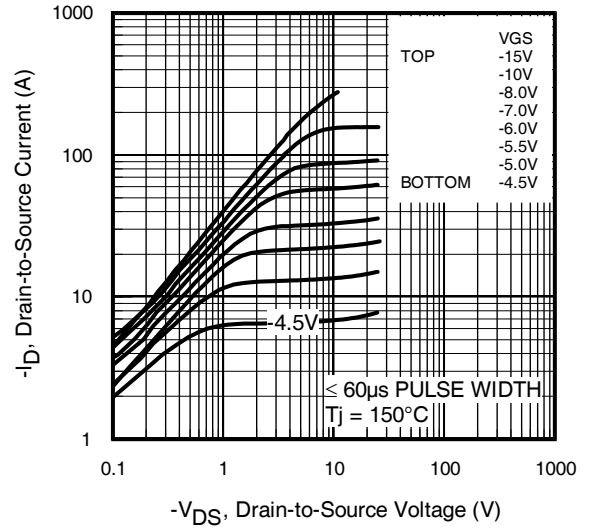
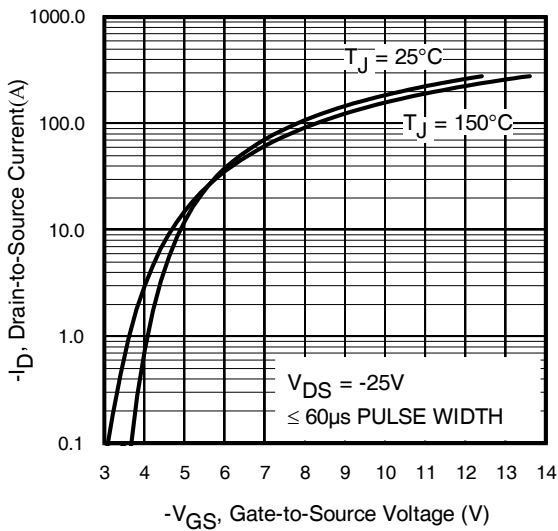
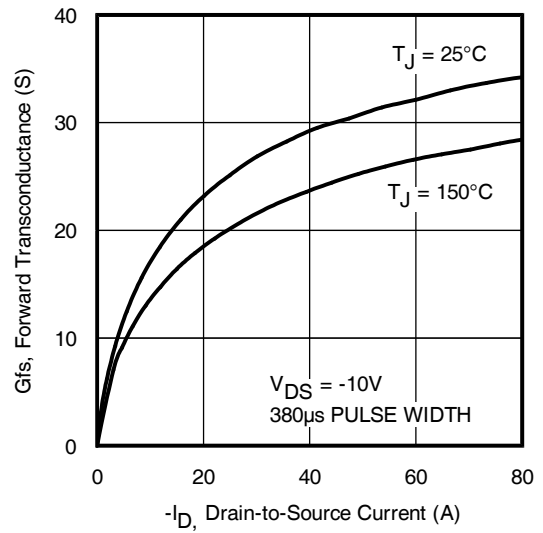
Q <sub>g</sub>	Total Gate Charge	—	120	180	nC	I <sub>D</sub> = -42A V <sub>DS</sub> = -44V V <sub>GS</sub> = -10V ③
Q <sub>gs</sub>	Gate-to-Source Charge	—	32	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	53	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	20	—	ns	V <sub>DD</sub> = -28V I <sub>D</sub> = -42A R <sub>G</sub> = 2.6Ω, V <sub>GS</sub> = -10V ③
t <sub>r</sub>	Rise Time	—	99	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	51	—		
t <sub>f</sub>	Fall Time	—	64	—		
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	3500	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = -25V f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = -1.0V f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = -44V f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to -44V ④
C <sub>oss</sub>	Output Capacitance	—	1250	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	450	—		
C <sub>oss</sub>	Output Capacitance	—	4620	—		
C <sub>oss</sub>	Output Capacitance	—	940	—		
C <sub>oss eff.</sub>	Effective Output Capacitance	—	1530	—		

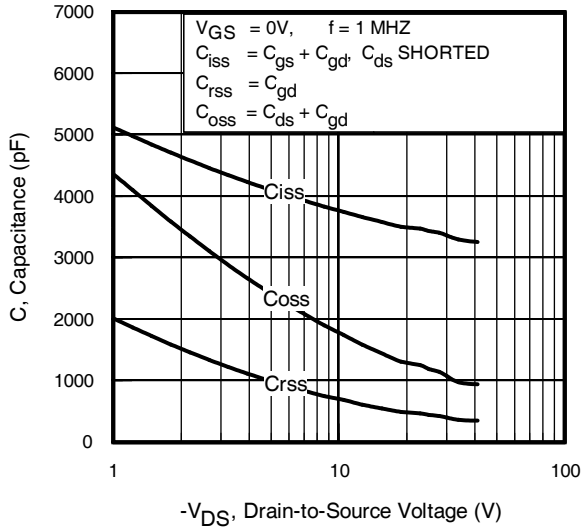
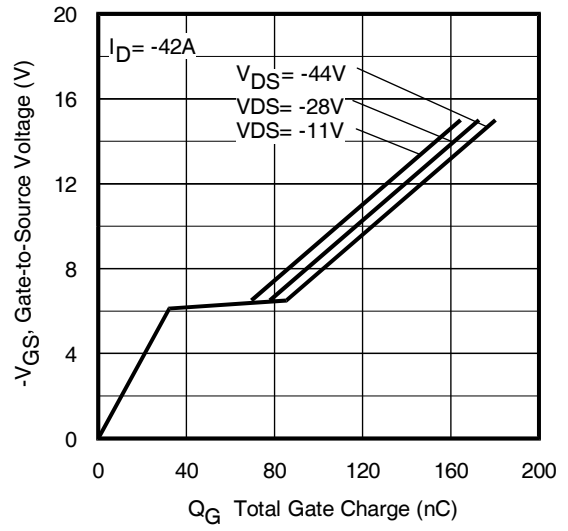
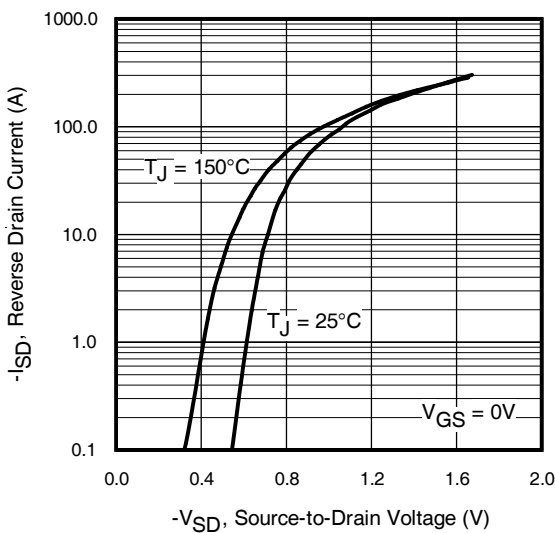
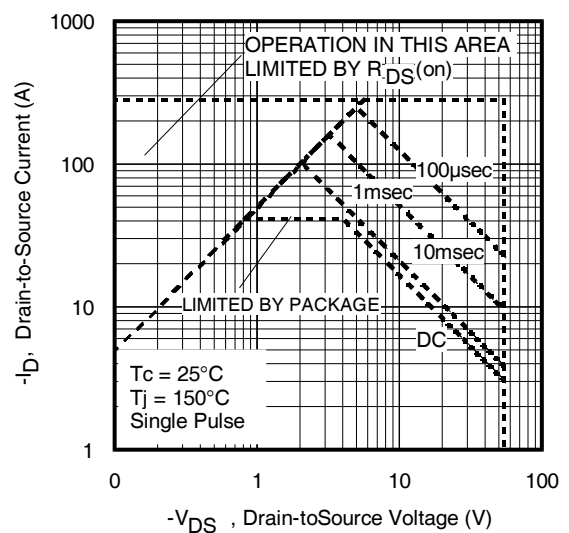
**Diode Characteristics**

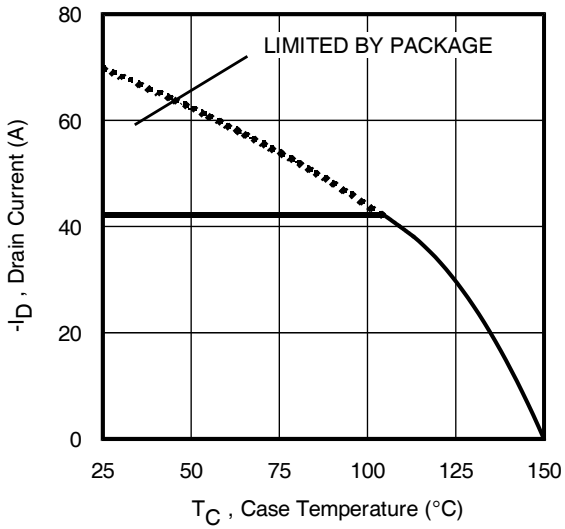
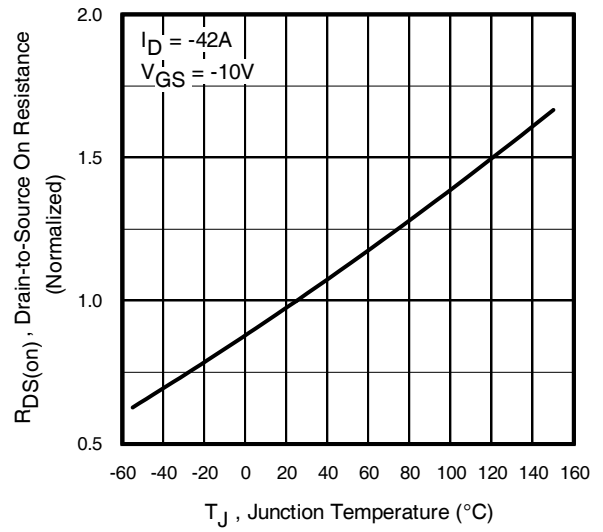
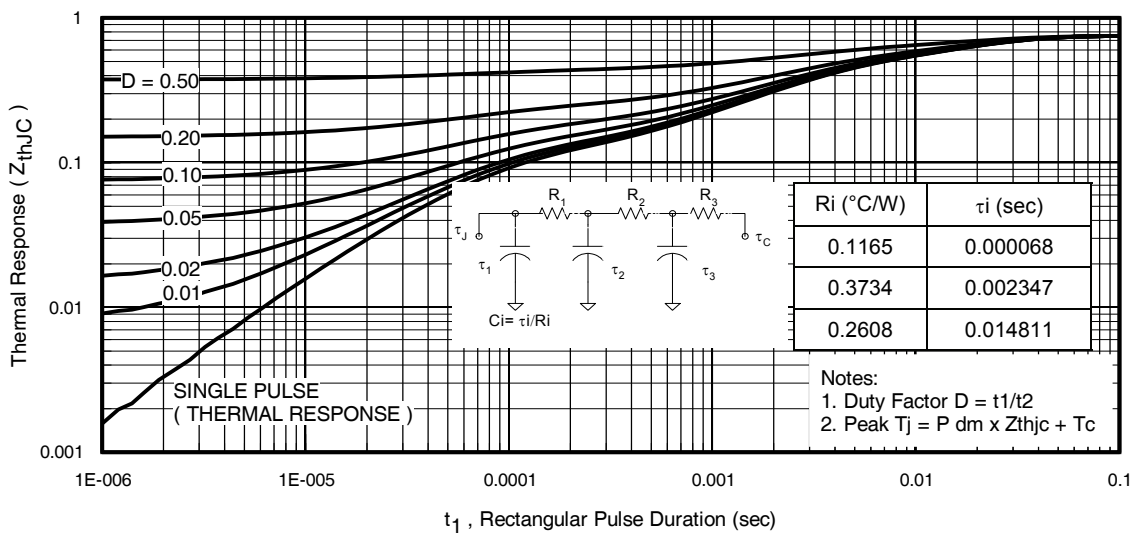
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-42	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-280		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -42A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	61	92	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -42A, V <sub>DD</sub> = -28V
Q <sub>rr</sub>	Reverse Recovery Charge	—	150	220	nC	di/dt = 100A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

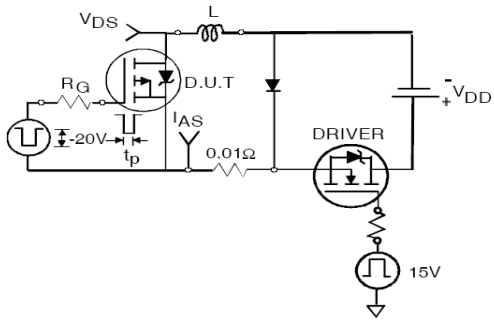
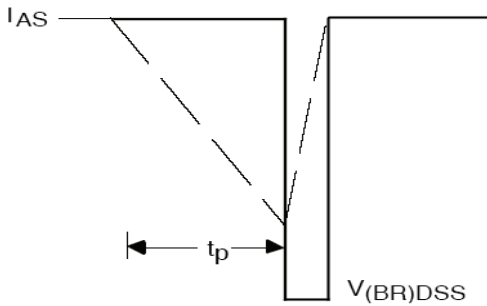
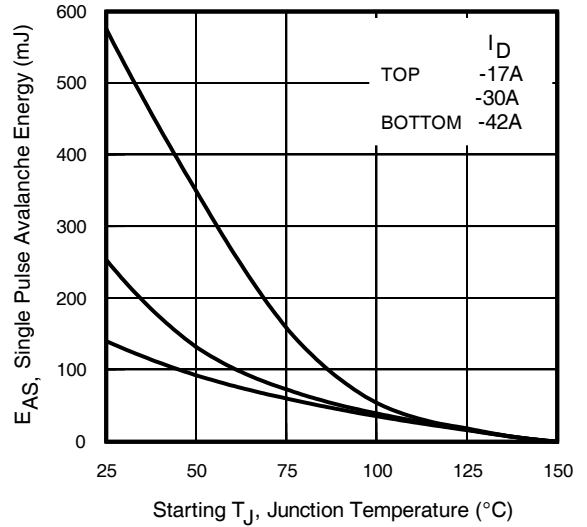
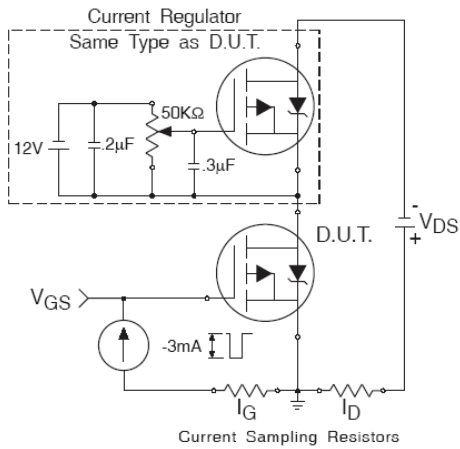
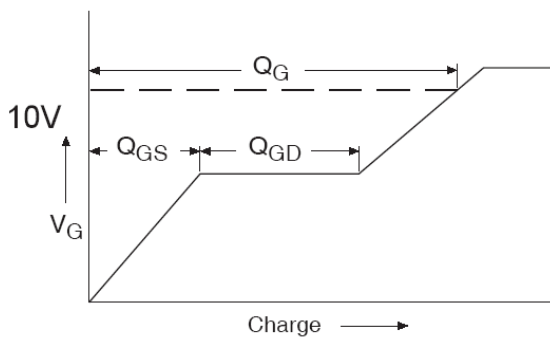
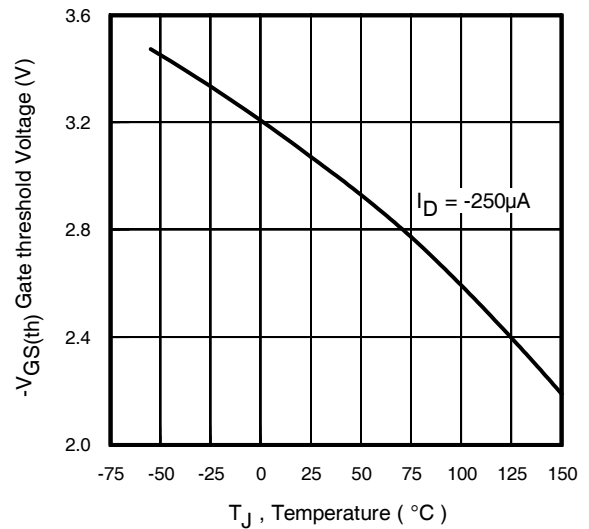
**Notes:**

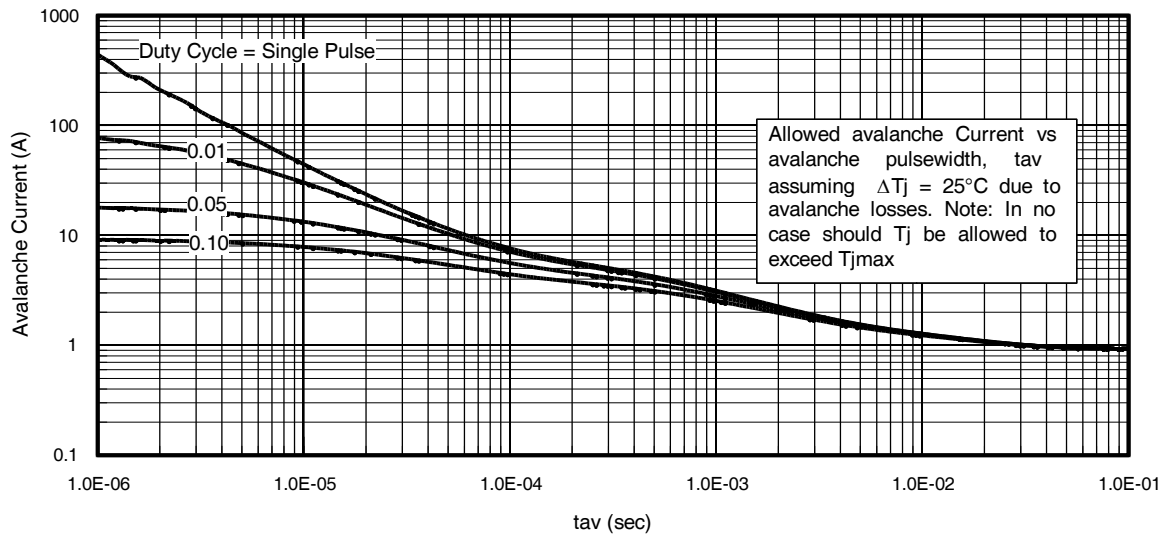
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig.11)
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.16mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = -42A, V<sub>GS</sub> = -10V. Part not recommended for use above this value.
- ③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ④ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑤ Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting T<sub>J</sub> = 25°C, L = 0.08mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 66A, V<sub>GS</sub> = 10V.
- ⑦ This is applied to D<sup>2</sup> Pak, When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C


**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Typical Forward Trans conductance vs. Drain Current


**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area


**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Normalized On-Resistance vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12a. Unclamped Inductive Test Circuit**

**Fig 12b. Unclamped Inductive Waveforms**

**Fig 12c. Maximum Avalanche Energy vs. Drain Current**

**Fig 13a. Gate Charge Test Circuit**

**Fig 13b. Gate Charge Waveform**

**Fig 14. Threshold Voltage vs. Temperature**

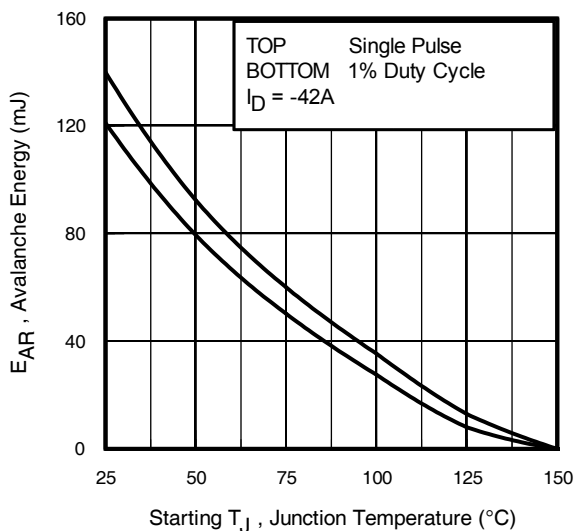

**Fig 15. Avalanche Current vs. Pulse width**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.infineon.com)**

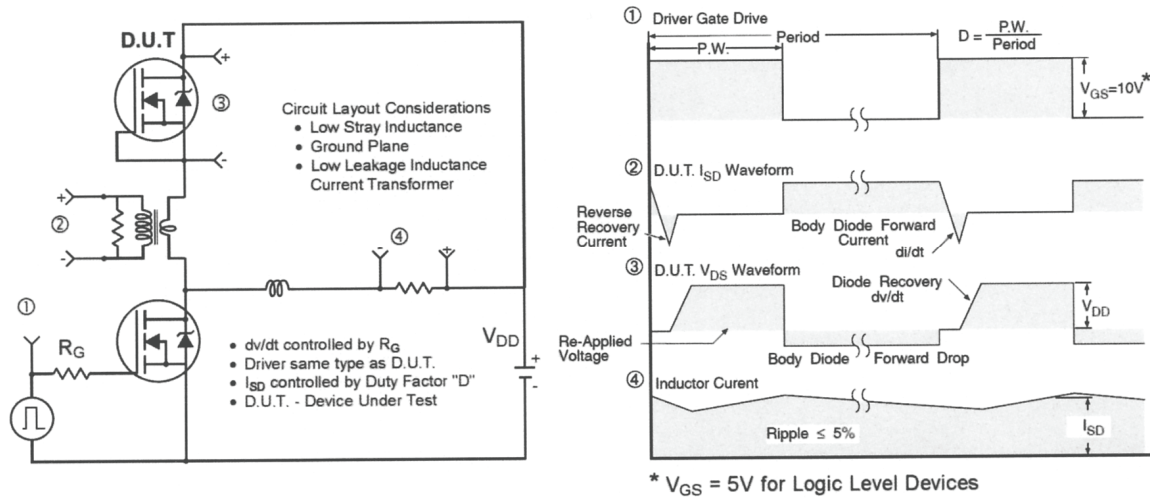
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

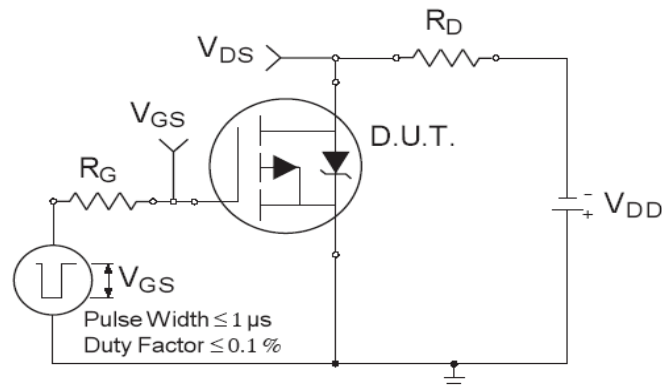
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

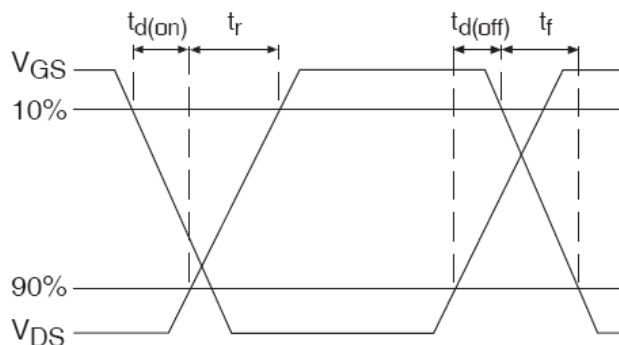

**Fig 16. Maximum Avalanche Energy vs. Temperature**



**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for P-Channel HEXFET® Power MOSFETs



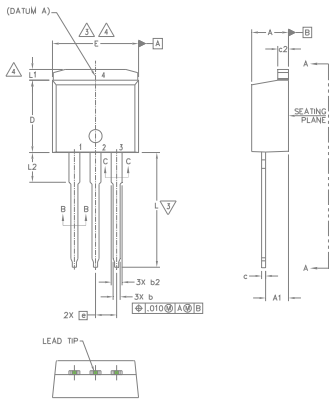
**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms





**TO-262 Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

**LEAD ASSIGNMENTS**
**IGBTs, CoPACK**

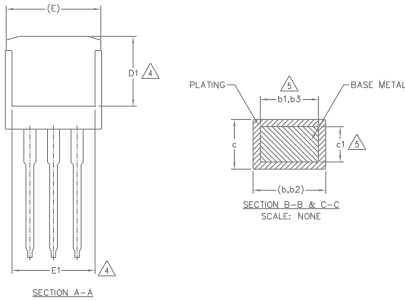
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

**HEXFET**

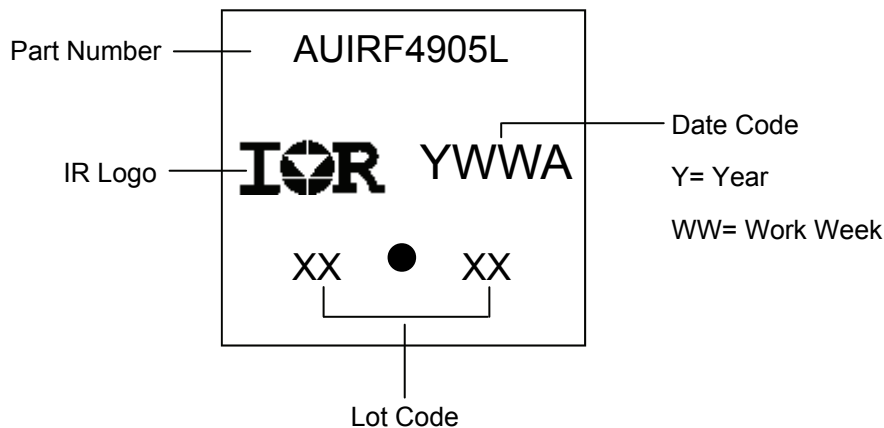
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**DIODES**

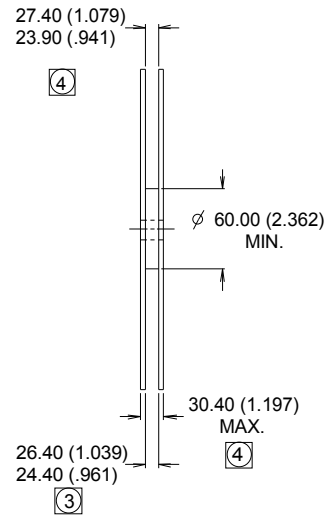
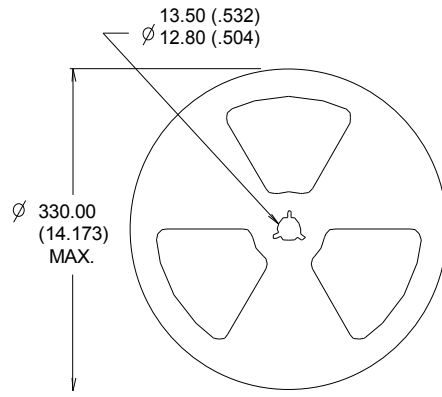
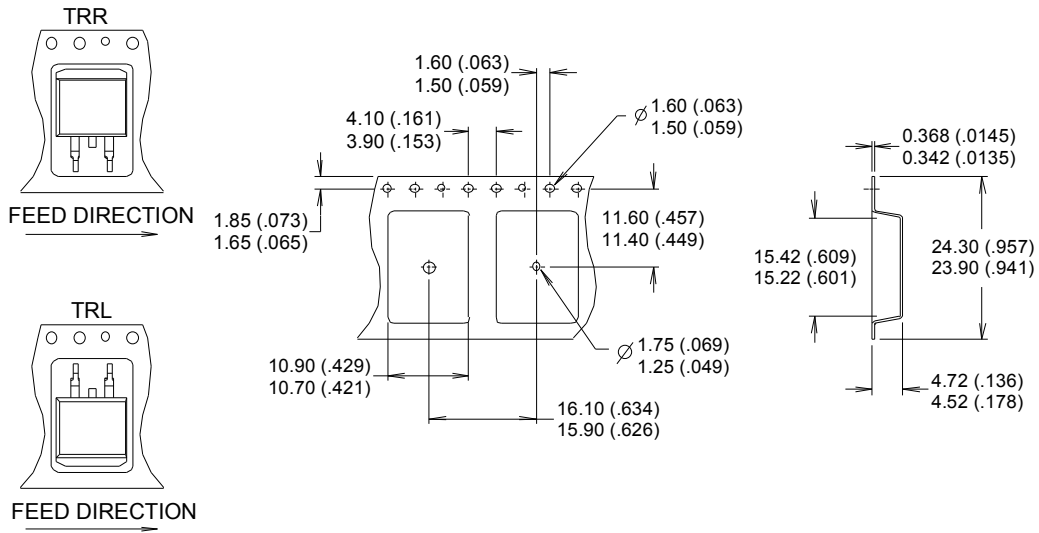
- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

**TO-262 Part Marking Information**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))**


- NOTES :
1. COMFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		TO-262 Pak	MSL1
		D <sup>2</sup> -Pak	
<b>ESD</b>	Machine Model	Class M4 (+/- 425V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H2 (+/- 4000V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
11/13/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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