High current PROFET™

BTS50050-1EGA

Smart High-Side Power Switch
One Channel, 5 mΩ

Datasheet

High current PROFET™
V1.1, 2011-08-16

Automotive

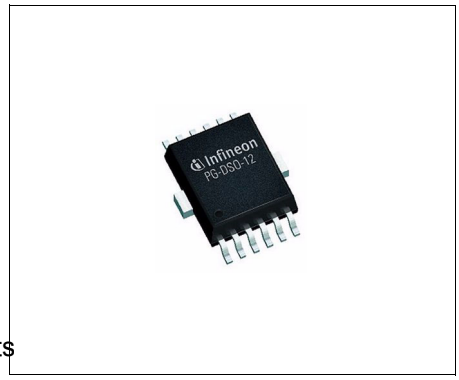
Smart High-Side Power Switch
One Channel, 5 mΩ

BTS50050-1EGA

AEC Qualified

RoHS

1 Overview



PG-DSO-12-16

Features

- Part of scalable product family
- 3.3 and 5V compatible, ground referenced CMOS compatible inputs
- Optimized electromagnetic compatibility (EMC)
- Very low standby current
- Stable behavior at under-voltage
- Secure load turn-off while device ground disconnected
- ReverSave™ - Reverse battery protection without external components
- Inverse load current capability
- Infineon® INTELLIGENT LATCH
- Green Product (RoHS compliant)
- AEC qualified

Extended operating voltage range	$V_{bb(ext)}$	6 .. 28V
Minimum power stage over-voltage protection	$V_{DS(CL)}$	42 V
Typical on-state resistance at T_j = 25°C	$R_{DS(ON)}$	5 mΩ
Maximum on-state resistance at T_j = 150°C	$R_{DS(ON)}$	10 mΩ
Typical nominal load current	$I_{L(nom)}$	16 A
Minimum short circuit shutdown Threshold (SCT)	$I_{L(SC)high}$	100 A
Maximum stand-by current for whole device with load for $T_j \leq 85$°C	$I_{bb(OFF)}$	10 µA

Description

The BTS50050-1EGA is a single channel high-side power switch in PG-DSO-12-16 package providing embedded protective functions including ReverSave™ and Infineon® INTELLIGENT LATCH.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The design is based on Smart power chip on chip technology.

The BTS50050-1EGA has ground referenced CMOS compatible inputs.

ReverSave™ is a protection feature that causes the power transistor to switch on in case of reverse polarity. As a result, the power dissipation is reduced.

Infineon® INTELLIGENT LATCH ensures a latched switch-off and reporting in case of fault condition.

The Infineon® ENHANCED SENSE pin IS provides a sophisticated diagnostic feedback signal including current sense functionality, open load in ON-state (via sense signal) and open load and short to battery in OFF-state. Diagnostic reporting can be enabled and disabled by the DEN-Pin in ON-state and OFF-state. In OFF-state, open load detection can also be disabled by the DEN-Pin to optimize stand-by current.

Type	Package	Marking
BTS50050-1EGA	PG-DSO-12-16	BTS 50050A

Protective Functions

- Short circuit protection with latch
- Thermal shutdown with latch
- Infineon® INTELLIGENT LATCH - reset able latch resulting from protective switch-off
- ReverSave™ - Reverse battery protection by self turn on of power MOSFET
- Inverse load current capability - Inverse operation function
- Under voltage shutdown with restart
- Over voltage protection (including load dump)
- Loss of ground protection
- Loss of V_{bb} protection (with external diode for charged inductive loads)
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Enable function for diagnosis and reporting
- Provides capability for muliplexing of the reporting signal from multiple devices by DEN pin.

In ON-state:

- Provides analog sense signal of load current in normal operation mode
- Provides defined fault current signal in case of overload, over temperature and short circuit to ground
- Open load detection in ON-state by load current sense

In OFF-State:

- Open load and short to battery detection

Applications

- µC compatible high-side power switch with diagnostic feedback for 12 V system grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, such as glow plugs, PTC heaters, or lamps
- Replaces electromechanical relays, fuses and discrete circuits

2 Block Diagram and Terms

2.1 Block Diagram

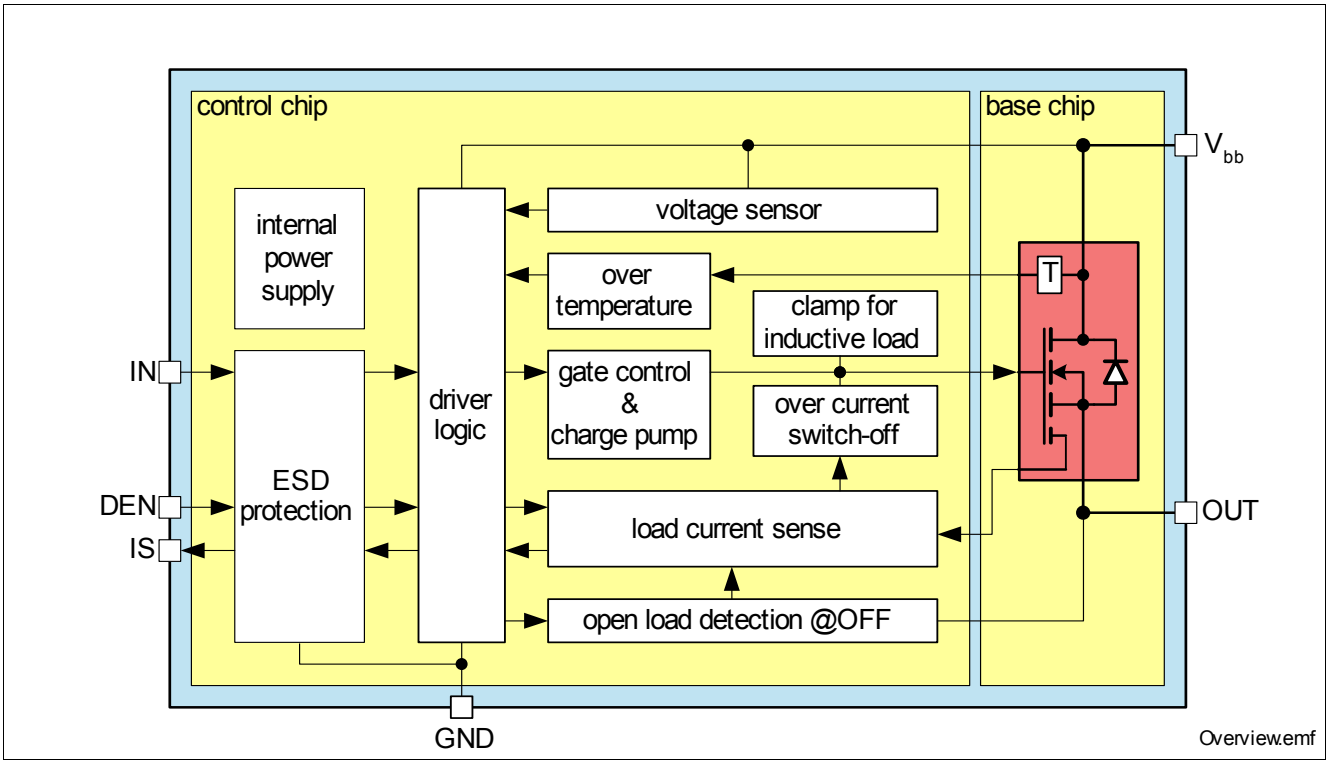


Figure 1 Block Diagram

2.2 Terms

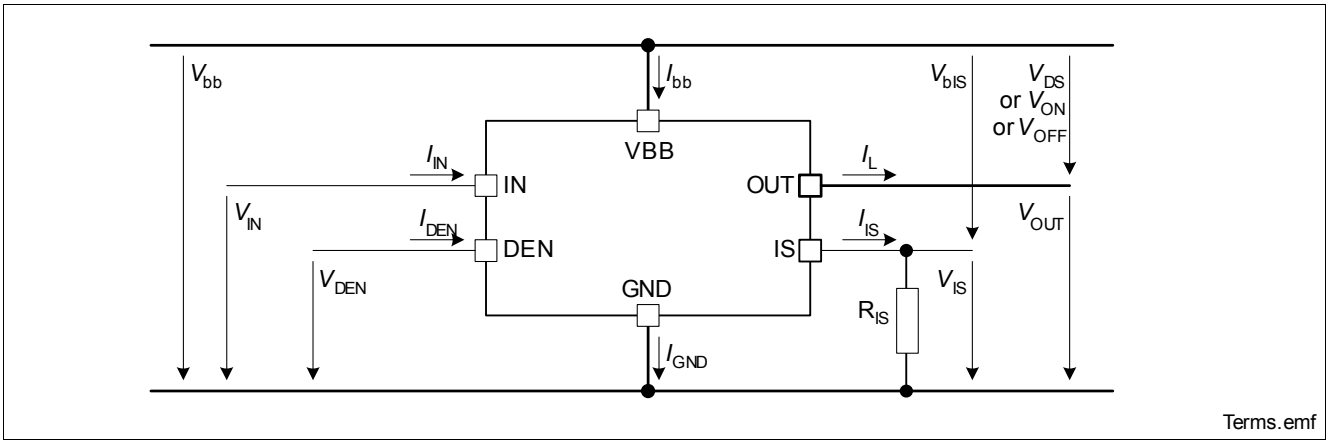


Figure 2 Terms

3 Pin Configuration

3.1 Pin Assignment BTS50050-1EGA

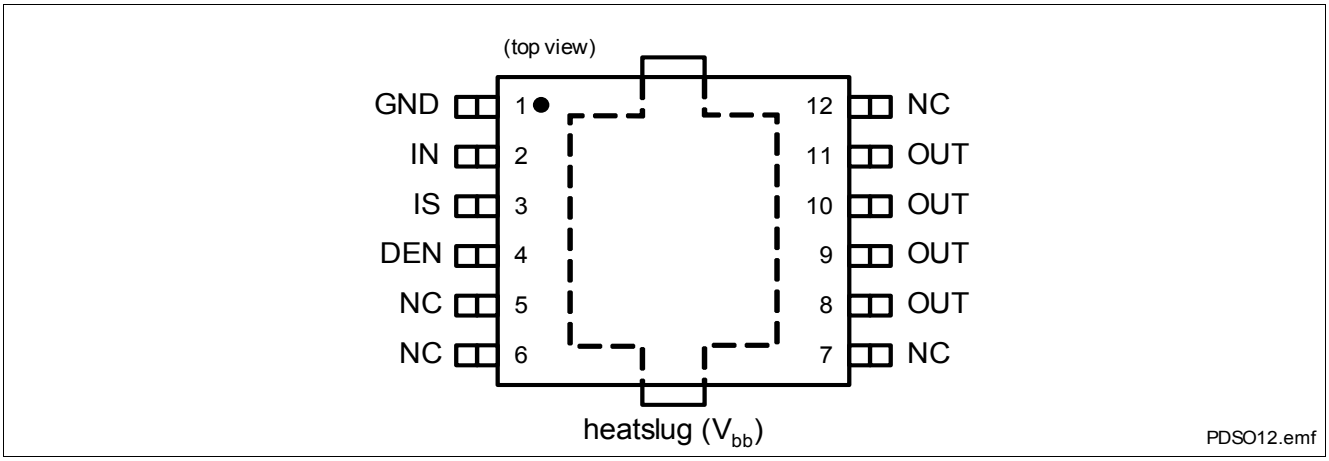


Figure 3 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
1	GND	-	Ground connection for control chip
2	IN	I	Input: activates power switch. Has an internal pull down resistor.
3	IS	O	Sense Output: With diagnosis enabled, provides a sense current proportional to the load current during normal operation. During open load in ON provides no current. Provides a defined fault current in case of overload, over temperature or short circuit during ON or open load or short to battery during OFF (see **Table 1 “Truth Table” on Page 24**)
4	DEN	I	Diagnosis ENable: with high level enables diagnosis reporting and open load / short to battery detection in OFF. Resets a protective, latched switch-off by falling edge acknowledgement. Has an internal pull down resistor.
5, 6, 7, 12	NC	-	Not connected. For recommendation on handling the NC pins, please see **Chapter 8.1**.
8, 9, 10, 11	OUT	O	Output: output to the load; pins 8 to 11 must be externally shorted together[1)]
heatslug	V_{bb}	-	Supply Voltage: positive power supply for logic and output

1) Not shorting all output pins will considerably increase the on-state resistance, reduce the peak current capability, the clamping capability and decrease the current sense accuracy.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Operation outside the parameters listed here may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability

Absolute Maximum Ratings [1)]

Tj = -40 °C to +150 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Supply Voltage						
4.1.1	Supply voltage	V_{bb}	0	42	V	
4.1.2	Reverse polarity voltage	$-V_{bb(rev)}$	0	16	V	T_j = 25 °C [2)]
4.1.3	Supply voltage for short circuit protection (single pulse)	$V_{bat(SC)}$	0	28	V	[3)]
4.1.4	Supply Voltage for Load Dump protection	$V_{bb(LD)}$	-	42	V	R_I = 2 Ω [4)], R_L = 1Ω t_d =400 ms T_j = 25 °C
Input Pins						
4.1.5	Voltage at IN pin	V_{IN}	-0.3	6	V	-
4.1.6	Current through IN pin	I_{IN}	-2	2	mA	[2)]
4.1.7	Voltage at DEN pin	V_{DEN}	-0.3	6	V	-
4.1.8	Current through DEN pin	I_{DEN}	-2	2	mA	[2)]
Output Pins						
4.1.9	Voltage at sense pin	V_{IS}	-0.3	V_{ZIS}	V	-
4.1.10	Current through sense pin IS	I_{IS}	-10 [2)5)]	10	mA	-
Power Stages						
4.1.11	Load current [6)]	$\|I_L\|$	-	$I_{L(SC)}$	A	-
4.1.12	Inductive load switch-off energy (single pulse)	E_{AS}	-	200	mJ	V_{bb}=13.5V [7)], $I_{L(0)}$ = 50A, $T_{j(0)} \leq$ 150 °C
4.1.13	Inductive load switch-off energy (repetitive pulses)	E_{AR}	-	100	mJ	V_{bb}=13.5V [7)8)], $I_{L(0)}$ = 20A, $T_{j(0)} \leq$105 °C
Temperatures						
4.1.14	Junction temperature	T_j	-40	150	°C	-
4.1.15	Dynamic temperature increase while switching	ΔT_j	-	60	K	-
4.1.16	Storage temperature	T_{stg}	-55	150	°C	-
ESD Susceptibility						
4.1.17	ESD susceptibility HBM IN, DEN, IS, V_{bb}, OUT V_{bb} versus OUT	V_{ESD}	 -2 -4	 2 4	kV	according to EIA/JESD 22-A 114B

1) Not subject to production test, specified by design.

2) $t \leq$ 2 min

3) Short circuit is defined as a combination of remaining resistances and inductances. See **Figure 15**.
4) $V_{bb(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839. R_i is the internal resistance of the Load Dump pulse generator
5) Valid at disabled diagnosis.
6) Over current threshold switch-off is a protection feature. Protection features are not designed for continuous repetitive operation.
7) See also **Chapter 5.5** .
8) Resuls from simulation of temperature swing. Not subject to production test, specified by design.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Supply Voltage						
4.2.1	Supply voltage range for normal operation	$V_{bb(nor)}$	9	16	V	-
4.2.2	Extended supply voltage range for operation	$V_{bb(ext)}$	6	28[1)]	V	[2)]
4.2.3	Operating current V_{IN} = 0V, V_{DS} > $V_{DS(OL)}$ V_{IN} = 5V	I_{GND}	 - -	 4 24	mA	V_{DEN} = 5V, V_{IS} < 5.5V, V_{bb} = $V_{bb(nor)}$
4.2.4	Load current range for sense functionality [1)]	$I_{L(IS)}$	1.5	59	A	I_{IS} - $I_{IS(LH)}$ > 30 µA, $I_{IS(lim)}$ > I_{IS}, V_{bb} = $V_{bb(nor)}$, V_{IN} = V_{DEN} = 5 V, V_{bIS} > 5 V
4.2.5	Junction temperature	T_j	-40	150	°C	-

1) Not subject to production test, specified by design
2) In extended supply voltage range, the device is functional but electrical parameters are not specified.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to case [1]	R_{thjc}	-	-	1.3	K/W	[2]
4.3.2	Control chip to case [1]	$R_{thj(cc)c}$	-	40	-	K/W	[3]
4.3.3	Junction to ambient [1] device on PCB[4]	R_{thja}	-	27	-	K/W	–

1) Not subject to production test, specified by design

2) Specified R_{thjc} value is simulated at natural convection on a cold plate setup. T_a = 25 °C.

3) Specified $R_{thj(cc)c}$ value is simulated at natural convection on a cold plate setup. T_a = 25 °C, I_L = 0A.

4) Specified R_{thja} value and **Figure 4** are according Jedec JESD51_7 at natural convection on FR4 2s2p board. The BTS50050-1EGA was measured on a 76.2 x 114.3 x 1.6 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu) applying power losses of 1.4W at the channel. According to JESD51-5 a thermal via array under the exposed pad contacted the first inner copper layer. T_a = 25 °C.

Figure 4 shows the typical transient thermal impedance of BTS50050-1EGA.

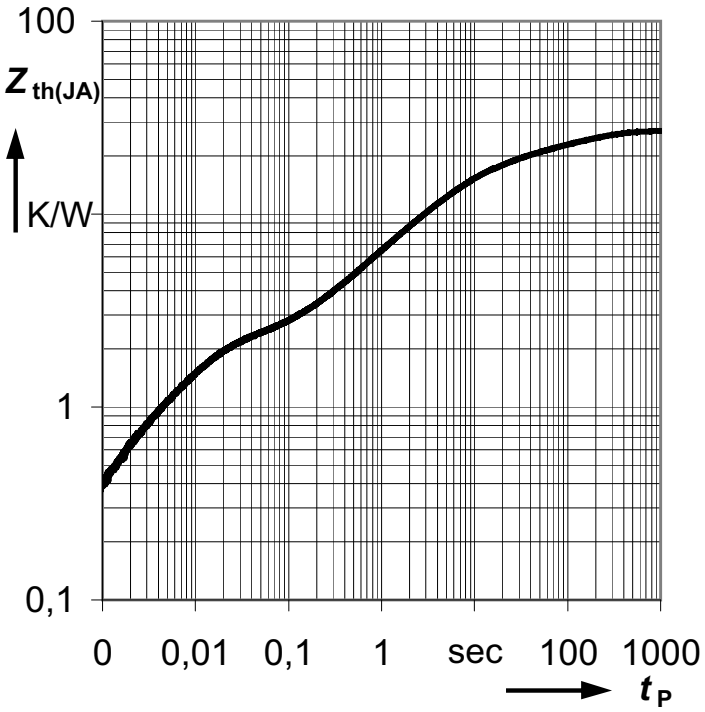


Figure 4 Transient Thermal Impedance $Z_{th(JA)}=f(t_p)$ [4]

4.4 Package

Pos.	Parameter	Value	Test Conditions
4.4.1	Jedec humidity category acc. J-STD-020-D	MSL3	-
4.4.2	Jedec classification temperature acc. J-STD-020-D	260°C	-

5 Power Stages

The power stage is built by a N-channel vertical power MOSFET (DMOS) with charge pump.

5.1 Input Circuit

Figure 5 shows the input circuit of the BTS50050-1EGA. The input resistor to ground ensures that the input signal is low in case of open input pin. The zener diode protects the input circuit against ESD pulses.

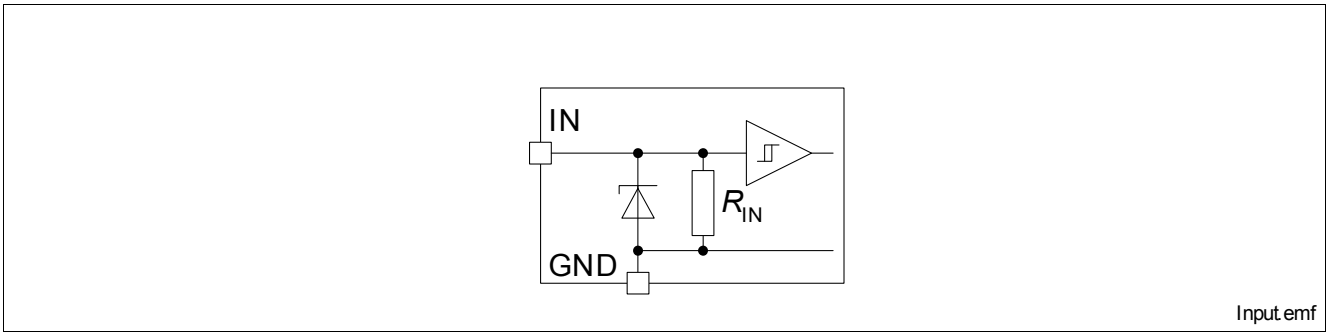


Figure 5 Input Circuit

A high signal at the input pin causes the DMOS to switch on.

5.2 Output On-State Resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage V_{bb} and the junction temperature T_j. **Figure 6** shows these dependencies for the typical on-state resistance. The on-state resistance in reverse polarity mode is described in **Chapter 6.5**.

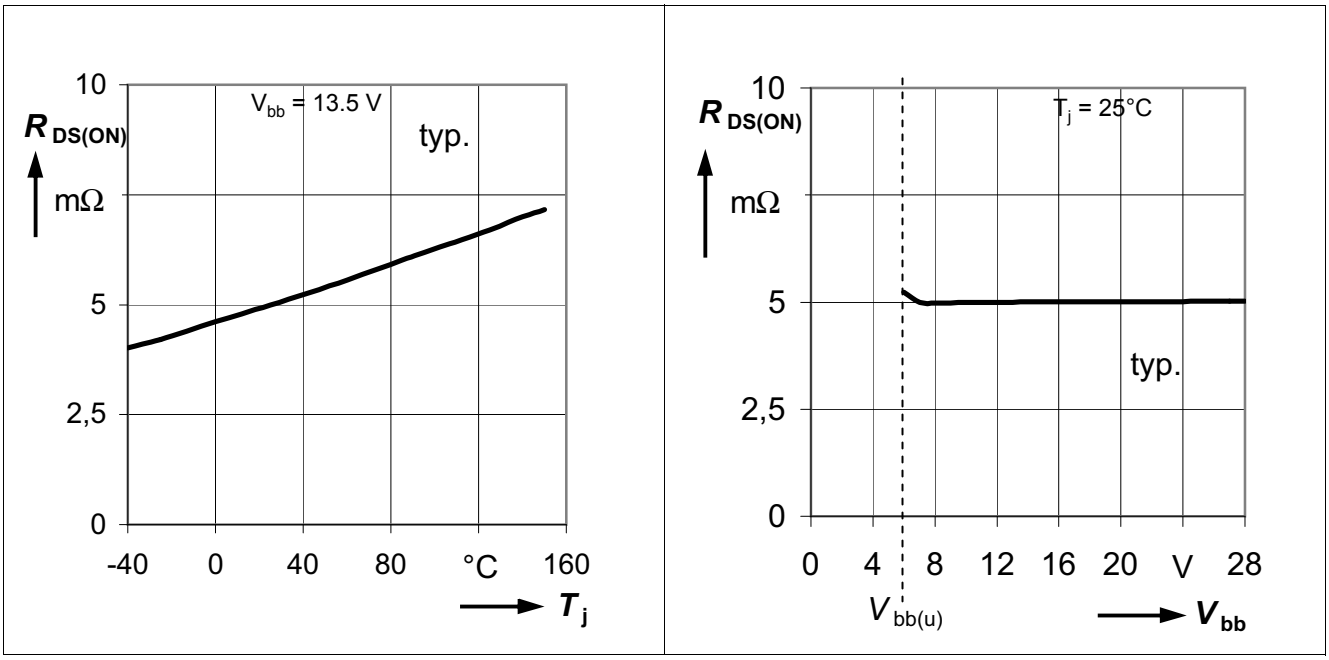


Figure 6 Typical On-State Resistance

5.3 Output Timing

The power stage is designed for high side configuration (**Figure 9**).

The power stage has a defined switching behavior. Defined slew rates as well as edge shaping support PWM'ing of the load while achieving lowest EMC emission at minimum switching losses.

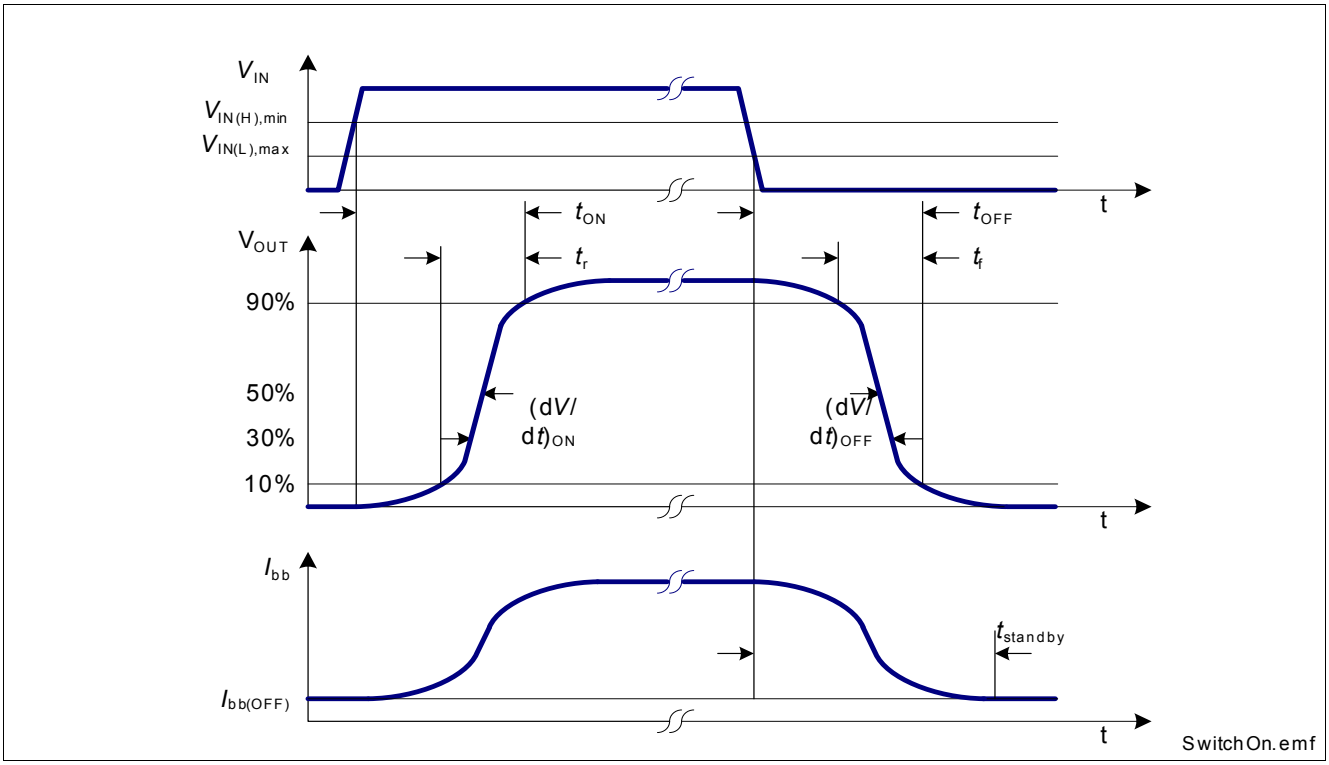


Figure 7 Switching a Load (resistive)

5.4 Switching losses for resistive loads

Switching the device on and off may cause switching losses E_{ON} and E_{OFF}. In case of a resistive load, the switching losses depend on the supply voltage V_{bb} as well as on the load current I_L and the junction temperature T_j. **Figure 8** shows this dependencies of the switching losses.

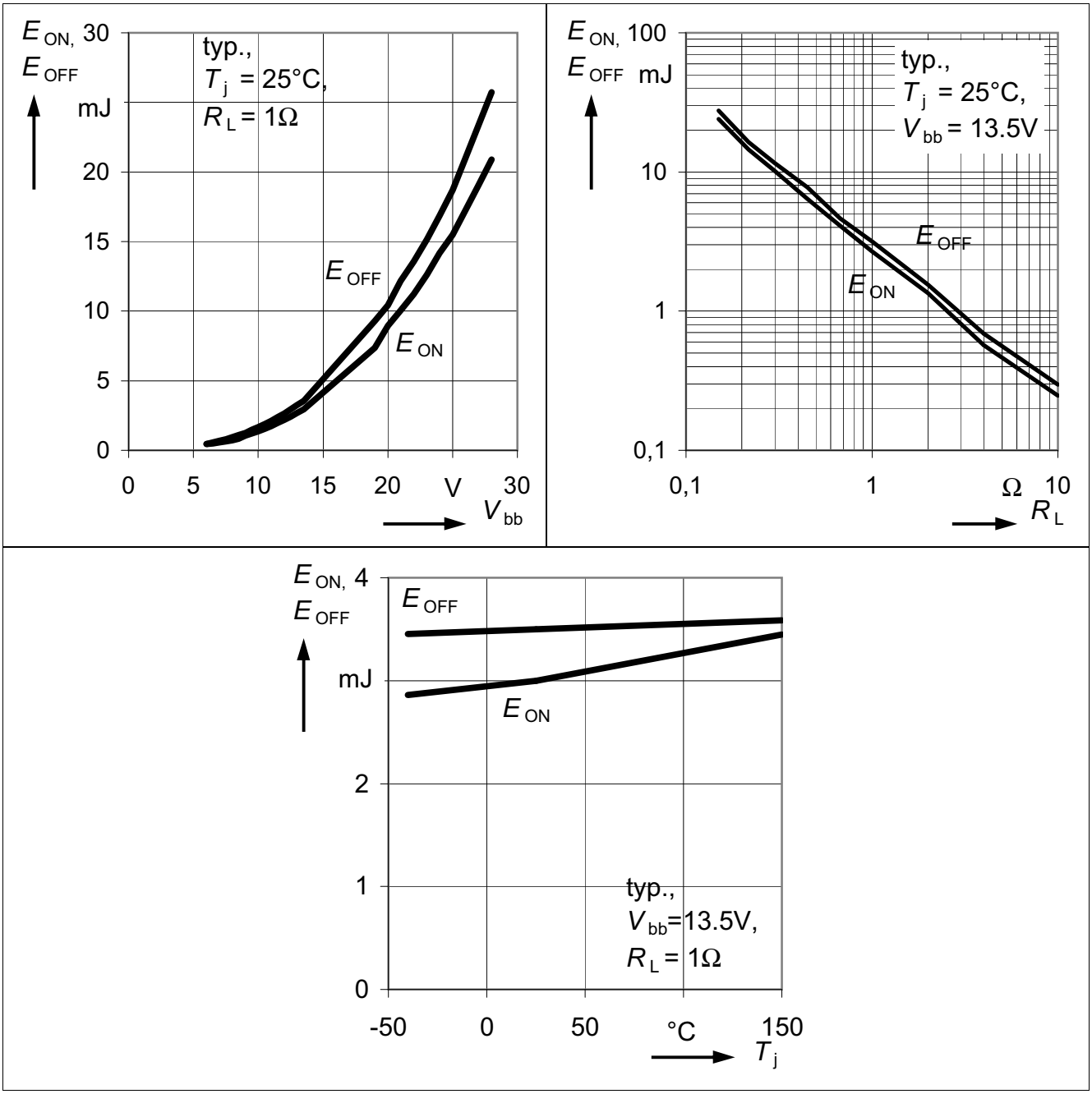


Figure 8 Typical switching losses E_{ON} and E_{OFF}

5.5 Output Inductive Clamp

When switching off inductive loads, the output voltage V_{OUT} drops below ground potential due to the inductive properties of the load ($-di_L/dt = -v_L/L$; $-V_{OUT} \cong -V_L$).

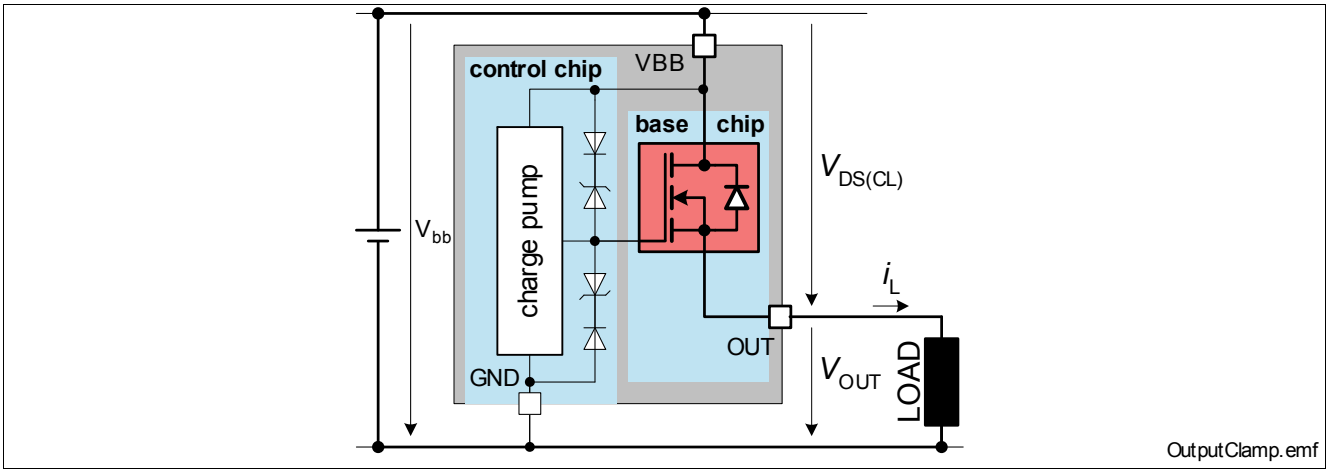


Figure 9 Output Clamp

To prevent destruction of the device, there is a voltage clamp mechanism implemented that keeps the voltage drop across the device at a certain level. At nominal battery voltage the output is clamped to $V_{OUT(CL)}$. At over voltages the output is clamped to $V_{DS(CL)}$. See **Figure 9** and **Figure 10** for details. The maximum allowed load inductance is limited.

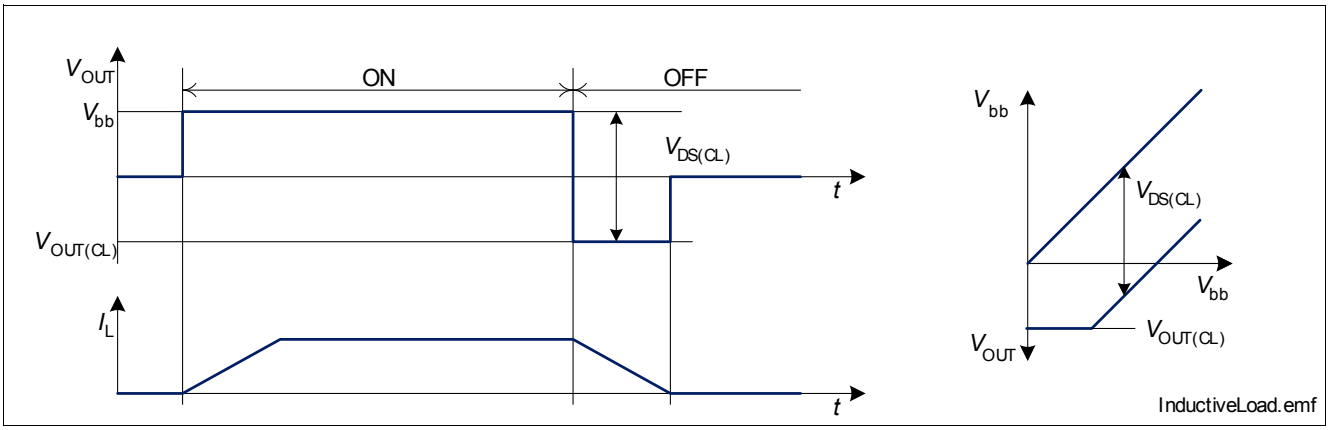


Figure 10 Switching an Inductance

Maximum Load Inductance

While de-energizing inductive loads, energy has to be dissipated in the BTS50050-1EGA. This energy can be calculated by the following equation:

$$E = (V_{bb} + |V_{OUT(CL)}|) \cdot \left[\frac{-|V_{OUT(CL)}|}{R_L} \cdot \ln\left(1 + \frac{R_L \cdot I_L}{|V_{OUT(CL)}|}\right) + I_L \right] \cdot \frac{L}{R_L}$$

In the event of de-energizing very low ohmic inductances ($R_L \approx 0$) the following, simplified equation can be used:

$$E = \frac{1}{2} L I_L^{\,2} \cdot \frac{|V_{DS(CL)}|}{|V_{DS(CL)}| - V_{bb}}$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 11** for the maximum allowed energy dissipation.

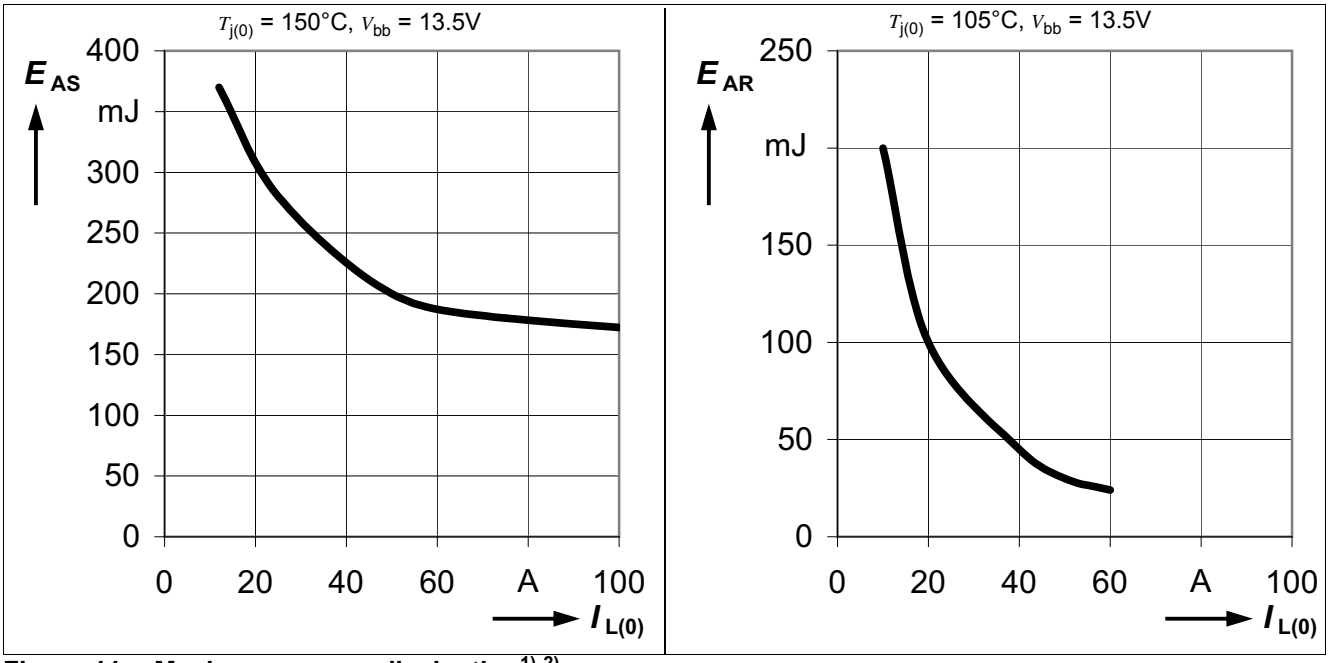


Figure 11 Maximum energy dissipation[1) 2)]

Note: Clamping overrides all protection functionalities. In order to avoid device destruction resulting from inductive switch-off or over voltage the device has to be operated within the maximum ratings.

5.6 Inverse Operation Capability

The BTS50050-1EGA can be operated in inverse load current condition ($+V_{OUT} > +V_{bb}$). The device can not block the current flow during inverse mode.

In ON condition a voltage drop across the activated channel of $-V_{ON(inv)}=R_{ON(inv)}*(-I_L)$ can be observed.

In OFF condition a voltage drop across the intrinsic body diode of $-V_{OFF(inv)}=f(-I_L)$ can be observed.

As long as the inverse current does not exceed $|-I_L| \leq |-I_{L(inv)}|$ the logic will operate and report according **Table 1** and the BTS50050-1EGA will be able to remain in ON mode.

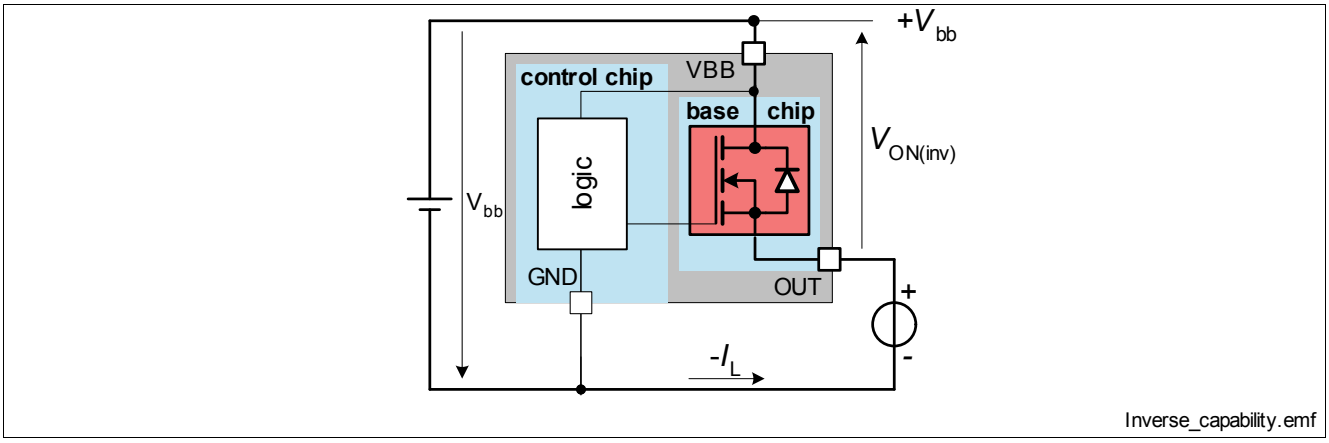


Figure 12 Inverse current capability

1) Not subject to production test, specified by design.

2) Resuls for E_{AR} from simulation of temperature swing.

Note: Activation of any protection mechanism will not block the current flow. Over temperature detection and current sense is not functional during inverse mode.

5.7 Undervoltage shutdown and restart

The BTS50050-1EGA is supplied by V_{bb}. The internal logic permanently monitors the supply voltage V_{bb}. In the event that the supply voltage drops below the under voltage shutdown threshold $V_{bb(u)}$, the BTS50050-1EGA will switch off. If the supply voltage reaches nominal operating voltage range $V_{bb(ext)}$, the BTS50050-1EGA will switch on after a delay $t_{delay(UV)}$, assuming V_{IN}=High. Protective latch is reset by undervoltage shutdown.

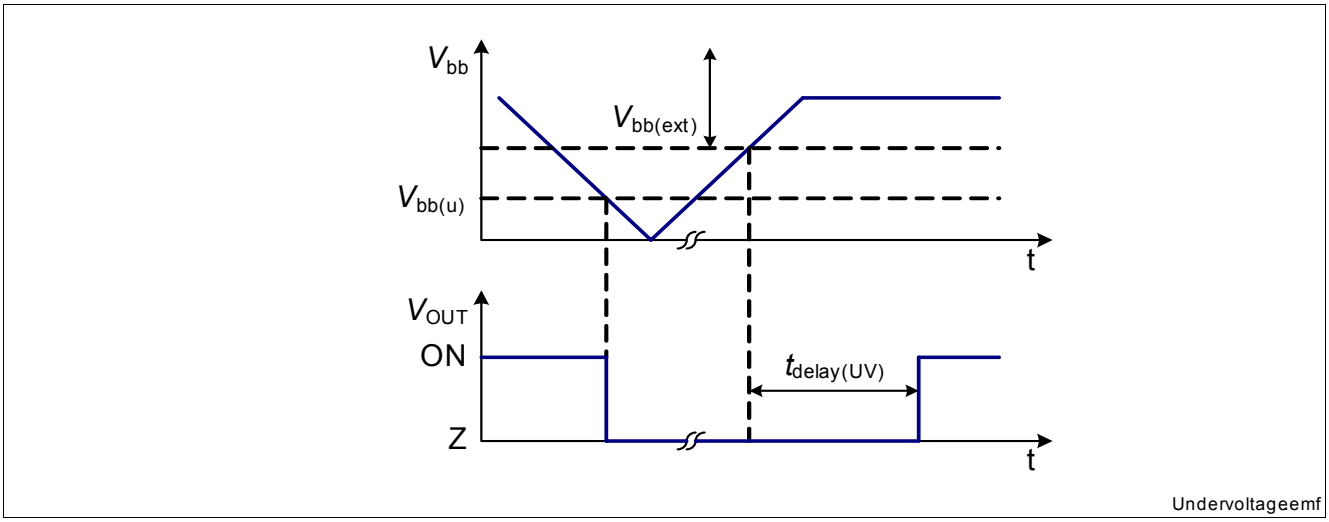


Figure 13 Undervoltage shutdown and restart

5.8 Electrical Characteristics: Power Stages

Note: Characteristics show the deviation of parameters at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
General							
5.8.1	Stand-by current T_j = -40 °C, T_j = 25 °C $T_j \leq$ 85 °C [1] T_j = 150 °C	$I_{bb(OFF)}$	 - - -	 6 6 16	 10 10 50	µA	[2], $\|V_{IN}\|=\|V_{DEN}\| \leq 0.3V$ [3], $V_{OUT}=V_{IS}=0V$, $t > t_{standby}$, no fault condition
5.8.2	Stand-by time [1] [2]	$t_{standby}$	-	0.5	1	ms	$\|V_{IN}\|=\|V_{DEN}\| \leq 0.3V$, $V_{OUT}=V_{IS}=0V$
5.8.3	Undervoltage shutdown[1]	$V_{bb(u)}$	-	5.7	6	V	-
5.8.4	Undervoltage recovery time[1]	$t_{delay(UV)}$	-	10	-	ms	-
Input characteristics							
5.8.5	L-input level	$V_{IN(L)}$	-0.3	-	1.0	V	-
5.8.6	H-input level	$V_{IN(H)}$	2.0	-	5.5	V	-
5.8.7	input hysteresis	$V_{IN(hys)}$	-	100	-	mV	[1]
5.8.8	input pull down resistor	R_{IN}	50	100	200	kΩ	-
Output characteristics							
5.8.9	On-state resistance T_j=25°C T_j=150°C V_{bb}=6V, T_j=25°C V_{bb}=6V, T_j=150°C	$R_{DS(ON)}$	 - - - -	 5 7 8 10	 - 10 - 20	mΩ	V_{IN}=5V, I_L=20A
5.8.10	Nominal load current [1] [4]	$I_{L(nom)}$	-	16	-	A	T_A = 85 °C $T_j \leq$ 150 °C
5.8.11	Output leakage current	$I_{L(OFF)}$	-	3	30	µA	$V_{IN}=V_{DEN}$=0V, V_{OUT}=0V
5.8.12	Output clamp during switch-off	$-V_{OUT(CL)}$	16	18	20	V	$V_{OUT} \geq V_{bb} - V_{DS(CL)}$ [5], I_L = 40 mA
			16	20	25	V	$V_{OUT} \geq V_{bb} - V_{DS(CL)}$ [5], I_L = 20 A [1]
5.8.13	Output clamp during over voltage	$V_{DS(CL)}$	42	50	-	V	$V_{DS} \leq V_{bb} - V_{OUT(CL)}$ [5], I_L = 40 mA
			42	51	-	V	$V_{DS} \leq V_{bb} - V_{OUT(CL)}$ [5], I_L = 20 A [1]
5.8.14	Switch-On energy 5↗95% V_{OUT}	E_{ON}	-	3	5	mJ	V_{bb} = 13.5 V, R_L = 1 Ω
5.8.15	Switch-Off energy 95↘5% V_{OUT}	E_{OFF}	-	3.5	5	mJ	
5.8.16	Inverse operation on-state resistance T_j=25°C T_j=150°C	$R_{ON(inv)}$	 - -	 5 7	 - 10	mΩ	V_{IN} = 5 V, I_L = -20 A, no protective switch-off

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.8.17	Inverse operation output voltage drop T_j=25°C T_j=150°C	$-V_{OFF(inv)}$	 - -	 700 400	 900 800	mV	V_{IN}=0V, I_L = -10 A
5.8.18	Inverse current capability[1)]	$-I_{L(inv)}$	20	-	-	A	-
Timings							
5.8.19	Turn-on time to 90%V_{OUT}	t_{ON}	-	200	350	µs	V_{bb} = 13.5 V R_L = 1Ω
5.8.20	Turn-off time to 10%V_{OUT}	t_{OFF}	-	200	350	µs	V_{bb} = 13.5 V R_L = 1 Ω
5.8.21	Slew rate On 30↗50% V_{OUT}	$(dV/dt)_{ON}$	0.1	0.15	0.21	V/µs	V_{bb} = 13.5 V R_L = 1 Ω
5.8.22	Slew rate Off 50↘30% V_{OUT}	$-(dV/dt)_{OFF}$	0.1	0.15	0.21	V/µs	V_{bb} = 13.5 V R_L = 1 Ω

1) Not subject to production test, specified by design
2) In case of protective switch-off STANDBY is only reached if the fault was acknowledged while IN=LOW by DEN=HIGH↘LOW and $t_{standby}$ expired. See also **Chapter 6.4** for details.
3) Tested at V_{IN}=V_{DEN}=0V only
4) according JESD51_7, FR4 2s2p board, 76.2 x 114.3 x 1.6 mm, 2x70µm Cu, 2x35µm Cu.
5) See **Figure 10**.

6 Protection Functions

The BTS50050-1EGA provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

6.1 Short Circuit Protection

The internal logic permanently monitors the load current I_L. In the event the load current exceeds the short circuit shutdown threshold ($I_L > I_{L(SC)}$), the device will switch off immediately. Any protective switch off latches the output. Please refer to **Figure 14** for details. The protective switch off remains latched until the fault is acknowledged and reset by a falling edge at the DEN pin. See also **Chapter 6.4**.

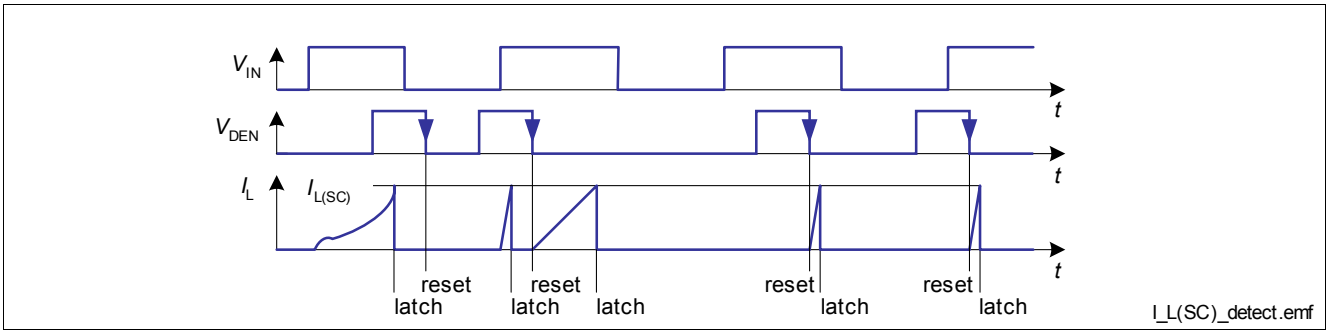


Figure 14 Shutdown by short circuit current detection

Before switching on, the device is measuring the battery voltage $V_{bb(0)}$. In case $V_{bb(0)}$ is above $V_{bb(SCT)}$, the short circuit current threshold $I_{L(SC)high}$ is reduced to a lower level $I_{L(SC)low}$.

*Note: In case of a short circuit between OUT and ground, an impedance between V_{bat} and V_{bb} pin of the device (see **Figure 15**) may cause the device’s supply voltage to drop below $V_{bb(u)}$ before short circuit shutdown threshold is reached. In that case, the device will detect an undervoltage condition and behave as described in **Chapter 5.7**.*

6.2 Short Circuit Impedance

The capability to handle single short circuit events depends on the battery voltage as well as on the primary and secondary short impedance. **Figure 15** outlines allowable combinations for a single short circuit event of maximum, secondary inductance for given secondary resistance.

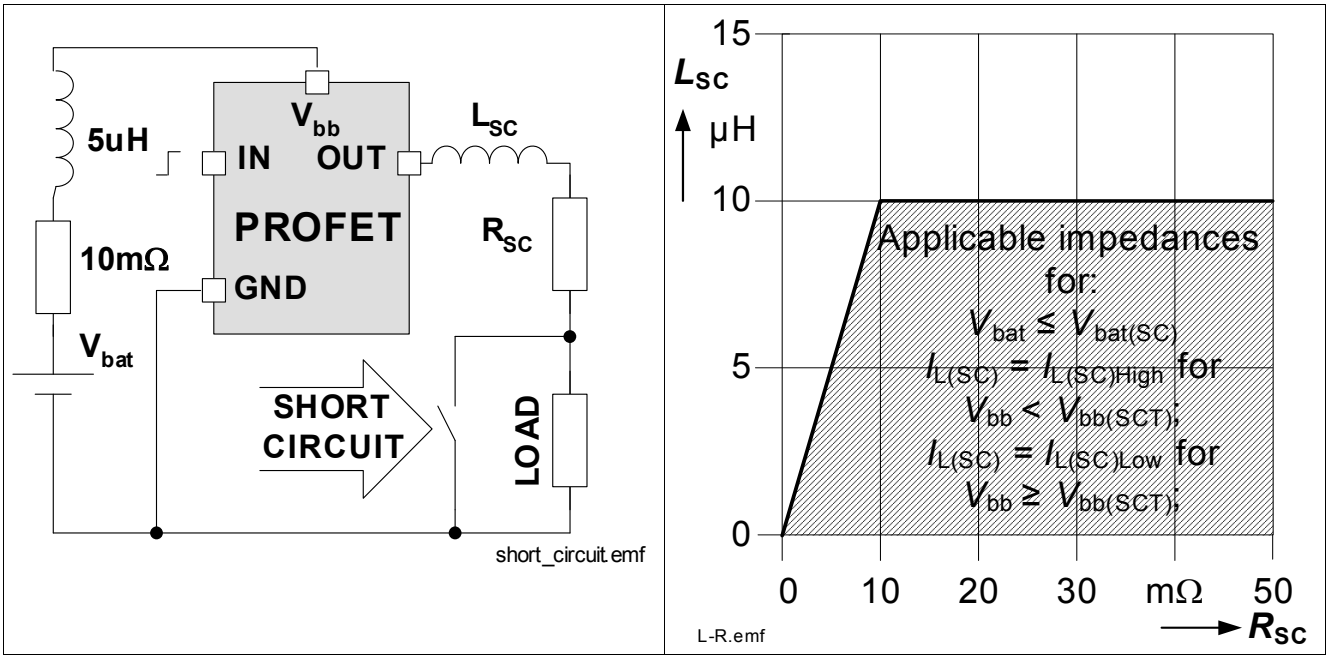


Figure 15 Short circuit

6.3 Over Temperature Protection

The internal logic permanently monitors the junction temperature of the output stage. In the event of an over temperature ($T_j > T_{jt}$) the output will switch off immediately. Please refer to **Figure 16** for details.The protective switch off remains latched until the fault is acknowledged and reset by a falling edge at the DEN pin. See also **Chapter 6.4**.

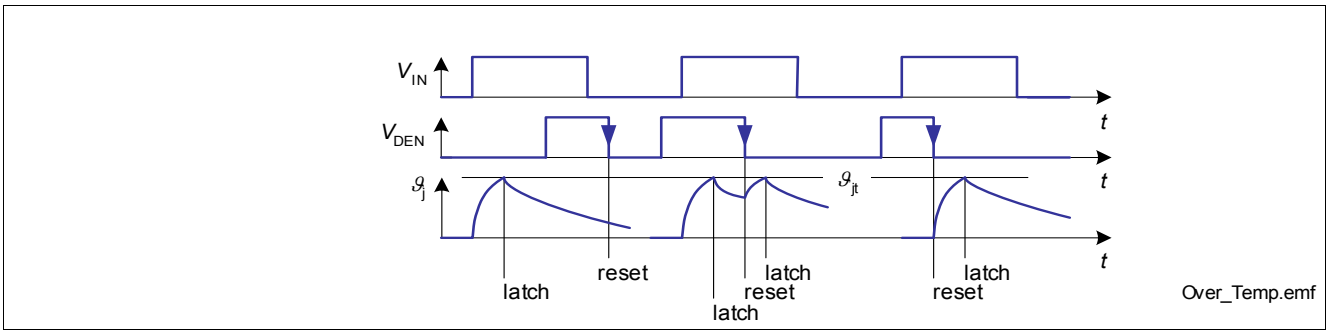
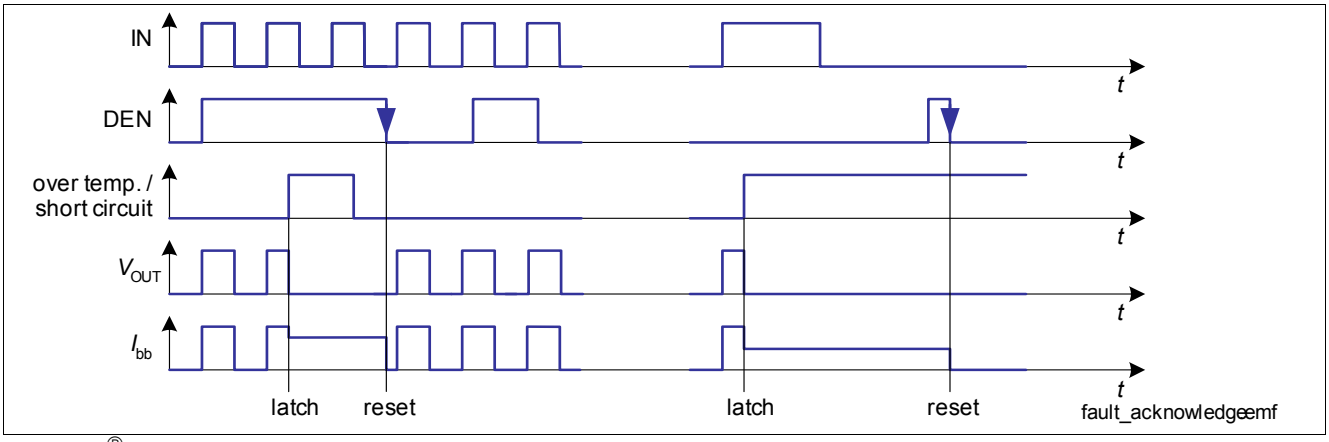


Figure 16 Over temperature detection

6.4 Infineon® INTELLIGENT LATCH - fault acknowledge and latch reset

The BTS50050-1EGA provides Infineon® INTELLIGENT LATCH to avoid permanent resetting of a protective, latched switch off in PWM applications. To reset a latched protective switch off the fault has to be acknowledged by a falling edge at the DEN pin. For a reset signal it's recommended to set the DEN signal to HIGH for 20µs before setting DEN to LOW for 20µs.

Please refer to **Figure** for details.



Infineon® INTELLIGENT LATCH - fault acknowledge and latch reset

6.5 Reverse Polarity Protection - ReverSave™

The device can not block a current flow in reverse battery condition. In order to minimize power dissipation, the device offers ReverSave™ functionality. Under reverse polarity condition, the output stage will be switched on, provided a sufficient gate to source voltage is generated $V_{GS} \approx V_{GND\_bb}$. Please refer to **Figure 17** for details.

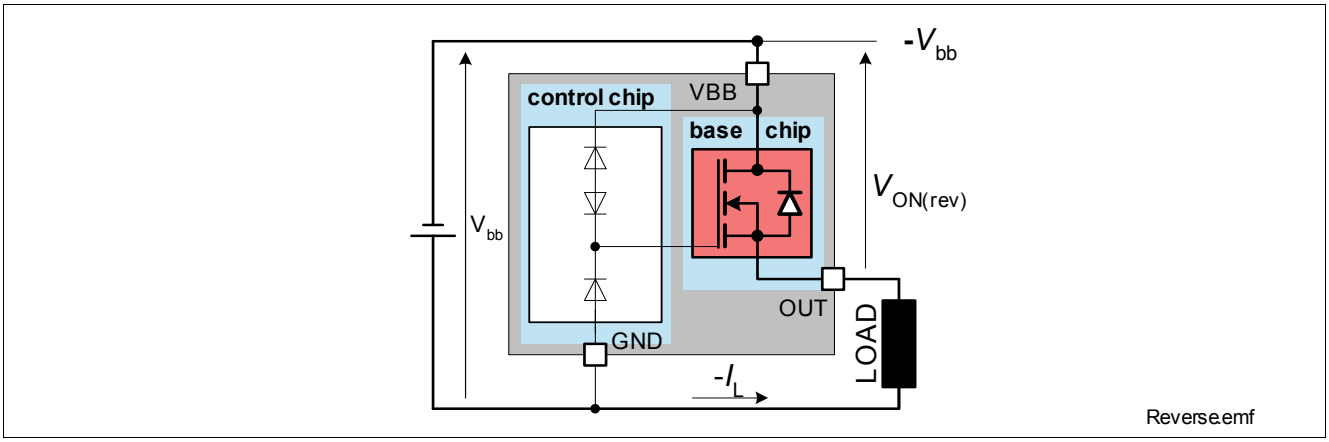


Figure 17 Reverse battery protection

Use the following formula for estimation of overall power dissipation $P_{diss(rev)}$ in reverse polarity mode.

$$P_{diss(rev)} \approx R_{ON(rev)} \cdot I_L^2$$

Note: No protection mechanism is active during reverse polarity. The control chip is not functional. Potentials of logic pins can become negative. Affected pins have to be protected by means of series resistors.

6.6 ESD Protection

All logic pins have ESD protection. Beside the output clamp for the power stage as described in **Chapter 5.5** there is a clamp mechanism implemented for pin IS. See **Figure 18** for details.

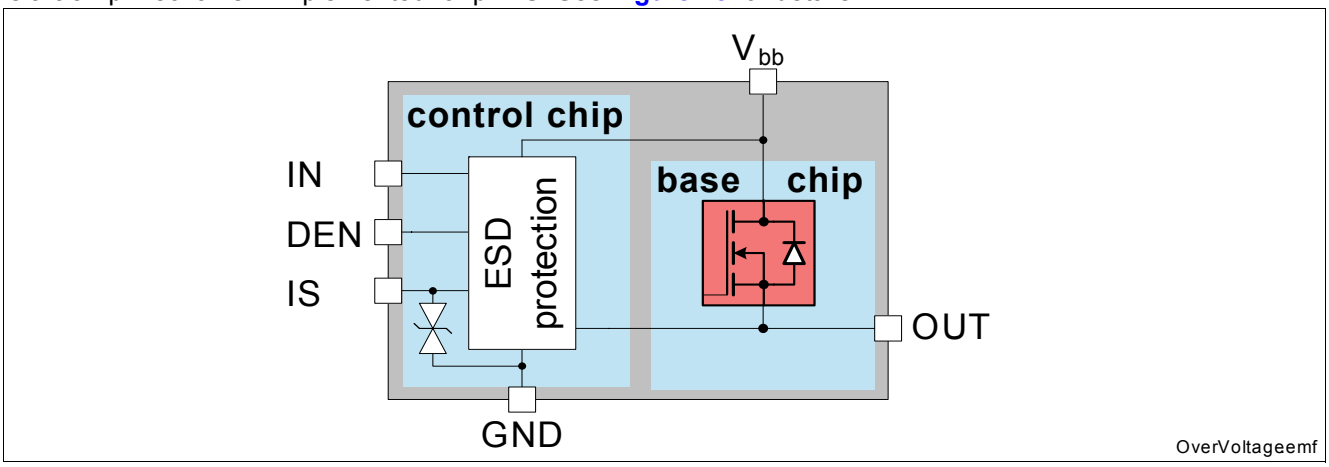


Figure 18 Over-Voltage Protection

6.7 Loss of Ground Protection

In case of complete loss of the device ground connections the BTS50050-1EGA securely changes to or remains in OFF state, if the sense resistor R_{IS} is higher than 500Ω.

6.8 Loss of Load Protection, Loss of V_{bb} Protection

In case of loss of load with charged primary inductances the maximum supply voltage has to be limited. It is recommended to use a Z-diode, a varistor (V_{Za} < 42 V) or V_{bb} clamping power switches with connected loads in parallel.

In case of loss of V_{bb} connection with charged inductive loads, a current path with load current capability has to be provided, to demagnetize the charged inductances. It is recommended to use a diode, a Z-diode or a varistor (V_{Zb} < 16 V, V_{ZL}+V_D < 16 V,).

For higher clamp voltages currents through all pins have to be limited according to the maximum ratings. Please refer to **Figure 19** for details.

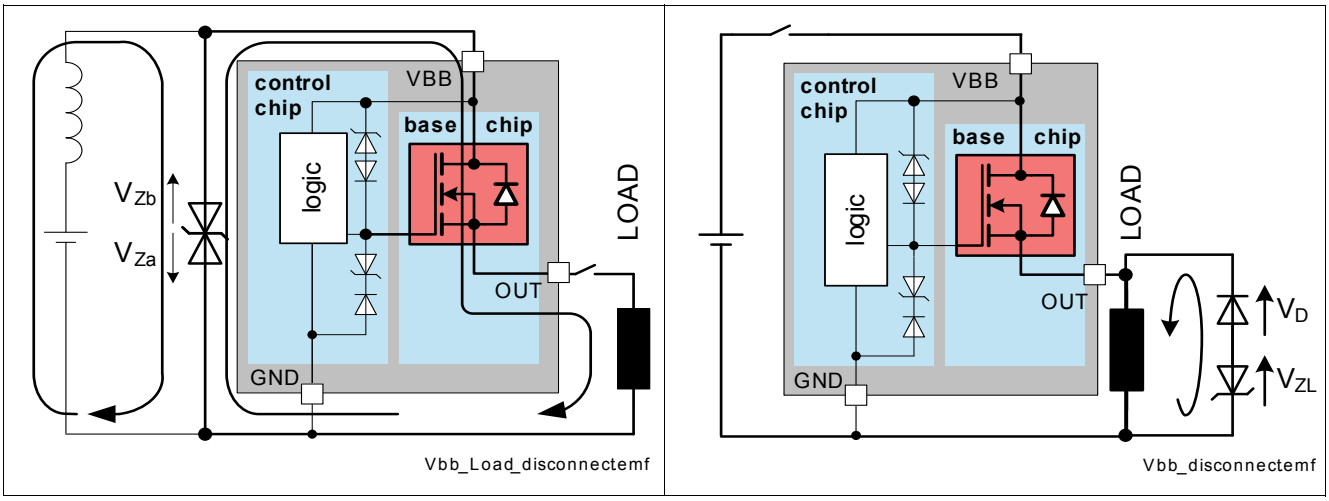


Figure 19 Loss of V_{bb}

In case of complete loss of V_{bb} the BTS50050-1EGA remains in OFF state.

6.9 Electrical Characteristics: Protection Functions

Note: Characteristics show the deviation of parameters at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Over-Load Protection							
6.9.1	Short circuit shutdown threshold (SCT) T_j = -40 °C, T_j = 25 °C T_j = 150 °C	$I_{L(SC)high}$	 100 100	 150 135	 200 170	A	V_{IN} = 5 V $V_{bb(0)} < V_{bb(SCT)}$
6.9.2	Short circuit shutdown threshold at high battery voltages	$I_{L(SC)low}$	42	70	95	A	V_{IN} = 5 V $V_{bb(0)} > V_{bb(SCT)}$
6.9.3	Supply voltage for reduced short circuit shutdown threshold[1)]	$V_{bb(SCT)}$	20	22	25	V	-
6.9.4	Thermal shut down temperature	T_{jt}	150	170 [1)]	-	°C	-
Reverse Battery							
6.9.5	On-State resistance in case of reverse polarity V_{bb}=-8V, T_j=150°C [1)] V_{bb}=-12V, T_j=150°C	$R_{ON(rev)}$	 - -	 12 10	 20 12	mΩ	I_L = -10A, R_{IS} = 1 kΩ
Over-Voltage							
6.9.6	Over-voltage protection Sense pin	$V_{IS(CL)}$	6	9.5	-	V	I_{IS} = -2 mA

1) Not subject to production test, specified by design

7 Diagnostic Functions

For diagnosis purposes, the BTS50050-1EGA provides an Infineon® ENHANCED SENSE signal at the pin IS.

7.1 Diagnosis Enable

In ON-State, diagnosis is allways enabled. Providing a low signal at the DEN pin will disable the reporting. In OFF-state, both, reporting and diagnosis can be disabled by a low signal at DEN pin. The pin IS will be set to tri-state mode when a low signal is provided at the DEN pin. A high signal at the DEN pin enables the reporting and the open load and short to battery diagnosis during OFF mode. A falling edge at the DEN resets a preceding latched output and reporting condition. Please see **Figure 20** and **Table 1** for details.

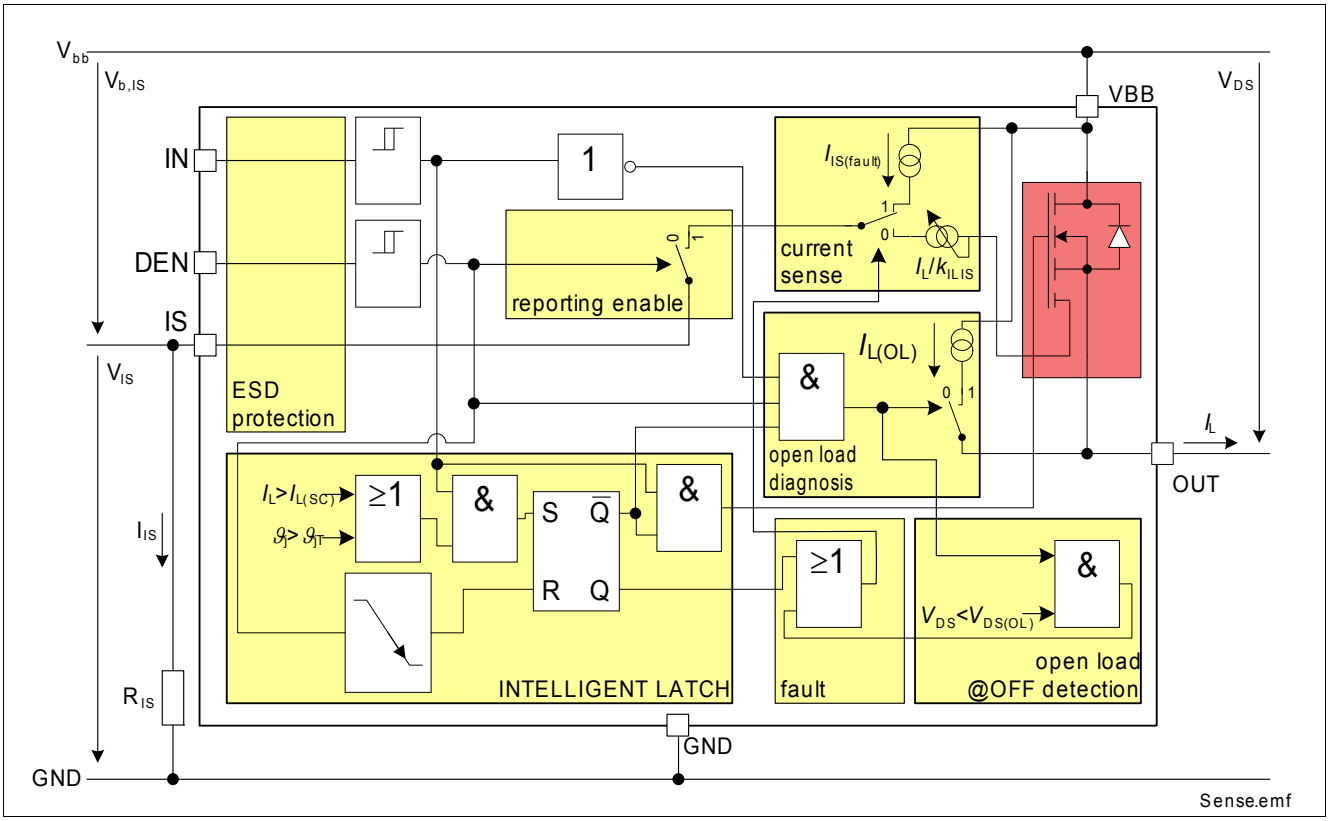


Figure 20 Block Diagram: Diagnosis

Table 1 Truth Table

Operation Mode	Input (IN) Level	Output Level	Diagnostic Output (IS)	
			DEN = H	DEN = L
Normal Operation (ON)	H	~V_{bb}	$I_{IS} = I_L / k_{ILIS}$	Z
Inverse Operation (-I_L)		>V_{bb}	Z	
Short Circuit to GND		Z	$I_{IS(fault)}$	
Over Temperature		Z	$I_{IS(fault)}$	
Short Circuit to V_{bb}		V_{bb}	$I_{IS}<I_L/k_{ILIS}$	
Open Load		~V_{bb}	Z	
Protective switch-off resulting from Short Circuit to GND or Over Temperature [1]	X	Z	$I_{IS(fault)}$	Z
Normal Operation (OFF)	L	Z	Z	Z
Inverse Operation (-I_L)		>V_{bb}	$I_{IS(fault)}$	
Short Circuit to GND		Z	$I_{IS(fault)}$ [2], Z [3]	
Over Temperature				
Short Circuit to V_{bb}		>V_{bb}-$V_{DS(OL)}$ <V_{bb}-$V_{DS(OL)}$	$I_{IS(fault)}$ Z	
Open Load		>V_{bb}-$V_{DS(OL)}$ <V_{bb}-$V_{DS(OL)}$	$I_{IS(fault)}$ Z	

L = Low Level, H = High Level, Z = high impedance, only leakage provided, potential depends on external circuit

1) Output and fault reporting remains latched until falling DEN edge acknowledge.

2) Before fault acknowledgement and latch reset.

3) After fault acknowledgement and latch reset.

7.2 Diagnosis during ON

During normal operation, an enabled IS pin provides a sense current, which is proportional to the load current as long as $V_{b,IS}$>5V and as long as I_{IS}*R_{IS}<$V_{Z,IS}$. The ratio of the output current is defined as k_{ILIS}=I_L/I_{IS}. During switch-on sense current is provided after a sense settling time $t_{sIS(ON)}$. During inverse operation and switch-off no current is provided.

The output sense current is limited to $I_{IS,lim}$. Please refer to **Figure 21** for details.

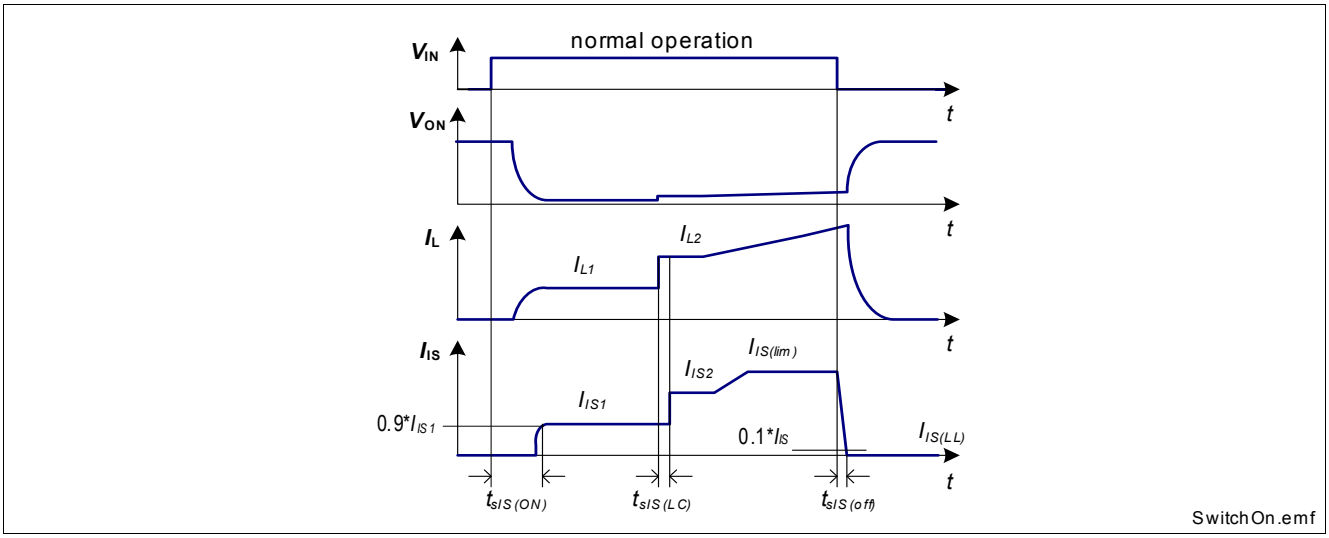


Figure 21 Timing of Diagnosis Signal in ON-state

The accuracy of the provided current sense ratio ($k_{ILIS} = I_L / I_{IS}$) depends on the load current. Please refer to **Figure 22** for details. A typical resistor R_{IS} of 1 kΩ is recommended (see also **Chapter 6.7**).

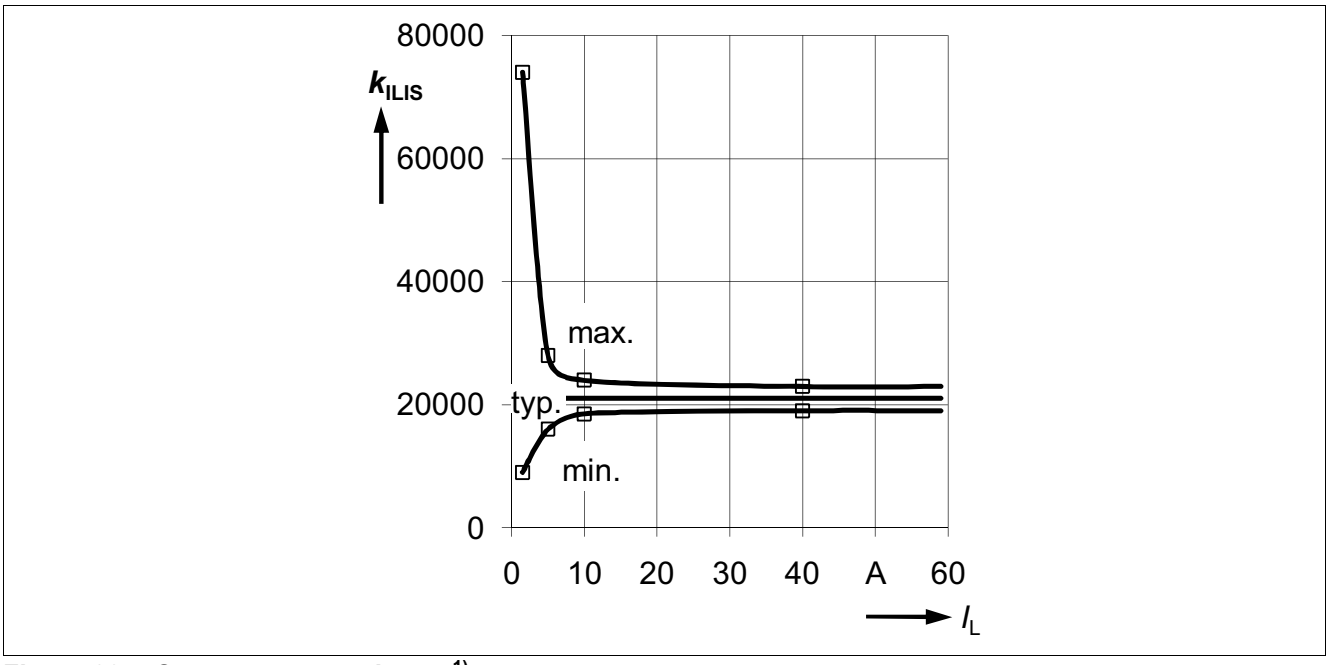


Figure 22 Current sense ratio k_{ILIS}[1)]

The diagnosis signal can be switched off by a low signal at the diagnosis enable pin DEN. See **Figure 23** for details on the timing between the DEN pin and the diagnosis signal I_{IS}. Please note that the diagnosis is disabled, when no signal is provided at the pin DEN.

1) The curves show the behavior based on characterization data. The marked points are described in this Datasheet in **Section 7.5** (Position **7.5.5**).

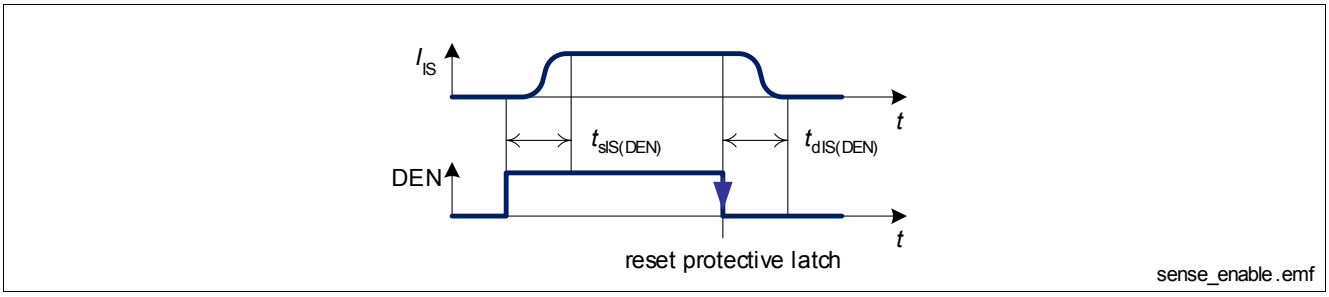


Figure 23 Timing of Sense Enable Signal

During fault condition an enabled IS pin provides a defined fault current $I_{IS(fault)}$. Fault conditions are over-current, over-temperature and short circuit switch-off. Any protective switch-off during on-state causes a latched OFF of the output and reporting, until being reset by a falling edge at the pin DEN. See **Figure 24** for details.

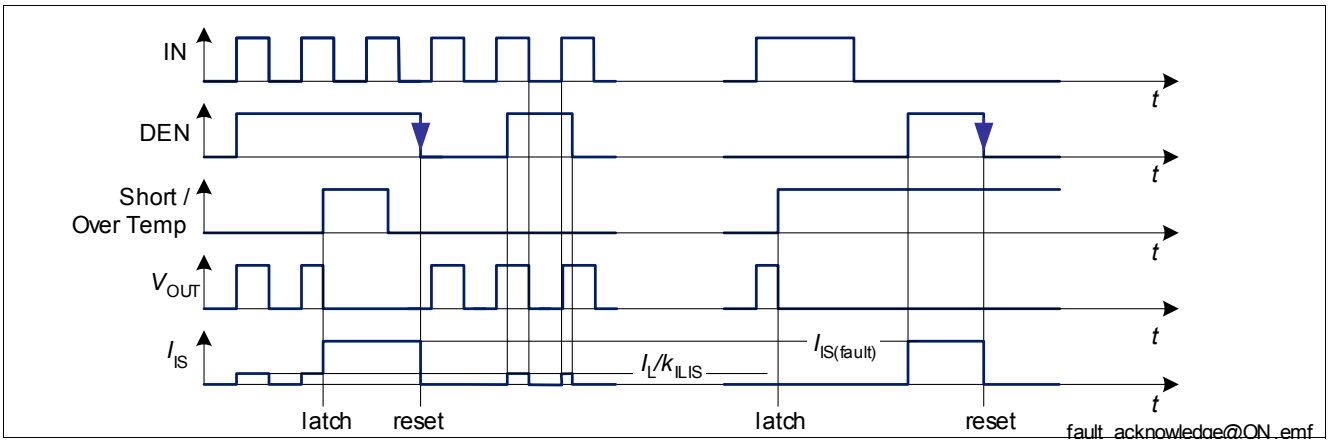


Figure 24 Fault acknowledge and latch reset

7.3 Diagnosis during OFF

During normal operation a disabled IS pin provides no current.

In case of shorted load to battery, open load or inverse operation an enabled IS pin provides a defined fault current $I_{IS(fault)}$. See **Figure 25** for details.

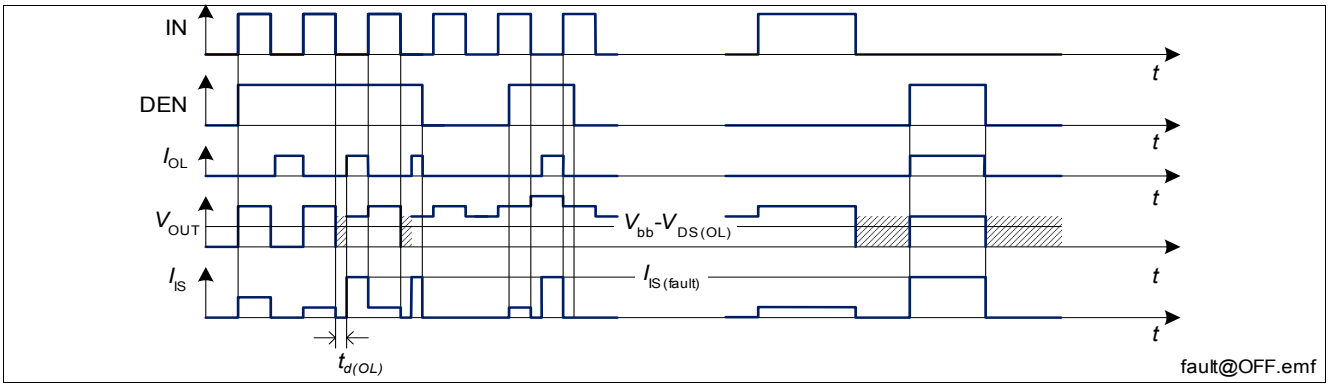


Figure 25 Fault reporting

7.4 Diagnosis Disable

In order to achieve minimum standby current, the IN pin and the DEN pin have to be low level. A possible preceding fault condition and reporting has to be reset by a falling edge at the pin DEN. See also **Chapter 6.4** for details.

7.5 Electrical Characteristics: Diagnostic Functions

Note: Characteristics show the deviation of parameters at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Input characteristics for Diagnosis Enable							
7.5.1	L-input level	$V_{DEN(L)}$	-0.3	-	1.0	V	–
7.5.2	H-input level	$V_{DEN(H)}$	2.0	-	5.5	V	–
7.5.3	input hysteresis	$V_{DEN(hys)}$	–	100	-	mV	1)
7.5.4	input pull down resistor	R_{DEN}	50	100	200	kΩ	–
Load Current Sense							
7.5.5	Current sense ratio, static on-condition	k_{ILIS}	-	21	-	k	V_{IN} = V_{DEN} = 5 V, I_{IS} < $I_{IS(lim)}$, V_{IS} < $V_{Z,IS}$, $V_{b,IS}$ > 5 V
	I_L=40A		19	21	23		
	I_L=10A		18.5	21	24		
	I_L=5A		16	21	28		
	I_L=1.5A		9	21	74		
	V_{IN} = 0 (e.g. during de energizing of inductive loads)		disabled			–	–
7.5.6	Sense saturation current 1)	$I_{IS(lim)}$	3.5	6	10	mA	V_{DEN} = 5 V, V_{ON} < 400 mV, typ. $V_{b,IS}$ > 5 V
7.5.7	Sense current under fault conditions	$I_{IS(fault)}$	3.5	6	10	mA	V_{DEN} = 5 V, $V_{b,IS}$ > 5 V, V_{ON} > 400 mV,typ. or V_{OFF}<$V_{DS(OL)}$
7.5.8	Current sense leakage current	$I_{IS(LL)}$	–	0.1	0.5	µA	V_{IN}=V_{DEN}=0V
7.5.9	Current sense offset current	$I_{IS(LH)}$				µA	V_{IN}=V_{DEN}=5V, $I_L \leq$ 0A
	T_j = -40 °C, T_j = 25 °C		–	8	30		
	T_j = 150 °C		–	18	60		
7.5.10	Current sense leakage, while diagnosis disabled	$I_{IS(dis)}$	–	1	2	µA	V_{IN} = 5V, V_{DEN} = 0V
7.5.11	Current sense settling time to 90% $I_{IS\_stat.}$ 1)	$t_{sIS(ON)}$	–	350	700	µs	V_{IN} = 0↗5V (switch-on), V_{DEN} = 5 V, R_L = 0.5 Ω
7.5.12	Current sense settling time to 10% $I_{IS\_stat.}$ 1)	$t_{sIS(OFF)}$	–	8	30	µs	V_{IN} = 5↘0V (switch-off), V_{DEN} = 5V, R_L = 0.5Ω
7.5.13	Current sense settling time to 90% $I_{IS\_stat.}$ 1)	$t_{sIS(LC)}$	–	15	50	µs	V_{IN}=V_{DEN}=5V, I_L = 10↗20A
7.5.14	Current sense settling time to 90% $I_{IS\_stat.}$ 1)	$t_{sIS(DEN)}$	–	8	30	µs	V_{IN} = 5V, OUT=ON, V_{DEN} = 0↗5V

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.5.15	Current sense deactivation time to 10% $I_{IS\_stat.}$ [1]	$t_{dIS(DEN)}$	–	2	20	µs	V_{IN} = 5V, V_{DEN} = 5↘0V
Open Load at OFF state							
7.5.16	Open load output current	$I_{L(OL)}$	3	5	10	mA	V_{IN} = 0V, V_{DEN} = 5V, V_{DS} = 2V
7.5.17	Open load detection threshold voltage	$V_{DS(OL)}$	2	2.8	3.5	V	V_{IN} = 0V, V_{DEN} = 5V
7.5.18	Open load blanking after negative input slope [1]	$t_{d(OL)}$	–	0.3	1	ms	V_{IN} = 5↘0 V, V_{DEN} = 5V, V_{bb} = 13.5V,

1) Not subject to production test, specified by design

8 Application schematic

Figure 26 shows an example for an application schematic.

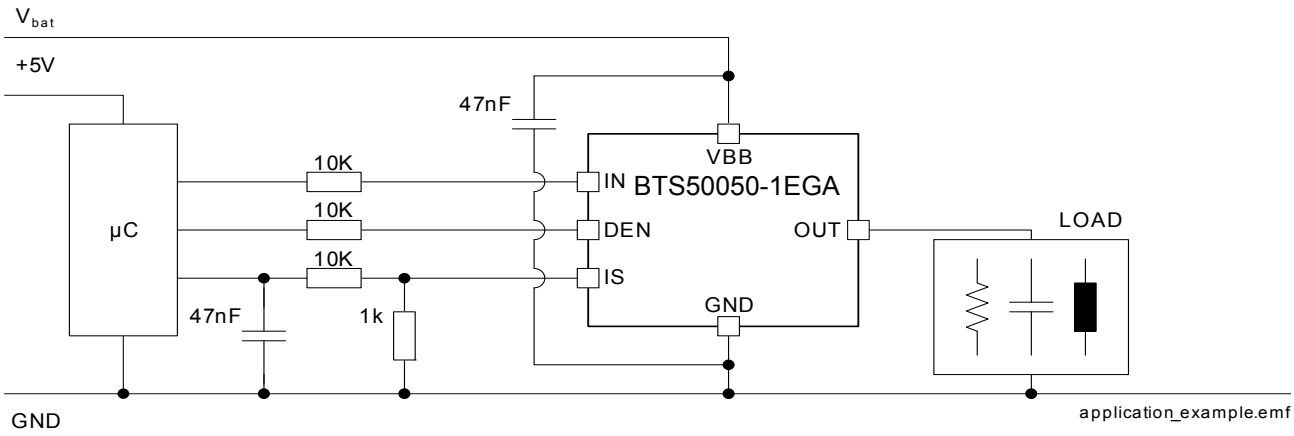


Figure 26 application example

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

8.1 Hints for PCB layout

- Handling of NC pins: It is recommended to connect all NC pins on a defined potential. E.g. pin 7 and pin 12 could be connected to OUT potential, while pin 5 and 6 could be connected to OUT or DEN.
- EMC filter cap between Vbb and GND: It is recommended to place the filter cap as close as possible to the device to minimize the inductance of the loop.
- The resistors connecting µC and IN-pin as well as µC and DEN-pin are recommended to protect the µC inputs against fast electrical transients.
- Ground shift: It is recommended to avoid a ground shift between µC ground and device pin GND of more than 0.3V during normal operation.

8.2 Further Application Information

- Please contact us to get the Pin FMEA
- Please contact us to get a test report on short circuit robustness according to AEC Q100-012
- Please contact us for Application Note “Diagnosis with BTS500x0-1EGA”
- For further information you may contact **http://www.infineon.com/**

9 Package Outlines

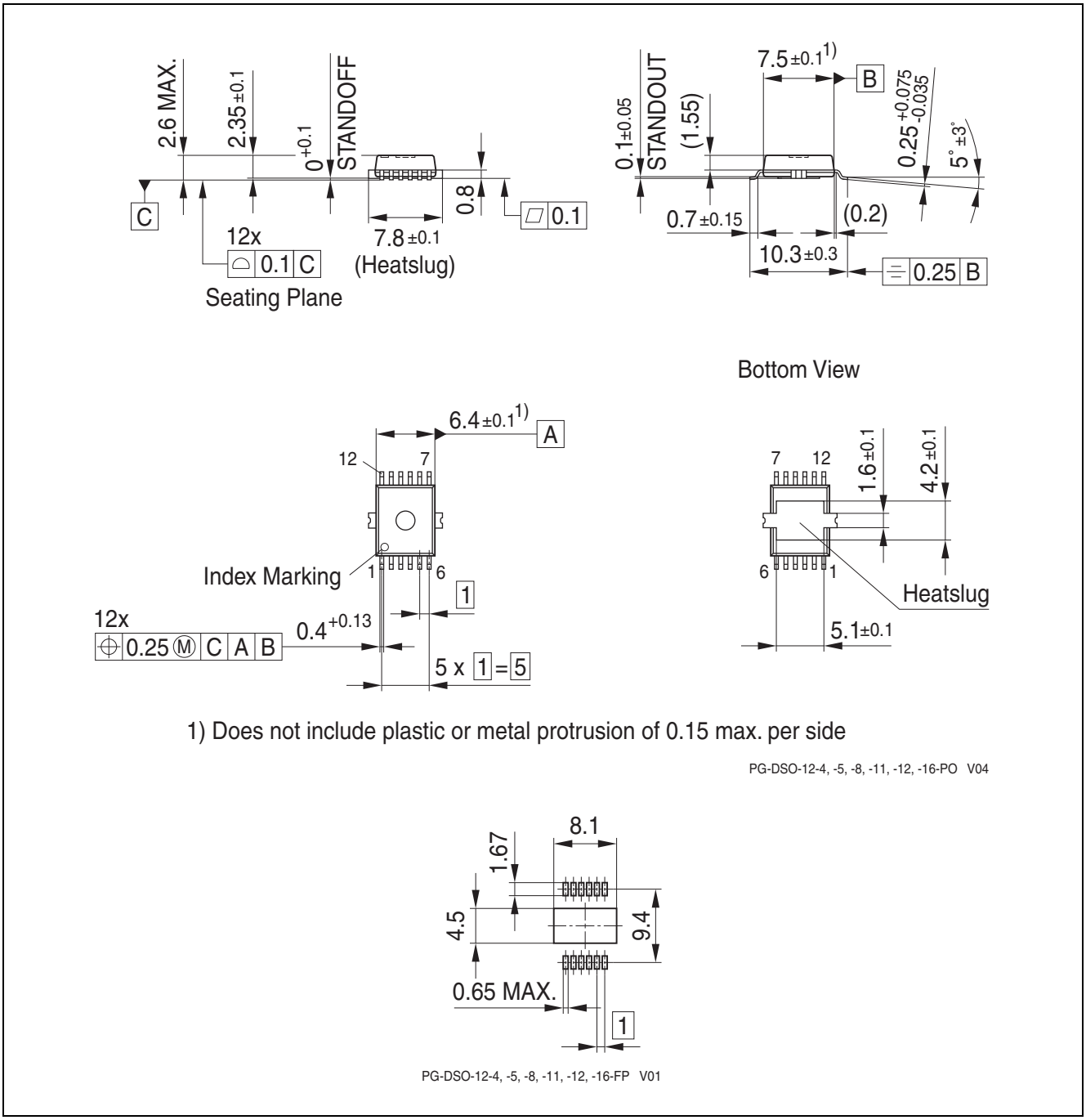


Figure 27 PG-DSO-12-16 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

10 Revision History

BTS50050-1EGA

Revision History: V1.1, 2011-08-16

Version	Date	Changes
Datasheet Rev. 1.1	2011-08-16	Update from production distribution data **Chapter 5.8**: Parameter $I_{bb(OFF)}$ and $I_{L(OFF)}$ limits tightened for T_j=150°C. Typical value updated. **Chapter 5.8**: Parameter t_{ON}, t_{OFF}, $(dV/dt)_{ON}$ and $-(dV/dt)_{OFF}$ limits tightened. Typical values updated. **Chapter 6.9**: Parameter $I_{L(SC)high}$ limits tightened for T_j=150°C. **Chapter 6.9**: Parameter $V_{IS(CL)}$ limits tightened. **Chapter 7.5**: Parameter k_{ILIS} limits tightened for I_L = 5A, 10A, 40A. **Figure 22** updated. **Chapter 4.3**, **Chapter 6.9**: Parameter numbering corrected.
Datasheet Rev. 1.0	2009-04-06	Initial version of datasheet.

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