

SMPS MOSFET **IRF3703PbF**

HEXFET® Power MOSFET

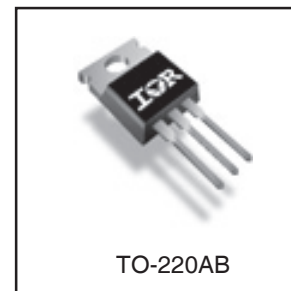
Applications

- Synchronous Rectification
- Active ORing
- Lead-Free

V_{DSS}	$R_{DS(on) \max}$	I_D
30V	2.8m Ω	210A ^⑥

Benefits

- Ultra Low On-Resistance
- Low Gate Impedance to Reduce Switching Losses
- Fully Avalanche Rated



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	210 ^⑥	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	100 ^⑥	
I_{DM}	Pulsed Drain Current ^①	1000	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	230	W
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	3.8	
	Linear Derating Factor	1.5	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ^③	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.65	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Notes ^① through ^⑥ are on page 8
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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.028	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	2.3	2.8	mΩ	V _{GS} = 10V, I _D = 76A ④
		—	2.8	3.9		V _{GS} = 7.0V, I _D = 76A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	250		V _{DS} = 24V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V

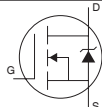
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	150	—	—	S	V _{DS} = 24V, I _D = 76A
Q _g	Total Gate Charge	—	209	—	nC	I _D = 76A
Q _{gs}	Gate-to-Source Charge	—	62	—		V _{DS} = 24V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	42	—		V _{GS} = 10V, ④
t _{d(on)}	Turn-On Delay Time	—	18	—	ns	V _{DD} = 15V, V _{GS} = 10V
t _r	Rise Time	—	123	—		I _D = 76A
t _{d(off)}	Turn-Off Delay Time	—	53	—		R _G = 1.8Ω
t _f	Fall Time	—	24	—		V _{GS} = 10V ④
C _{iss}	Input Capacitance	—	8250	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	3000	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	290	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	10360	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	3060	—		V _{GS} = 0V, V _{DS} = 24V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	2590	—		V _{GS} = 0V, V _{DS} = 0V to 24V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	1700	mJ
I _{AR}	Avalanche Current③	—	76	A
E _{AR}	Repetitive Avalanche Energy④	—	23	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	210⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	1000		
V _{SD}	Diode Forward Voltage	—	0.8	1.3	V	T _J = 25°C, I _S = 76A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	80	120	ns	T _J = 25°C, I _F = 76A, V _{DS} = 16V
Q _{rr}	Reverse Recovery Charge	—	185	275	nC	di/dt = 100A/μs ④

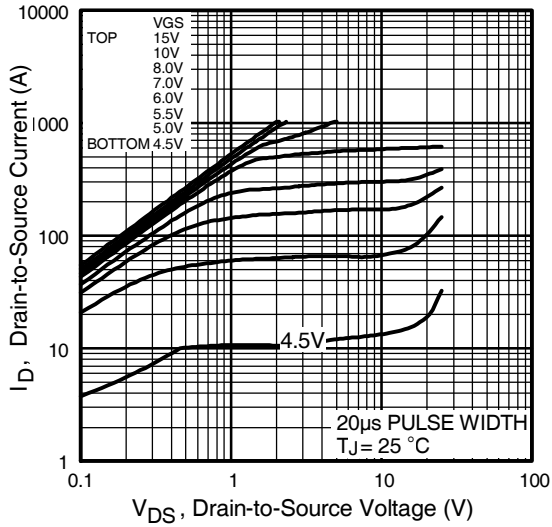


Fig 1. Typical Output Characteristics

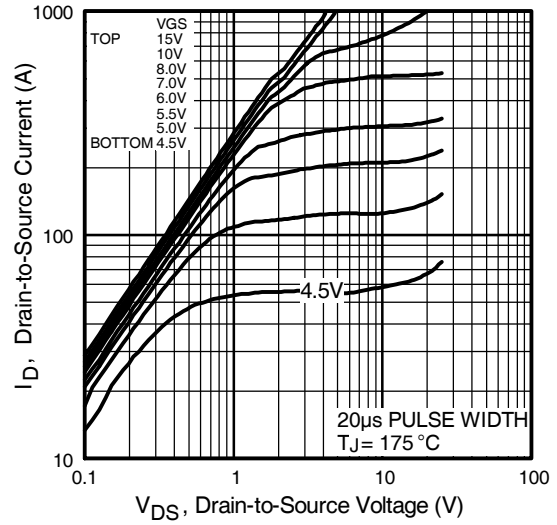


Fig 2. Typical Output Characteristics

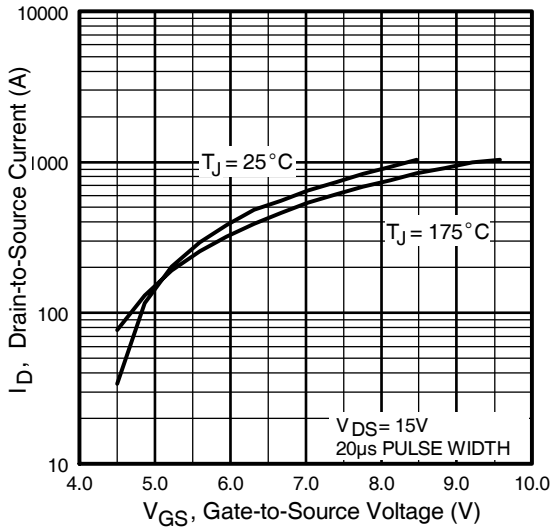


Fig 3. Typical Transfer Characteristics

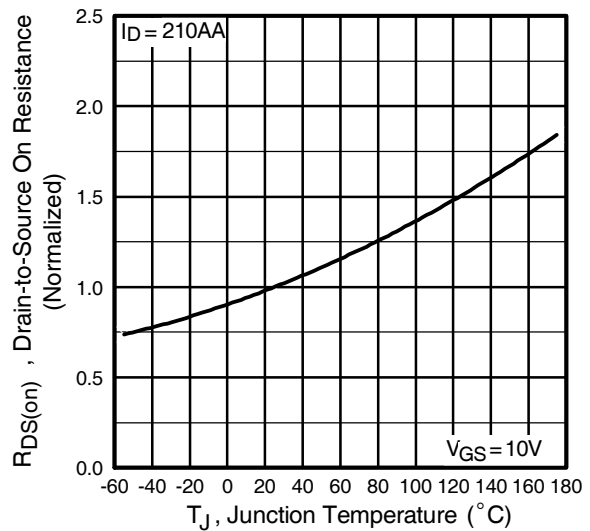


Fig 4. Normalized On-Resistance Vs. Temperature

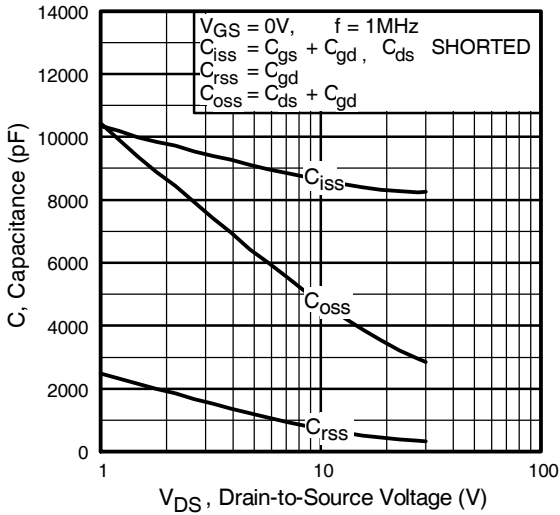


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

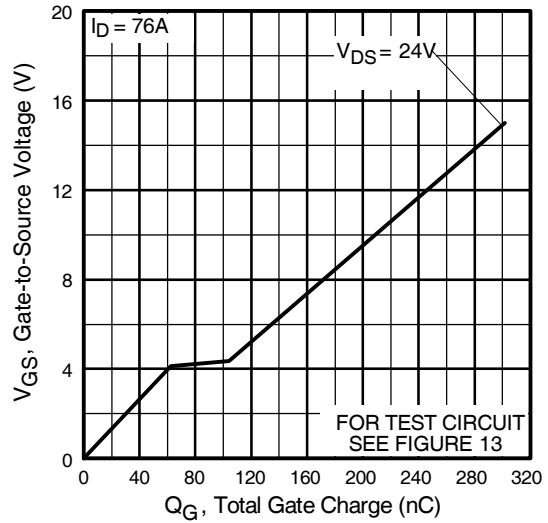


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

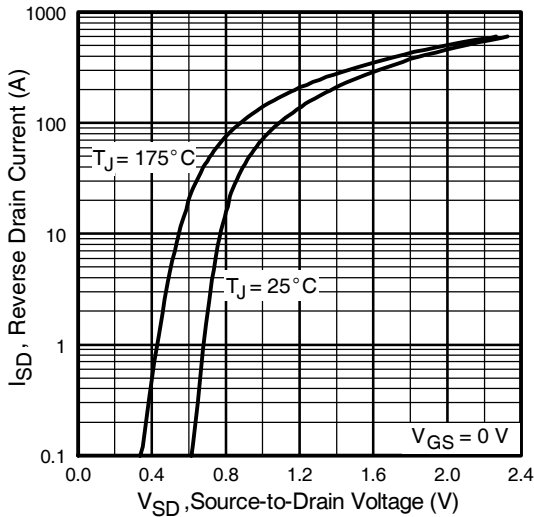


Fig 7. Typical Source-Drain Diode Forward Voltage

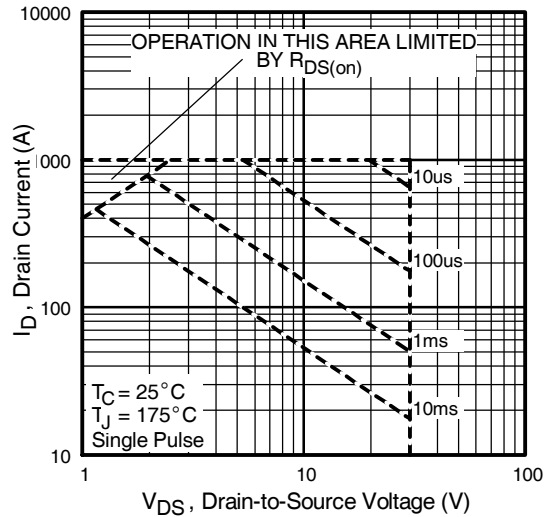


Fig 8. Maximum Safe Operating Area

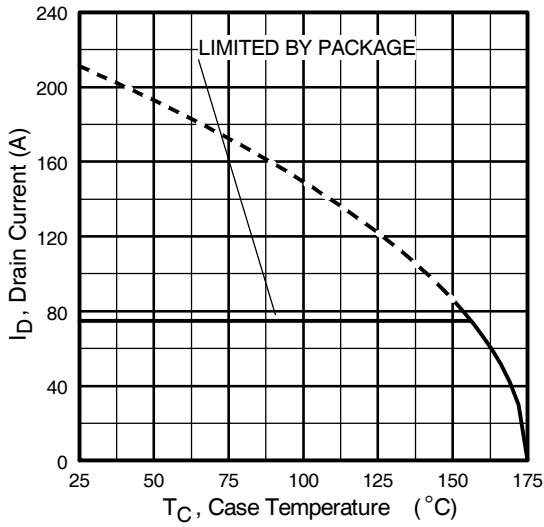


Fig 9. Maximum Drain Current Vs. Case Temperature

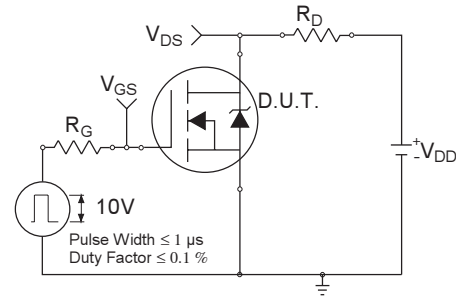


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

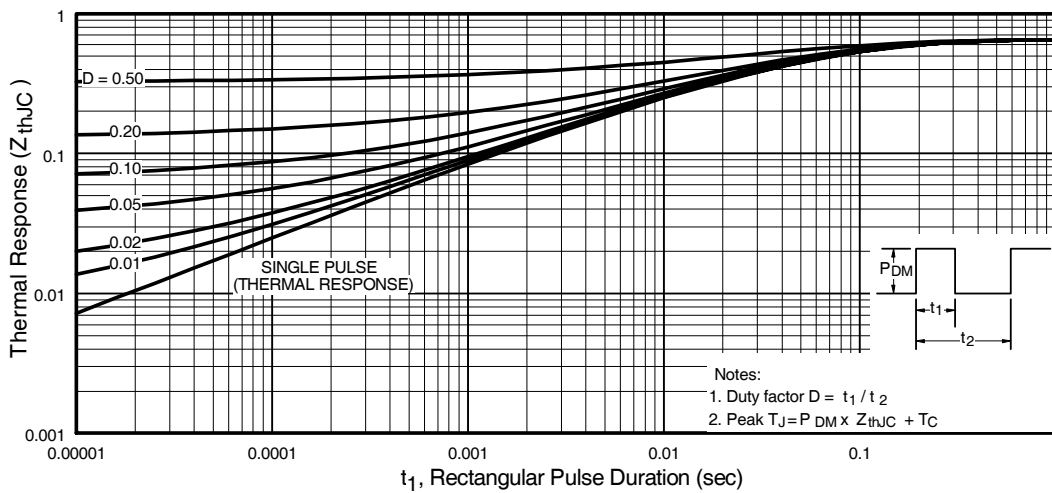


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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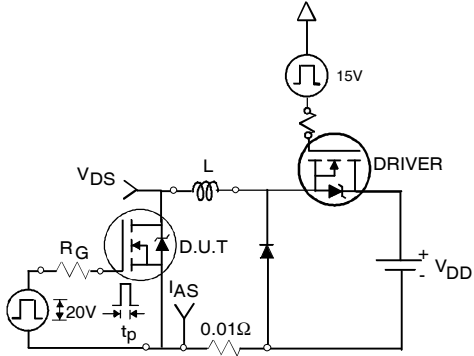


Fig 12a. Unclamped Inductive Test Circuit

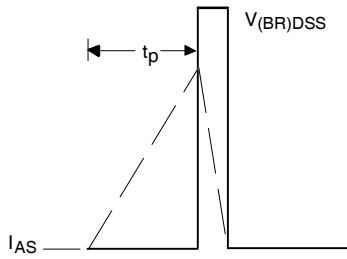


Fig 12b. Unclamped Inductive Waveforms

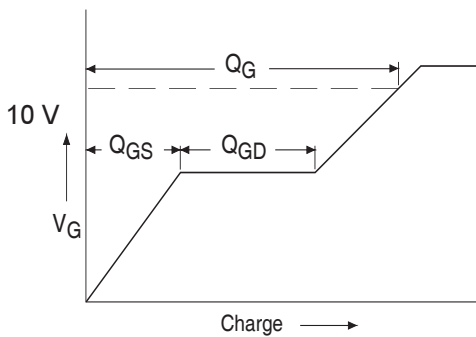


Fig 13a. Basic Gate Charge Waveform

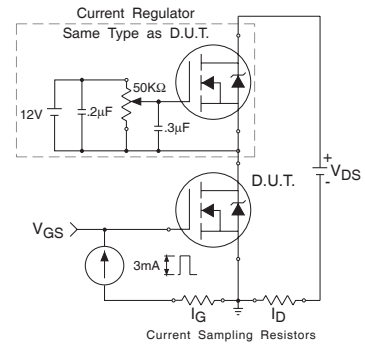


Fig 13b. Gate Charge Test Circuit

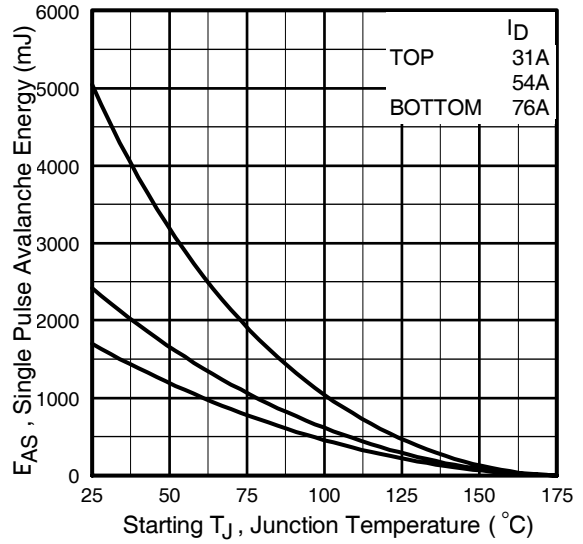


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Peak Diode Recovery dv/dt Test Circuit



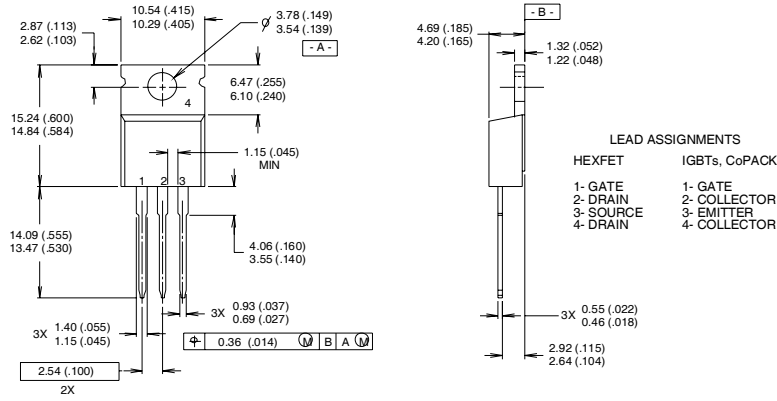
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET[®] Power MOSFET

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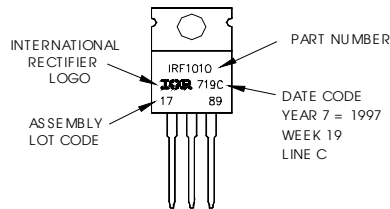
TO-220AB Package Outline



- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION : INCH
 - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
 - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line
position indicates "Lead-Free"



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.6\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 76\text{A}$.
- ③ $I_{SD} \leq 76\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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