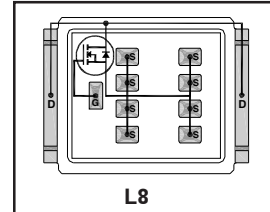


- RoHS Compliant, Halogen Free ①
- Lead-Free (Qualified up to 260°C Reflow)
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①
- Industrial Qualified

DirectFET™ Power MOSFET ②  
Typical values (unless otherwise specified)

<b>V<sub>DSS</sub></b>	<b>V<sub>GS</sub></b>	<b>R<sub>DS(on)</sub></b>
60V min	±20V max	1.1mΩ @ 10V
<b>Q<sub>g tot</sub></b>	<b>Q<sub>gd</sub></b>	<b>V<sub>gs(th)</sub></b>
200nC	71nC	2.9V



Applicable DirectFET Outline and Substrate Outline ①

<b>SB</b>	<b>SC</b>		<b>M2</b>	<b>M4</b>	<b>L4</b>	<b>L6</b>	<b>L8</b>
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### Description

The IRF7749L2TR/TR1PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has a footprint smaller than a D<sup>2</sup>PAK and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems.

The IRF7749L2TR/TR1PbF is optimized for high frequency switching and synchronous rectification applications. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance power converters.

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRF7749L2TRPbF	DirectFET2 Large Can	Tape and Reel	4000	"TR" suffix
IRF7749L2TR1PbF	DirectFET2 Large Can	Tape and Reel	1000	"TR1" suffix EOL notice # 264

### Absolute Maximum Ratings

	Parameter	Max.	Units
V <sub>DS</sub>	Drain-to-Source Voltage	60	V
V <sub>GS</sub>	Gate-to-Source Voltage	±20	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited) ④	200	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited) ④	140	
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited) ③	33	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited) ④	375	
I <sub>DM</sub>	Pulsed Drain Current ⑤	800	
E <sub>AS</sub>	Single Pulse Avalanche Energy ⑥	260	mJ
I <sub>AR</sub>	Avalanche Current ⑤	120	A

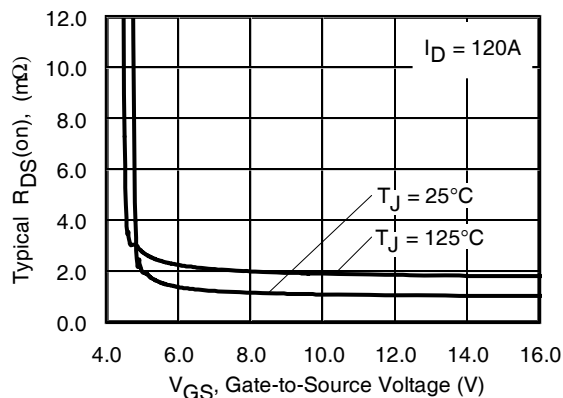


Fig 1. Typical On-Resistance vs. Gate Voltage

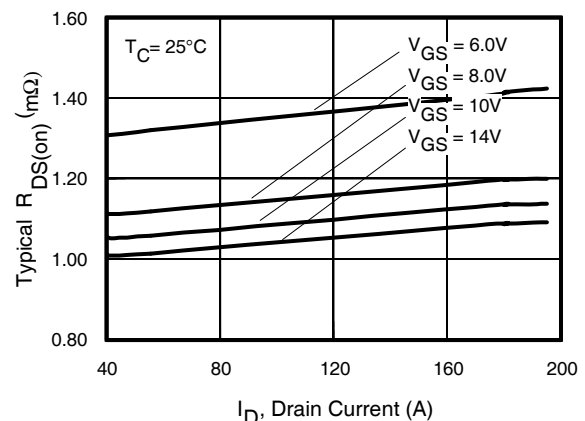


Fig 2. Typical On-Resistance vs. Drain Current

Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

- ④ T<sub>C</sub> measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting T<sub>J</sub> = 25°C, L = 0.035mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 120A.

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.03	—	V/°C	Reference to 25°C, I <sub>D</sub> = 2mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	1.1	1.50	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 120A ⑦
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	2.9	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-10	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
gfs	Forward Transconductance	280	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 120A
Q <sub>g</sub>	Total Gate Charge	—	200	300	nC	V <sub>DS</sub> = 30V V <sub>GS</sub> = 10V I <sub>D</sub> = 120A See Fig. 9
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	36	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	12	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	71	110		
Q <sub>godr</sub>	Gate Charge Overdrive	—	100	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	83	—		
Q <sub>oss</sub>	Output Charge	—	67	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	1.1	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	17	—	ns	V <sub>DD</sub> = 30V, V <sub>GS</sub> = 10V ⑦ I <sub>D</sub> = 120A R <sub>G</sub> = 1.8Ω
t <sub>r</sub>	Rise Time	—	43	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	78	—		
t <sub>f</sub>	Fall Time	—	39	—		
C <sub>iss</sub>	Input Capacitance	—	12320	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1810	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	850	—		
C <sub>oss</sub>	Output Capacitance	—	8060	—		
C <sub>oss</sub>	Output Capacitance	—	1310	—		

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	200	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ⑤	—	—	800		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 120A, V <sub>GS</sub> = 0V ⑦
t <sub>rr</sub>	Reverse Recovery Time	—	45	68	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 120A, V <sub>DD</sub> = 30V
Q <sub>rr</sub>	Reverse Recovery Charge	—	78	120	nC	di/dt = 100A/μs ⑦

**Notes:**

⑤ Repetitive rating; pulse width limited by max. junction temperature.

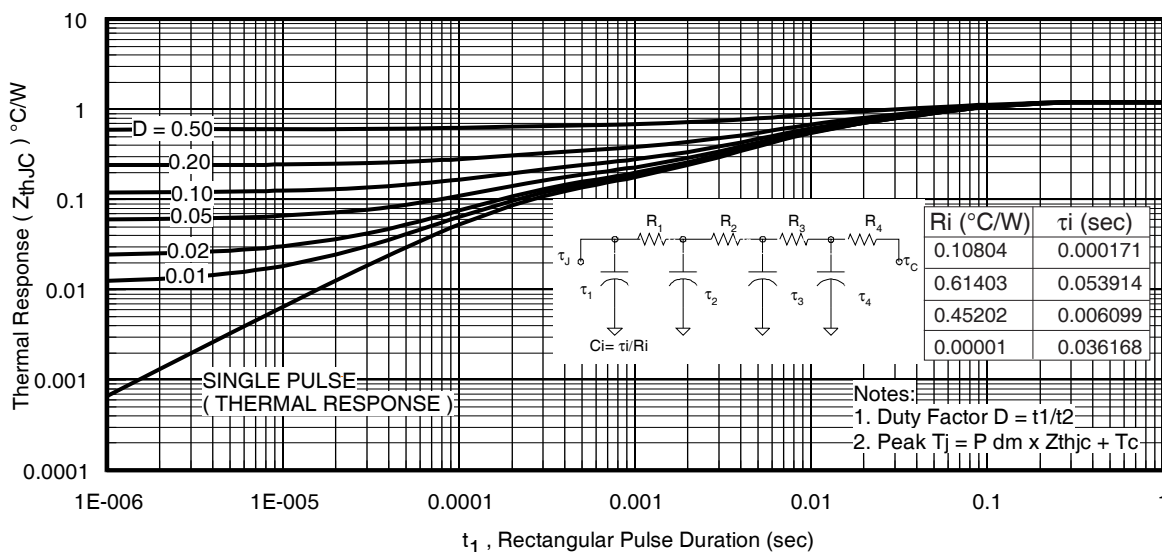
⑦ Pulse width ≤ 400μs; duty cycle ≤ 2%.

**Absolute Maximum Ratings**

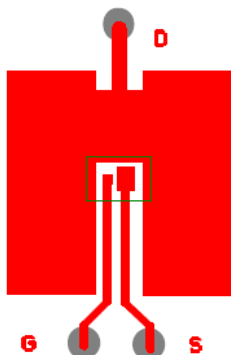
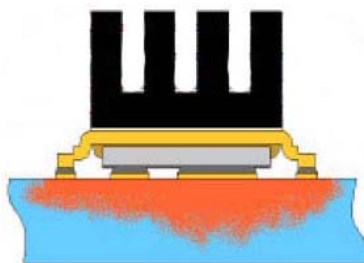
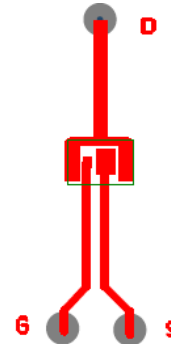
	Parameter	Max.	Units
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	125	W
$P_D @ T_C = 100^\circ\text{C}$	Power Dissipation ④	63	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ①	3.3	
$T_P$	Peak Soldering Temperature	270	°C
$T_J$	Operating Junction and	-55 to + 175	
$T_{STG}$	Storage Temperature Range		

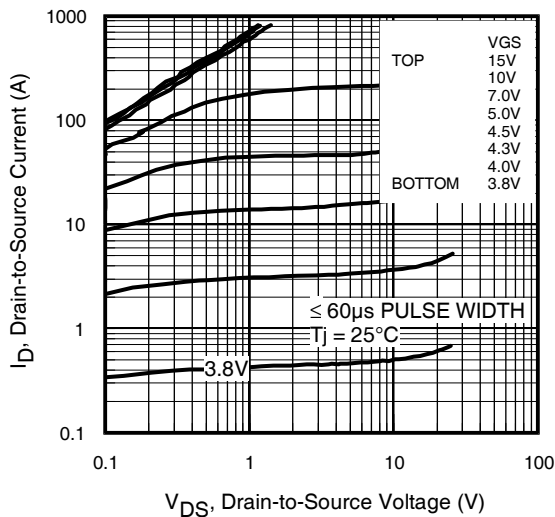
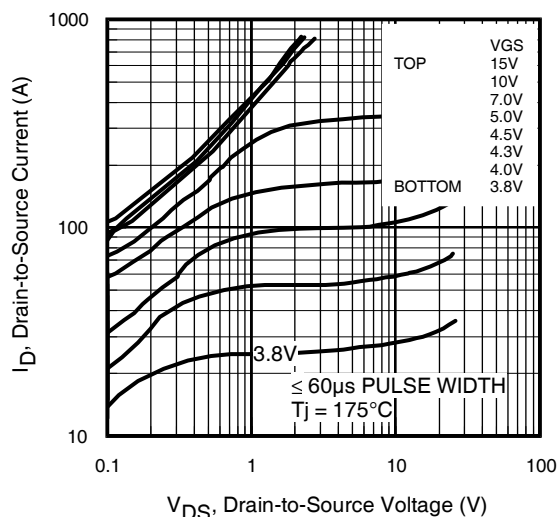
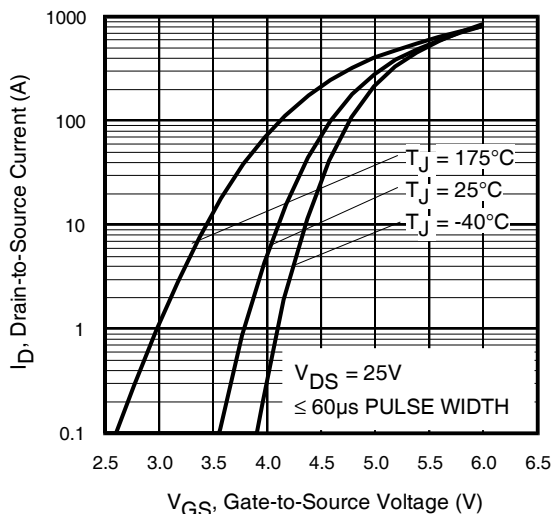
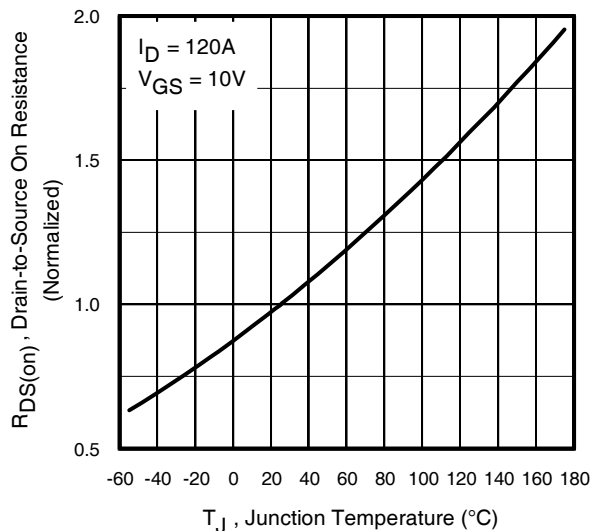
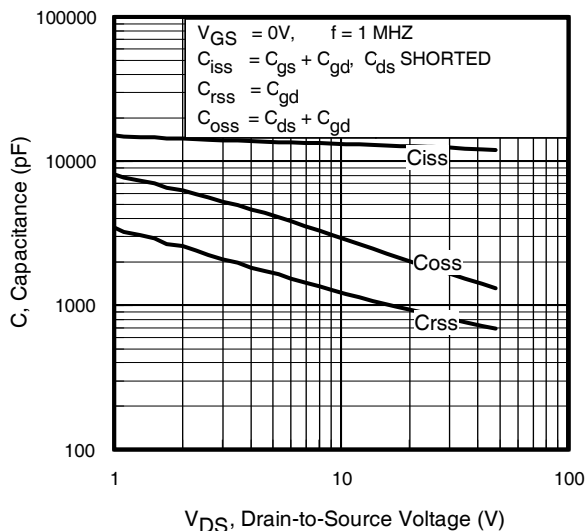
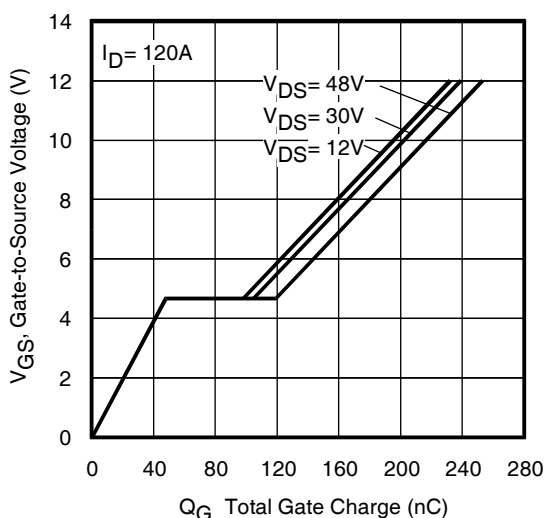
**Thermal Resistance**

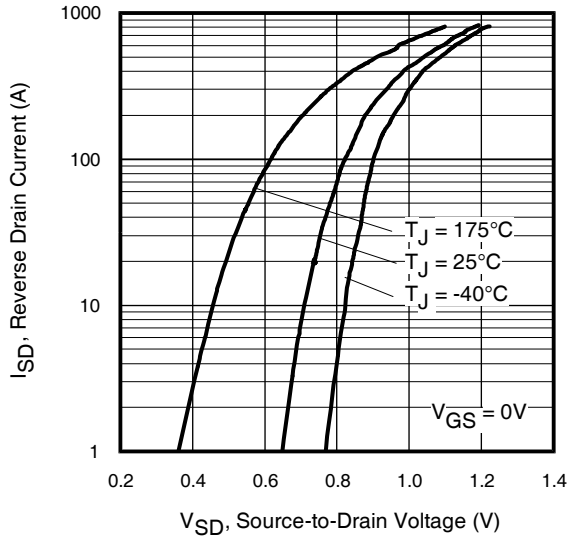
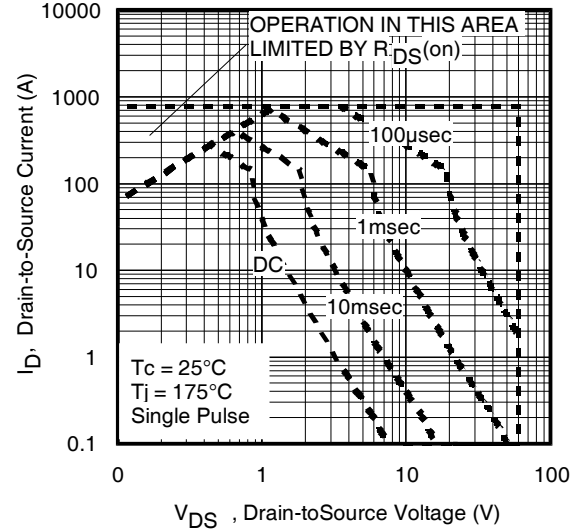
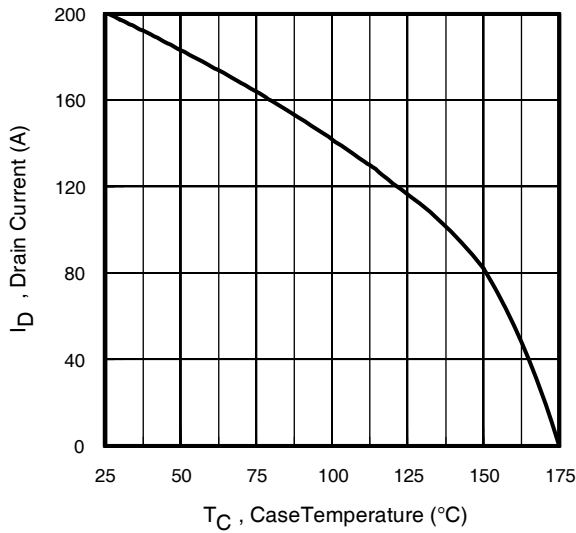
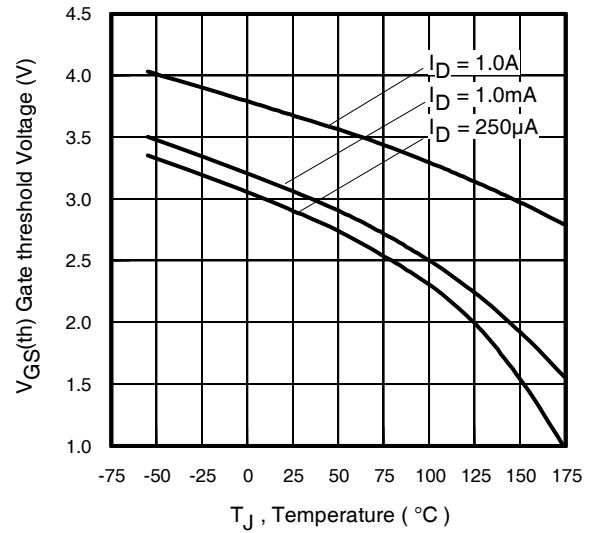
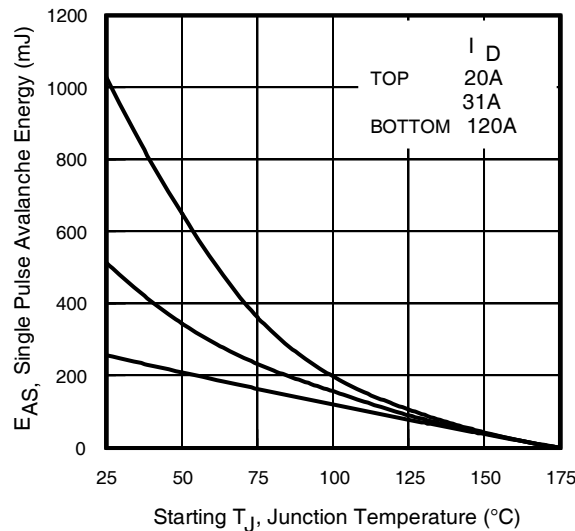
	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑧	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨	20	—	
$R_{\theta J-Can}$	Junction-to-Can ④⑩	—	1.2	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	—	0.5	

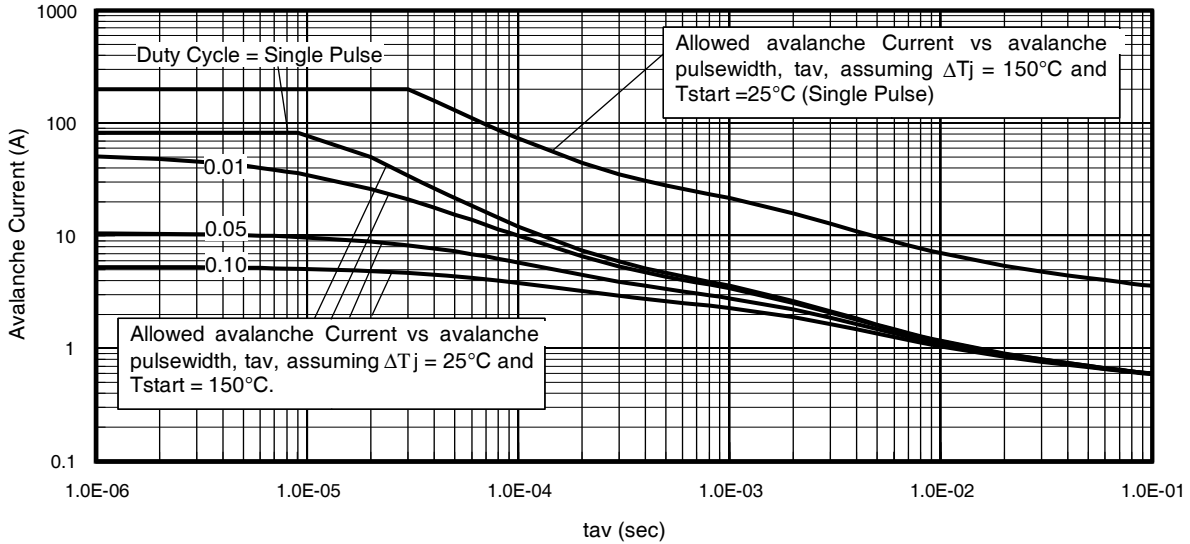
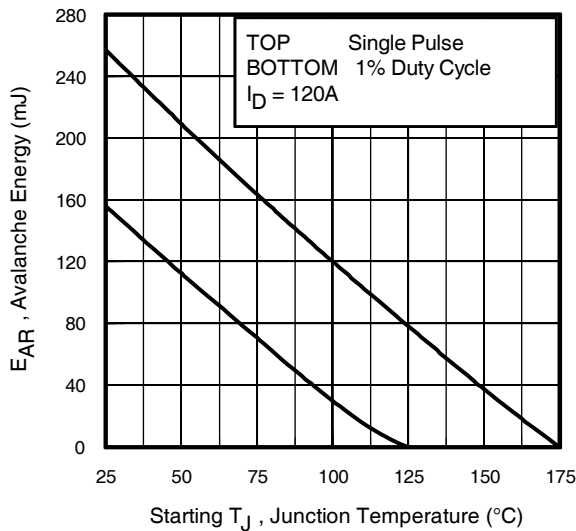

**Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Case ④**
**Notes:**

- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④  $T_C$  measured with thermocouple incontact with top (Drain) of part.
- ⑤ Used double sided cooling, mounting pad with large heatsink.
- ⑧ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑩  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .


**③** Surface mounted on 1 in. square Cu board (still air).

**⑧** Mounted on minimum footprint full size board with metalized back and with small clip heatsink. (still air)



**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Output Characteristics**

**Fig 6. Typical Transfer Characteristics**

**Fig 7. Normalized On-Resistance vs. Temperature**

**Fig 8. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 9. Typical Total Gate Charge vs. Gate-to-Source Voltage**


**Fig 10.** Typical Source-Drain Diode Forward Voltage

**Fig11.** Maximum Safe Operating Area

**Fig 12.** Maximum Drain Current vs. Case Temperature

**Fig 13.** Typical Threshold Voltage vs. Junction Temperature

**Fig 14.** Maximum Avalanche Energy Vs. Drain Current

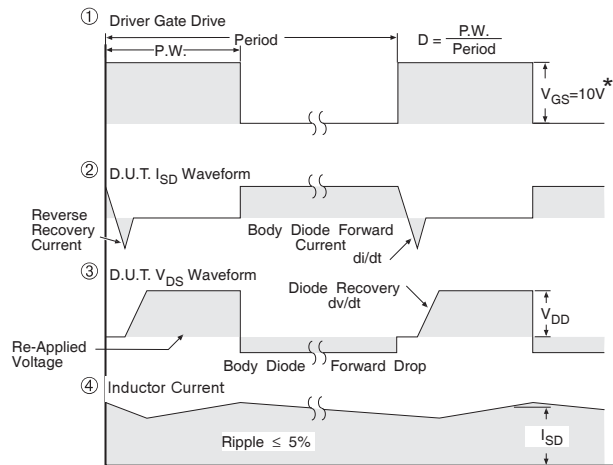
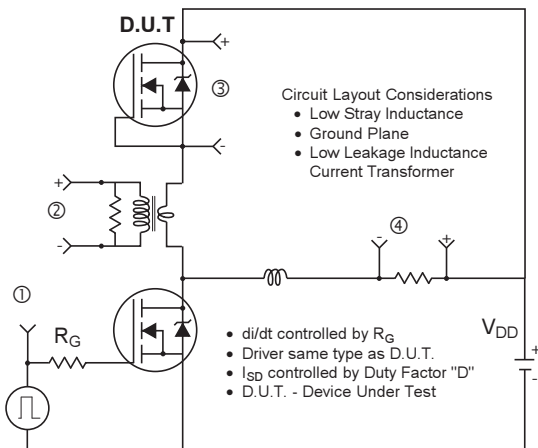

**Fig 15. Typical Avalanche Current Vs. Pulsewidth**

**Fig 16. Maximum Avalanche Energy Vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 19a, 19b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

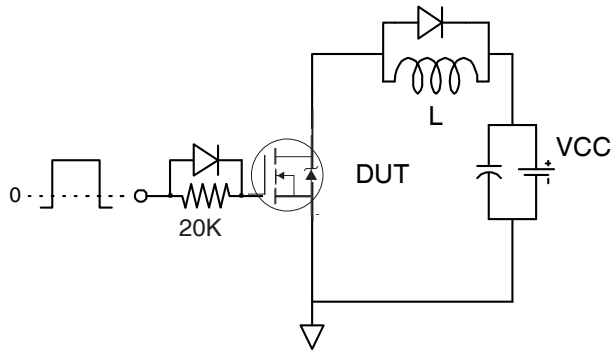
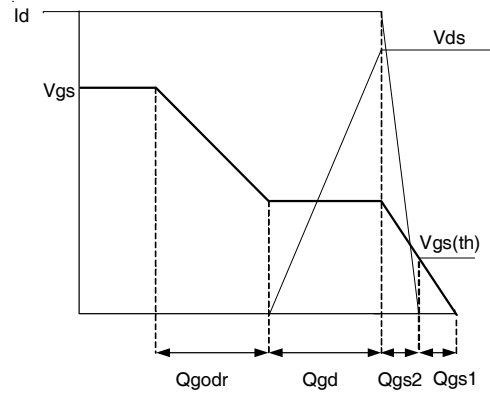
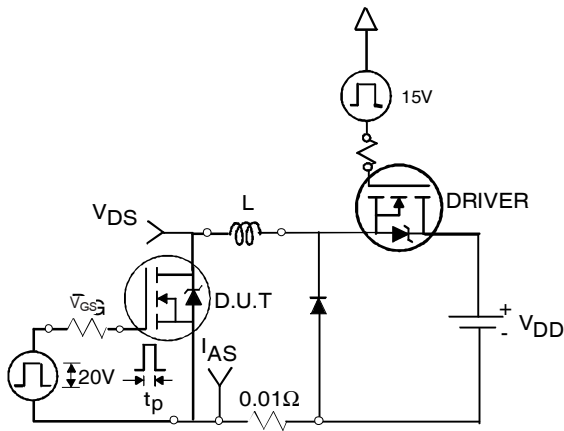
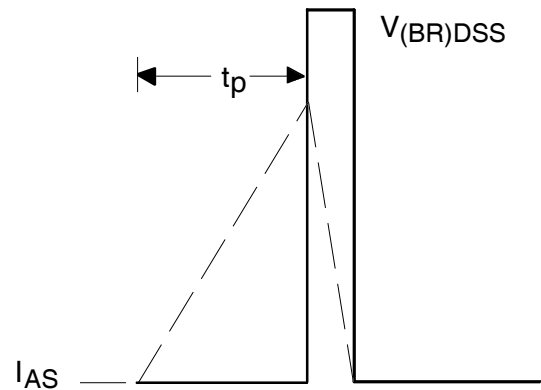
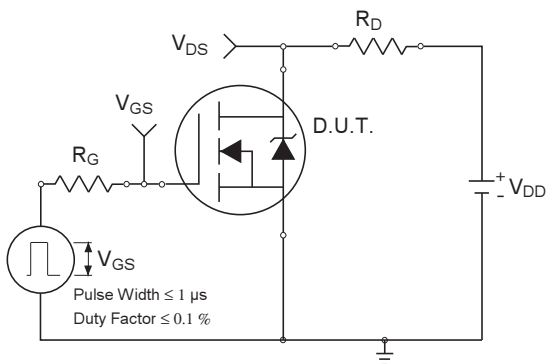
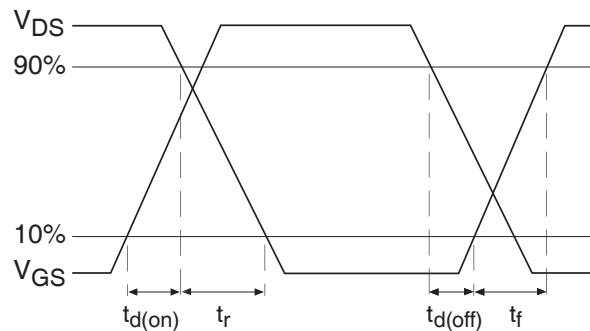
$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{thJC} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_a$$



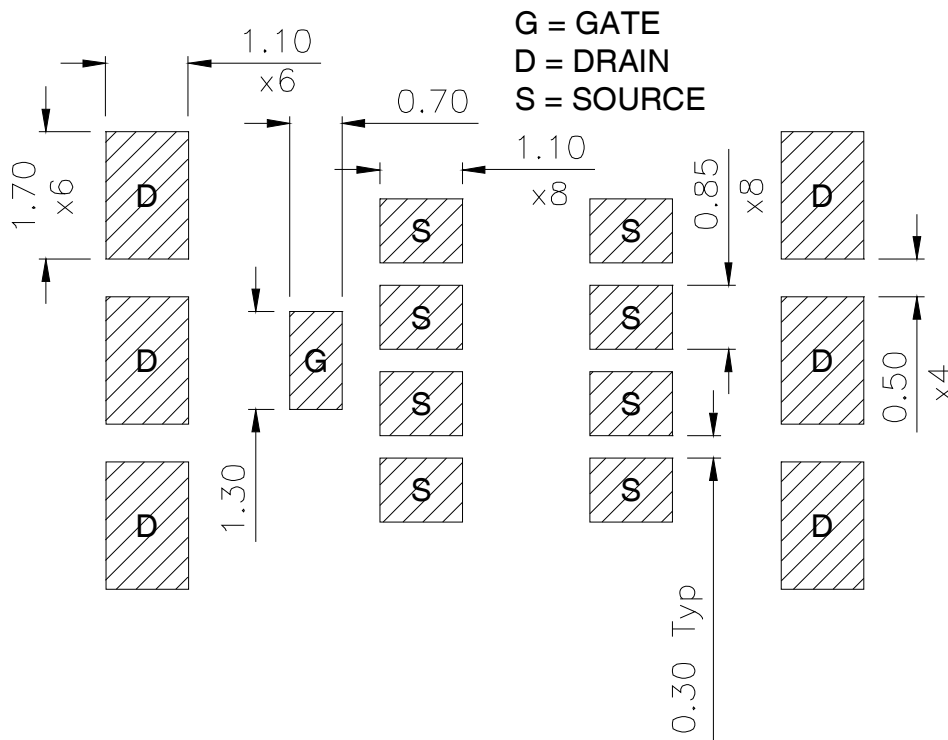
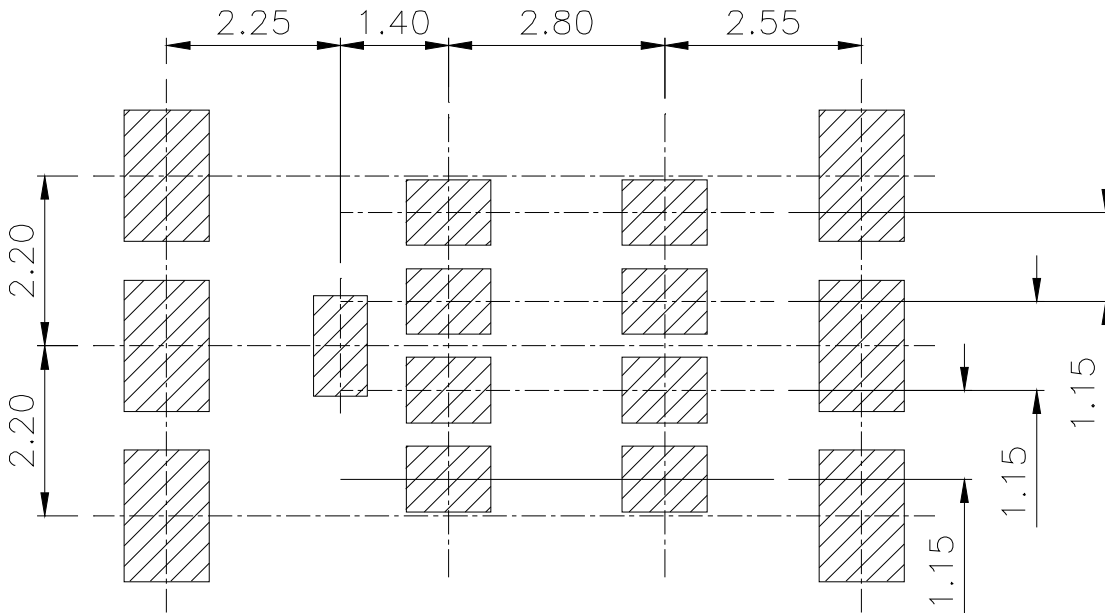
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 17. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs**


**Fig 18a. Gate Charge Test Circuit**

**Fig 18b. Gate Charge Waveform**

**Fig 19a. Unclamped Inductive Test Circuit**

**Fig 19b. Unclamped Inductive Waveforms**

**Fig 20a. Switching Time Test Circuit**

**Fig 20b. Switching Time Waveforms**

### DirectFET™ Board Footprint, L8 (Large Size Can).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations

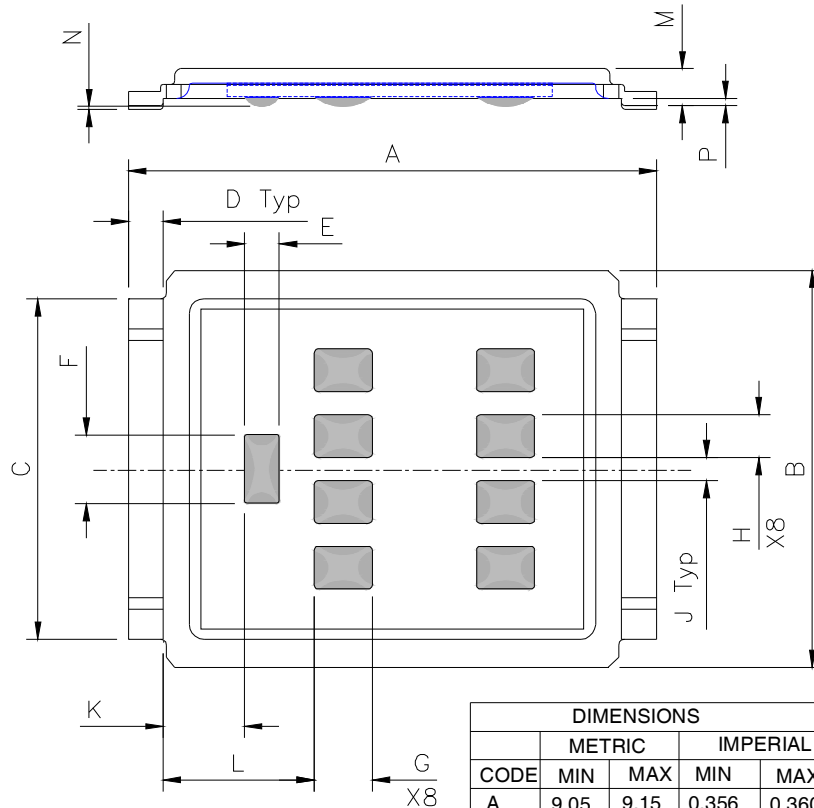


Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



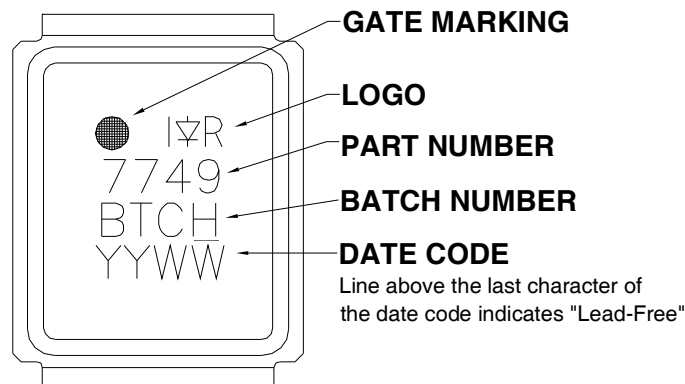
### DirectFET™ Outline Dimension, L8 Outline (LargeSize Can).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations



DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	9.05	9.15	0.356	0.360
B	6.85	7.10	0.270	0.280
C	5.90	6.00	0.232	0.236
D	0.55	0.65	0.022	0.026
E	0.58	0.62	0.023	0.024
F	1.18	1.22	0.046	0.048
G	0.98	1.02	0.015	0.017
H	0.73	0.77	0.029	0.030
J	0.38	0.42	0.015	0.017
K	1.34	1.47	0.053	0.058
L	2.52	2.69	0.099	0.106
M	0.59	0.70	0.023	0.028
N	0.03	0.08	0.001	0.003
P	0.09	0.18	0.003	0.007

### DirectFET™ Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



**Qualification Information<sup>†</sup>**

Qualification level	Industrial <sup>††</sup>	
	(per JEDEC JESD47F <sup>†††</sup> guidelines)	
	Comments: This family of products has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level	DFET2	MSL1 (per JEDEC J-STD-020D <sup>†††</sup> )
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
5/6/2014	<ul style="list-style-type: none"> <li>Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #264).</li> <li>Updated data sheet based on corporate template.</li> </ul>

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