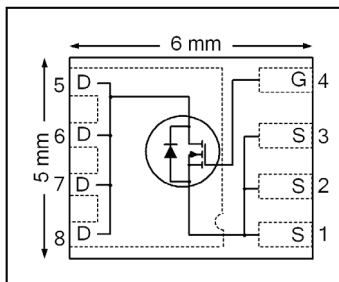


**Application**

- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- DC/DC converters
- DC/AC Inverters

HEXFET® Power MOSFET



<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>0.95mΩ</b>
	<b>max</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>265A①</b>
<b>I<sub>D</sub> (Package Limited)</b>	<b>100A①</b>

**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant



Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH7084PbF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH7084TRPbF

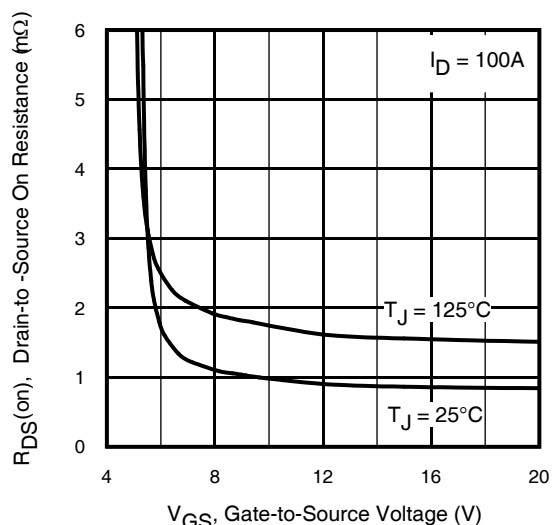


Fig 1. Typical On-Resistance vs. Gate Voltage

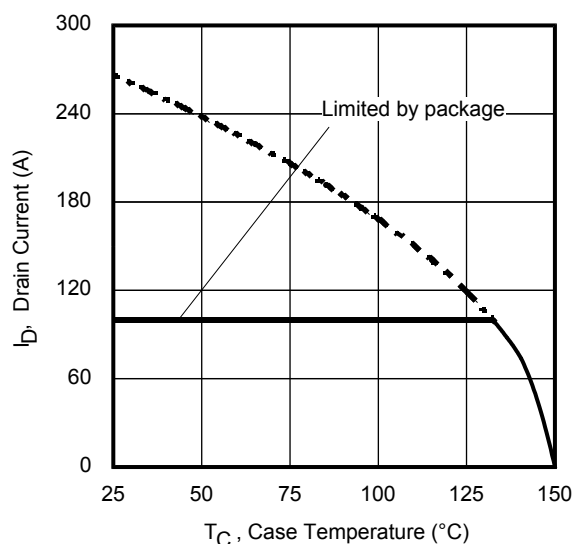


Fig 2. Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	40	A
$I_D @ T_{C(\text{Bottom})} = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	265①	
$I_D @ T_{C(\text{Bottom})} = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	170①	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	100①	
$I_{DM}$	Pulsed Drain Current ①	400	A
	Linear Derating Factor	1.25	W/°C
$P_D @ T_C = 25^\circ\text{C}$	Max Power Dissipation	156	
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	185	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ⑧	431	
$I_{AR}$	Avalanche Current ①	See Fig 14, 15, 23a,	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ⑦	0.5	0.8	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case	—	21	
$R_{\theta JA}$	Junction-to-Ambient ⑨	—	35	
$R_{\theta JA} (<10\text{s})$	Junction-to-Ambient ⑨	—	20	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.034	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.95	1.25	m $\Omega$	$V_{GS} = 10\text{V}, I_D = 100\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.2	—	3.9	V	$V_{DS} = V_{GS}, I_D = 150\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu\text{A}$	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	1.4	—	$\Omega$	

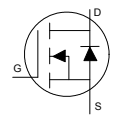
**Notes:**

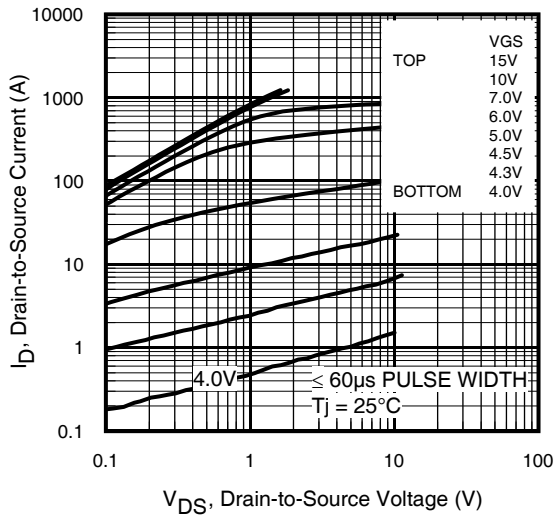
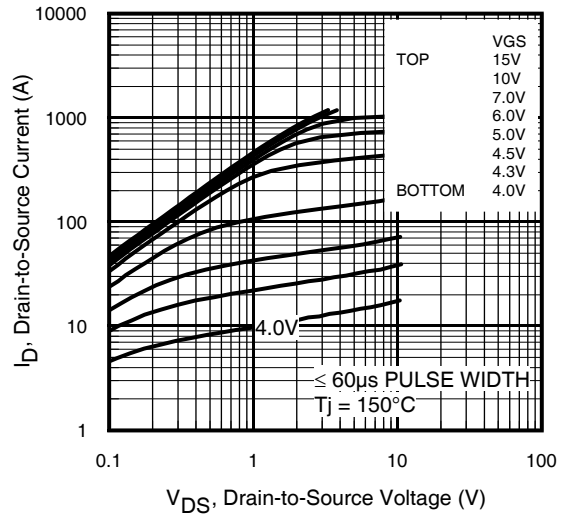
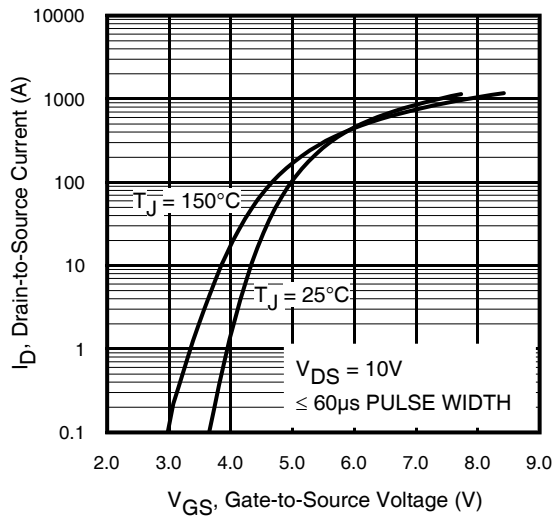
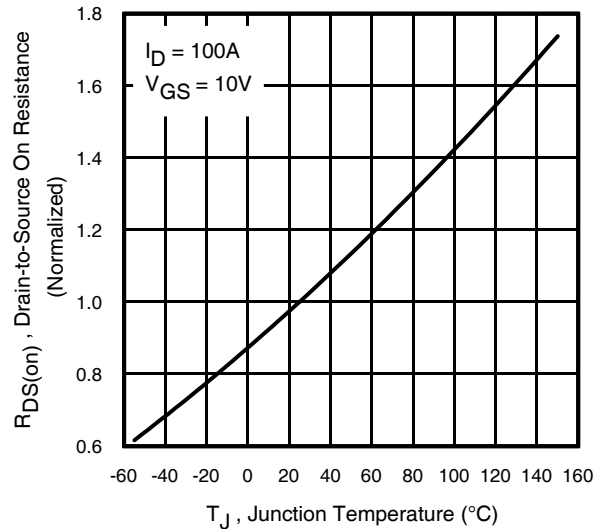
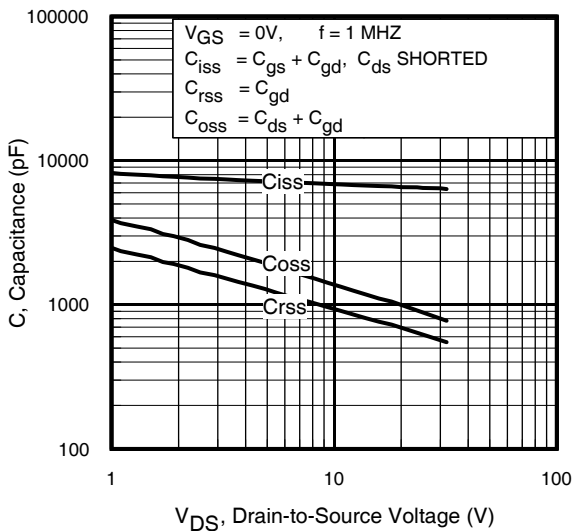
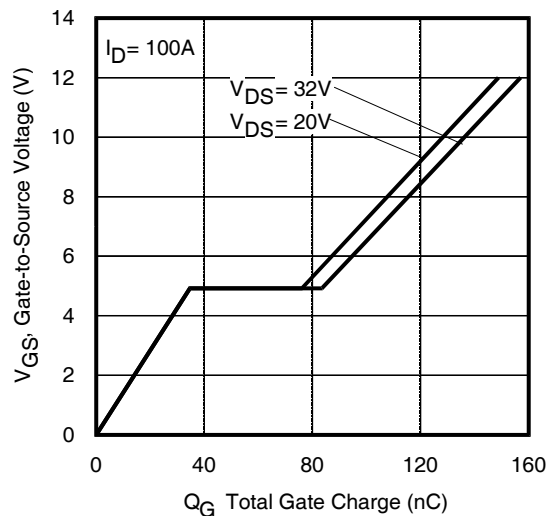
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.037\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 100\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 994\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑧ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 29\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ⑨ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:  
<http://www.irf.com/technical-info/appnotes/an-994.pdf>

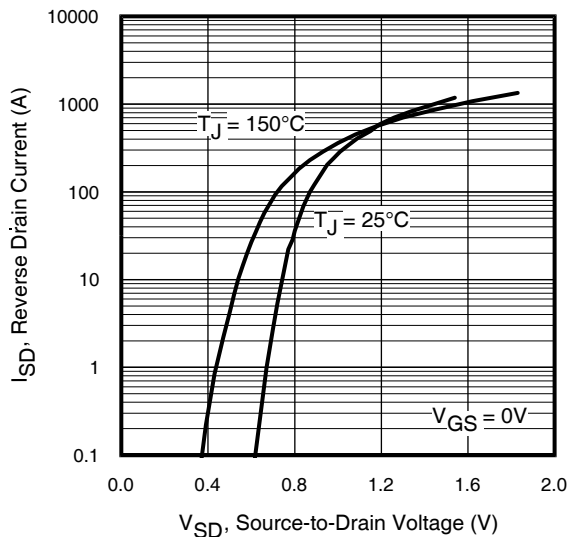
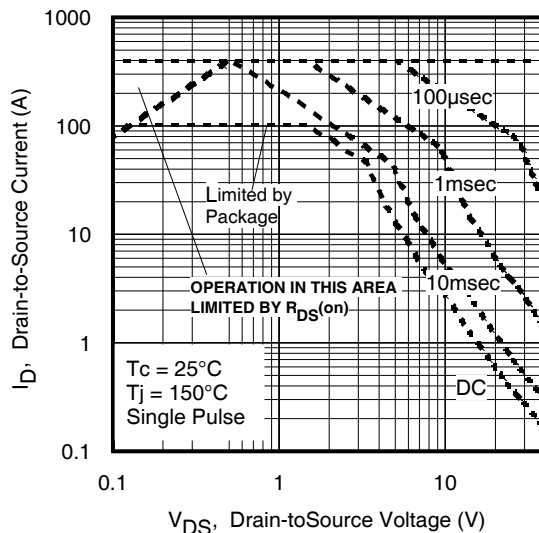
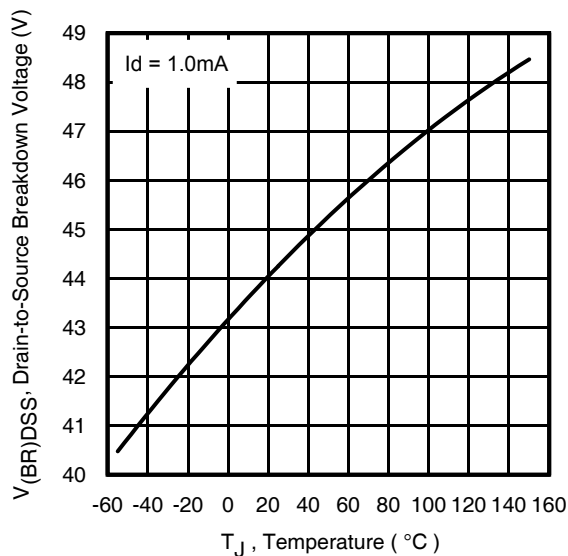
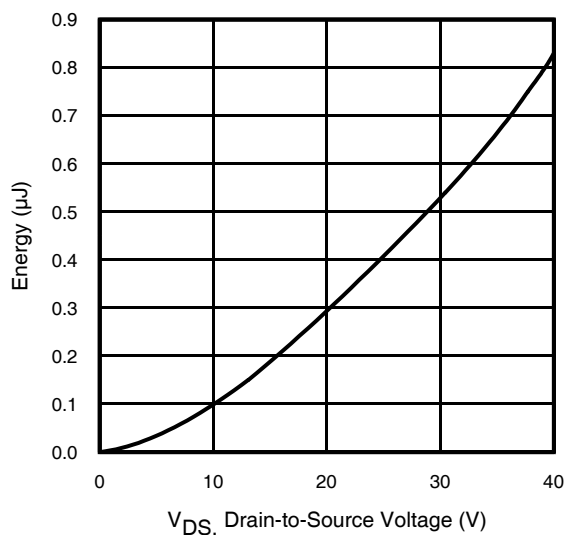
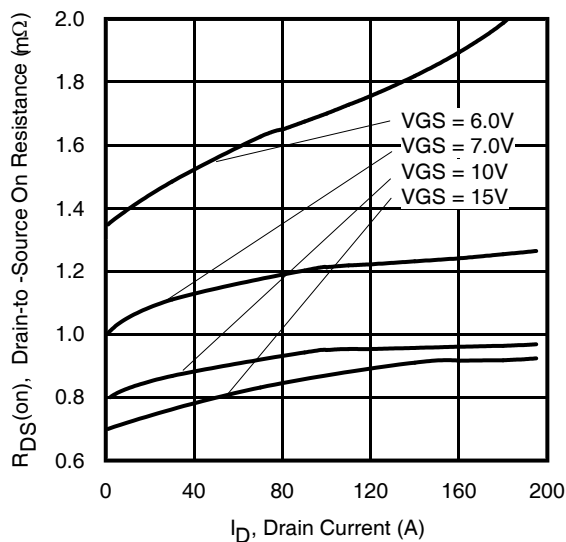
**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

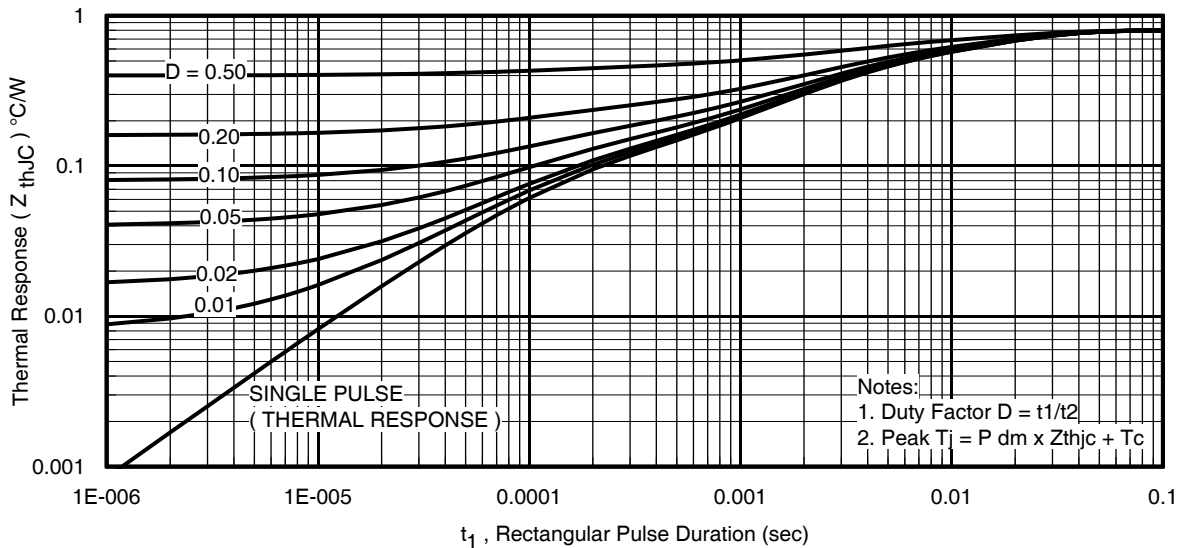
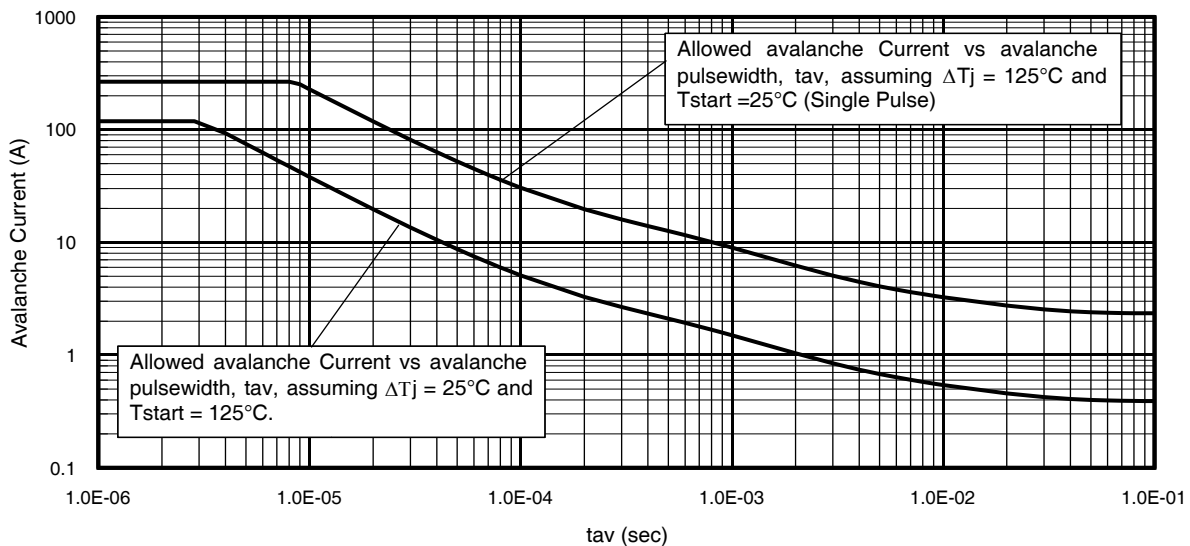
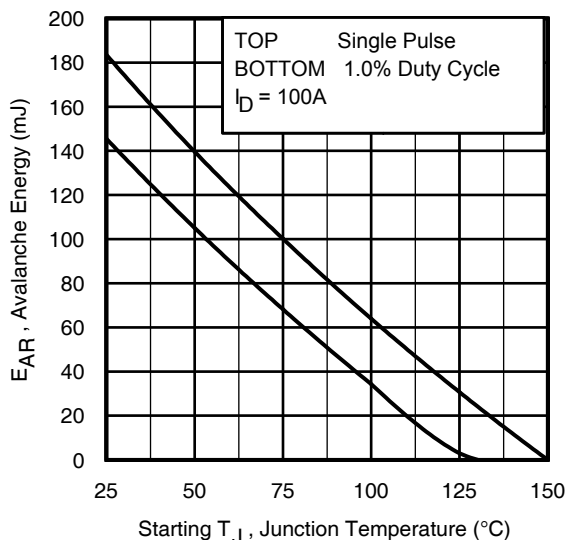
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	120	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 100A
Q <sub>g</sub>	Total Gate Charge	—	127	190	nC	I <sub>D</sub> = 100A V <sub>DS</sub> = 20V V <sub>GS</sub> = 10V
Q <sub>gs</sub>	Gate-to-Source Charge	—	35	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	41	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> – Q <sub>gd</sub> )	—	195	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—	ns	V <sub>DD</sub> = 20V I <sub>D</sub> = 30A R <sub>G</sub> = 2.7Ω V <sub>GS</sub> = 10V④
t <sub>r</sub>	Rise Time	—	31	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	64	—		
t <sub>f</sub>	Fall Time	—	34	—		
C <sub>iss</sub>	Input Capacitance	—	6560	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz, See Fig.5 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 32V⑥ See Fig.11 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 32V⑥
C <sub>oss</sub>	Output Capacitance	—	940	—		
C <sub>riss</sub>	Reverse Transfer Capacitance	—	650	—		
C <sub>oss eff.(ER)</sub>	Effective Output Capacitance (Energy Related)	—	1120	—		
C <sub>oss eff.(TR)</sub>	Output Capacitance (Time Related)	—	1300	—		

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)①	—	—	100①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	400		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 100A, V <sub>GS</sub> = 0V ④
dv/dt	Peak Diode Recovery dv/dt ③	—	4.5	—	V/ns	T <sub>J</sub> = 150°C, I <sub>S</sub> = 100A, V <sub>DS</sub> = 40V③
t <sub>rr</sub>	Reverse Recovery Time	—	36 37	—	ns	V <sub>DD</sub> = 34V I <sub>F</sub> = 100A, di/dt = 100A/μs ④
Q <sub>rr</sub>	Reverse Recovery Charge	—	38 40	—		
I <sub>RRM</sub>	Reverse Recovery Current	—	1.7	—	A	T <sub>J</sub> = 25°C


**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current


**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Typical Avalanche Current vs. Pulse width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)  
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

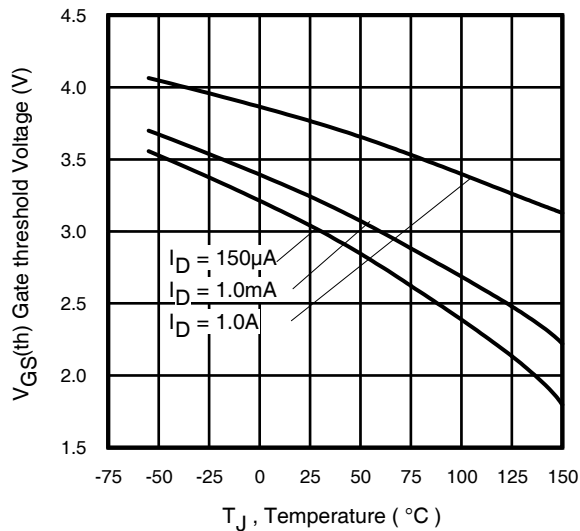


Fig 17. Threshold Voltage vs. Temperature

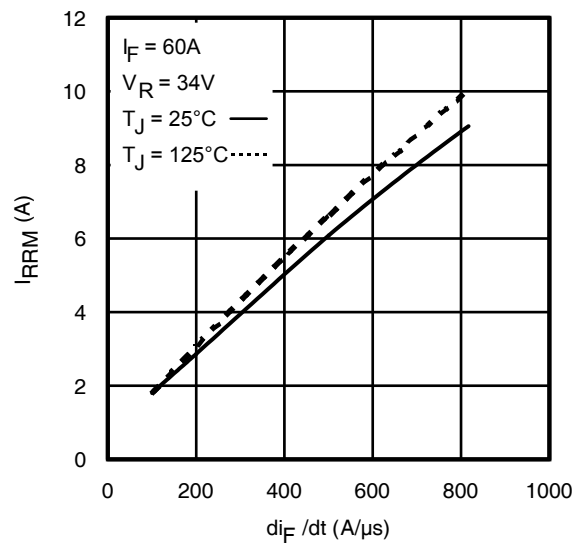


Fig 18. Typical Recovery Current vs.  $di_F/dt$

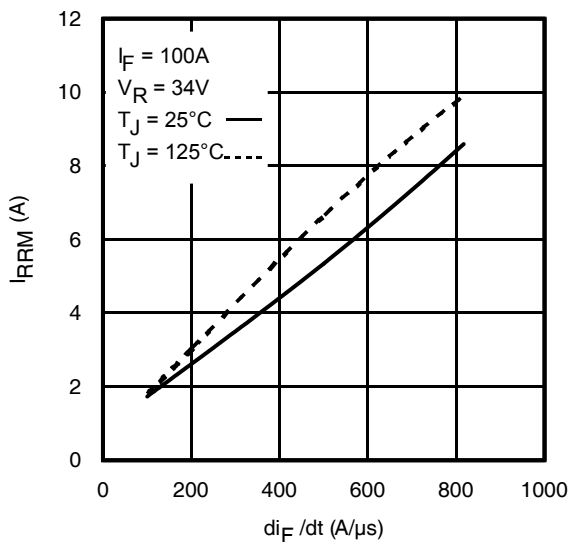


Fig 19. Typical Recovery Current vs.  $di_F/dt$

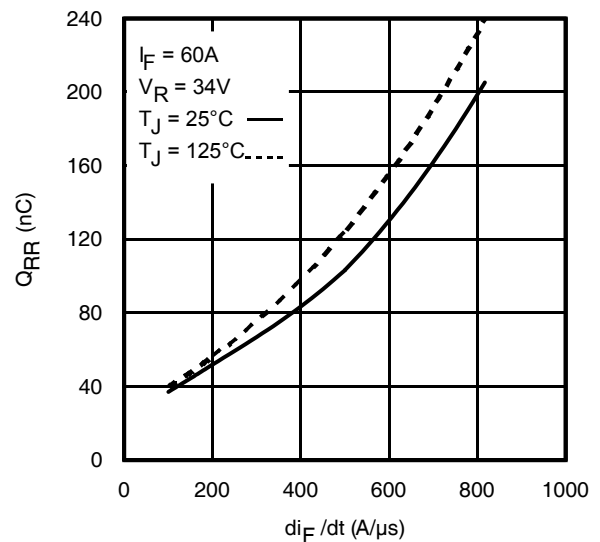


Fig 20. Typical Stored Charge vs.  $di_F/dt$

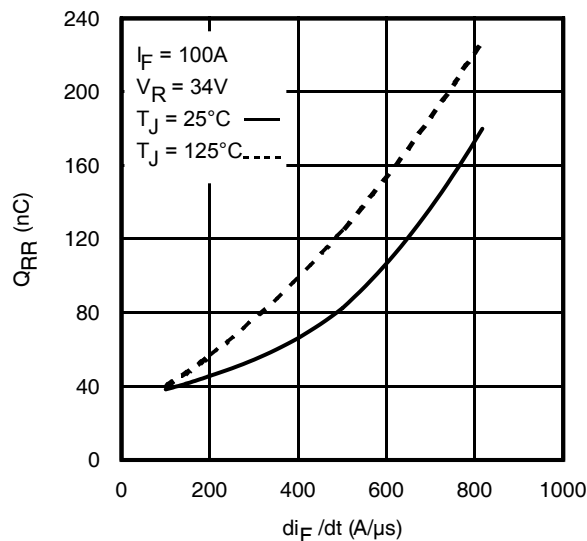
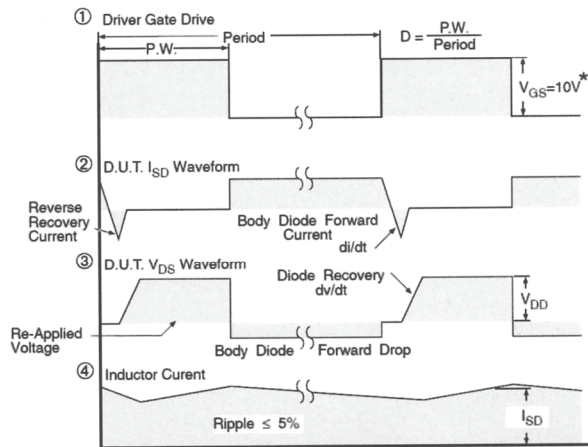
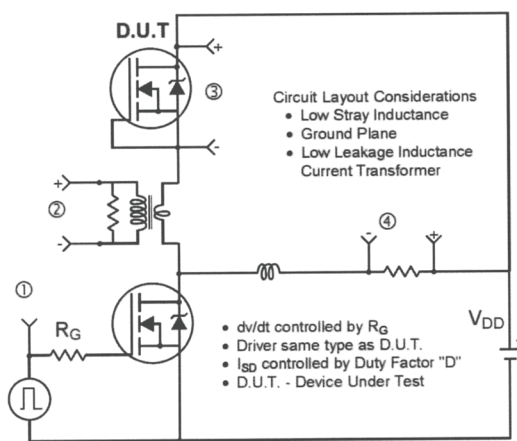
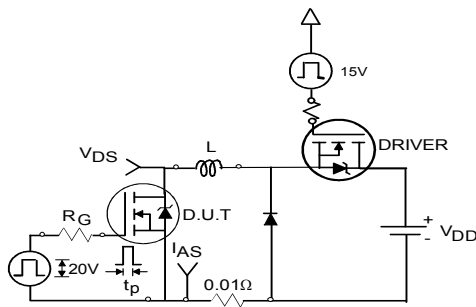


Fig 21. Typical Stored Charge vs.  $di_F/dt$

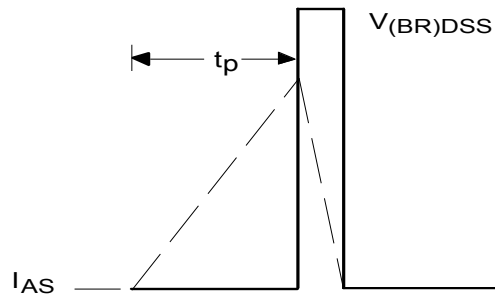


\*  $V_{GS} = 5V$  for Logic Level Devices

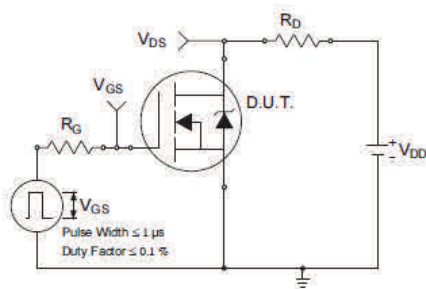
**Fig 22.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



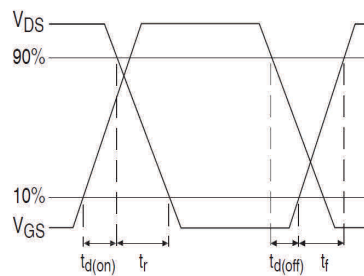
**Fig 23a.** Unclamped Inductive Test Circuit



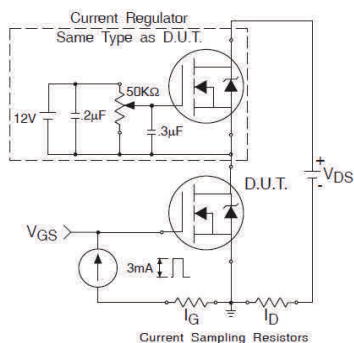
**Fig 23b.** Unclamped Inductive Waveforms



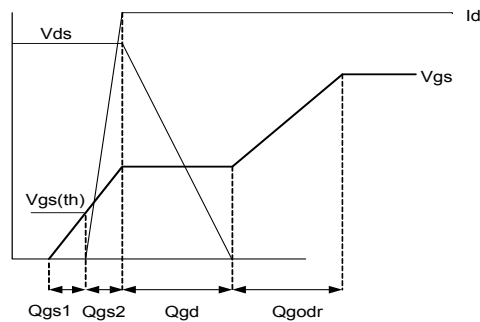
**Fig 24a.** Switching Time Test Circuit



**Fig 24b.** Switching Time Waveforms



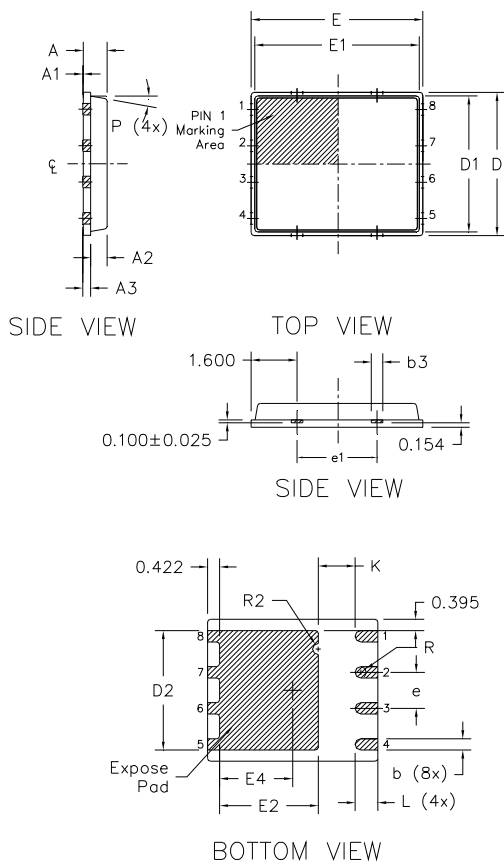
**Fig 25a.** Gate Charge Test Circuit



**Fig 25b.** Gate Charge Waveform



**PQFN 5x6 Outline "B" Package Details**



DIM SYMBOL	MILLIMETERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200 REF		0.0079 REF	
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000 BSC		0.1969 BSC	
D1	4.750 BSC		0.1870 BSC	
D2	4.100	4.300	0.1614	0.1693
E	6.000 BSC		0.2362 BSC	
E1	5.750 BSC		0.2264 BSC	
E2	3.380	3.780	0.1331	0.1488
e	1.270 REF		0.0500 REF	
e1	2.800 REF		0.1102 REF	
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200 REF		0.0079 REF	
R2	0.150	0.200	0.0059	0.0079

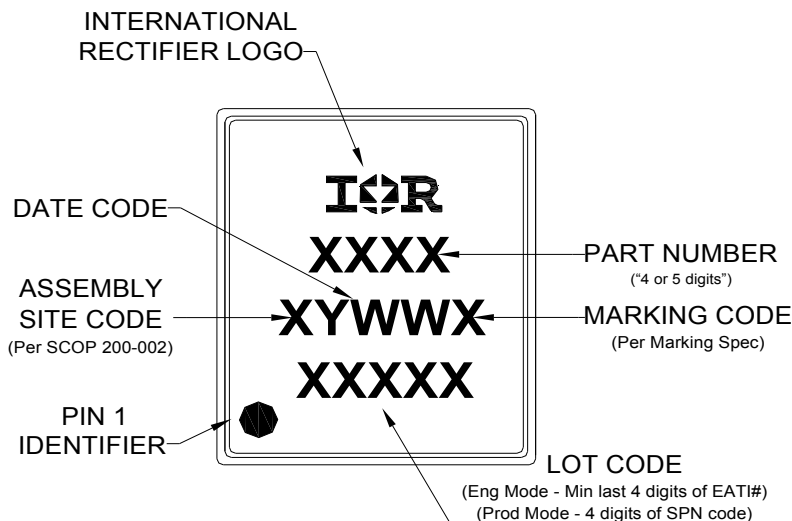
*Note:*

1. Dimensions and tolerancing confirm to ASME Y14.5M-1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

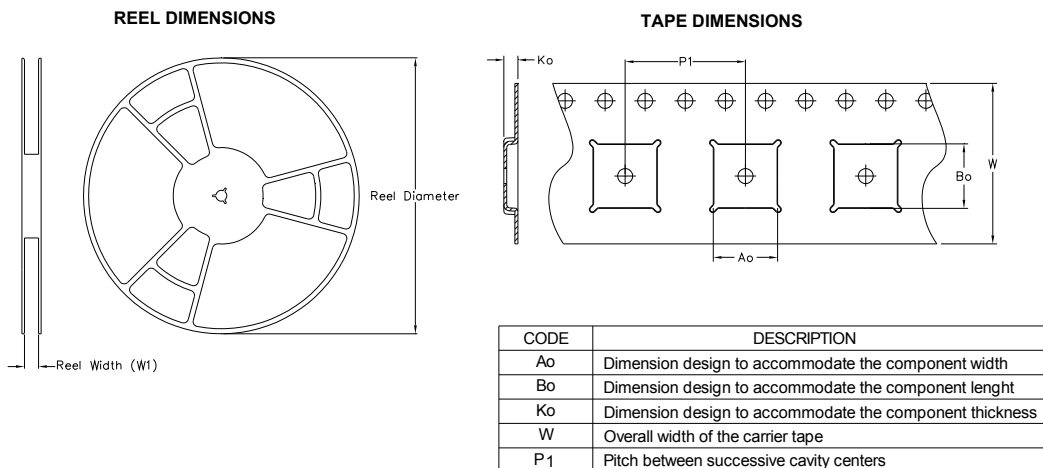
For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

**PQFN 5x6 Part Marking**

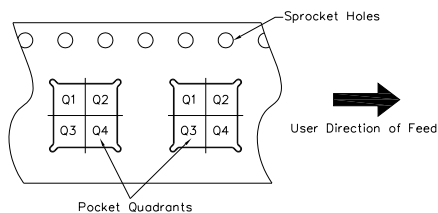


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN 5x6 Tape and Reel



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification information<sup>†</sup>**

Qualification level	Industrial <sup>††</sup>	
	(per JEDEC JESD47F <sup>††</sup> guidelines )	
Moisture Sensitivity Level	PQFN 5mmx 6mm	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
10/16/2014	<ul style="list-style-type: none"> <li>Add Pd at tc=25C on Absolute Max Rating table on page 2</li> </ul>
03/05/2015	<ul style="list-style-type: none"> <li>Updated E<sub>AS (L=1mH)</sub> = 431mJ on page 2</li> <li>Updated note 8 “Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 1mH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 29A, V<sub>GS</sub> =10V” on page 2</li> </ul>
3/19/2015	<ul style="list-style-type: none"> <li>Updated package outline on page 9.</li> </ul>

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