±15kV ESD Protected, +3V to +5.5V, 1µA, 250kbps, RS-232 Transmitters/Receivers

ICL3221E, ICL3222E, ICL3223E, ICL3232E, ICL3241E, ICL3243E

The Intersil ICL32xxE devices are 3.0V to 5.5V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Additionally, they provide ±15kV ESD protection (IEC61000-4-2 Air Gap and Human Body Model) on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications are PDAs, Palmtops, and notebook and laptop computers where the low operational, and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with manual and automatic power-down functions (except for the ICL3232E), reduce the standby supply current to a 1µA trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions. This family is fully compatible with 3.3V-only systems, mixed 3.3V and 5.0V systems, and 5.0V-only systems.

The ICL324XE are 3-driver, 5-receiver devices that provide a complete serial port suitable for laptop or notebook computers. Both devices also include noninverting always-active receivers for "wake-up" capability.

The **ICL3221E, ICL3223E and ICL3243E,** feature an ***automatic power-down*** function which powers down the on-chip power-supply and driver circuits. This occurs when an attached peripheral device is shut off or the RS-232 cable is removed, conserving system power automatically without changes to the hardware or operating system. These devices power up again when a valid RS-232 voltage is applied to any receiver input.

Table 1 summarizes the features of the devices represented by this data sheet, while Application Note AN9863 summarizes the features of each device comprising the ICL32xxE 3V family.

Features

- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- Drop in Replacements for MAX3221E, MAX3222E, MAX3223E, MAX3232E, MAX3241E, MAX3243E, SP3243E
- ICL3221E is a Low Power, Pin Compatible Upgrade for 5V MAX221E
- ICL3222E is a Low Power, Pin Compatible Upgrade for 5V MAX242E, and SP312E
- ICL3232E is a Low Power Upgrade for HIN232E, ICL232 and Pin Compatible Competitor Devices
- RS-232 Compatible with V_{CC} = 2.7V
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- Latch-Up Free
- On-Chip Voltage Converters Require Only Four External 0.1µF Capacitors
- Manual and Automatic Power-Down Features
- Guaranteed Mouse Driveability (ICL324xE Only)
- Receiver Hysteresis For Improved Noise Immunity
- Guaranteed Minimum Data Rate. 250kbps
- Wide Power Supply Range . . . . Single +3V to +5.5V
- Low Supply Current in Power-Down State 1µA
- Pb-Free Available (RoHS Compliant)

Applications

- Any System Requiring RS-232 Communication Ports
  - Battery Powered, Hand-Held, and Portable Equipment
  - Laptop Computers, Notebooks, Palmtops
  - Modems, Printers and other Peripherals
  - Digital Cameras
  - Cellular/Mobile Phones

Related Literature

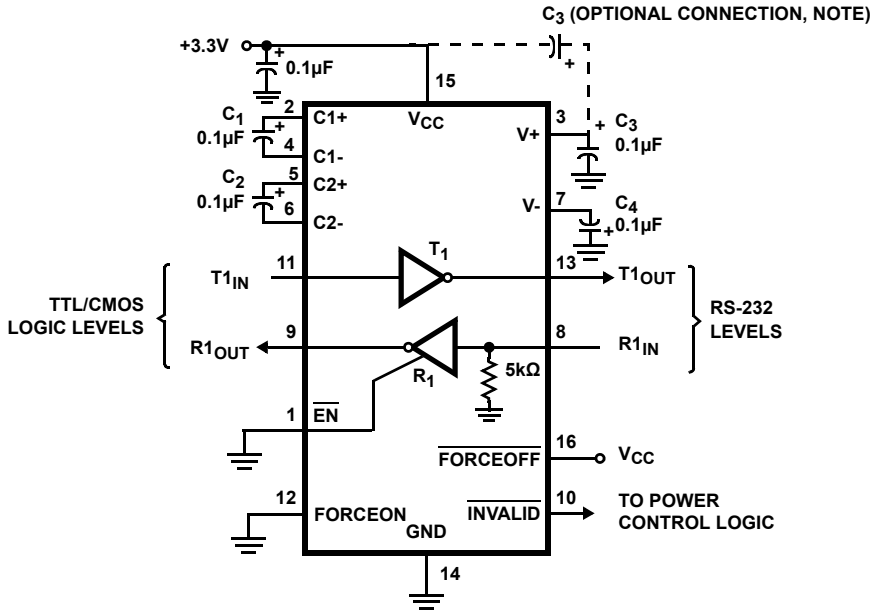
- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NUMBER OF Tx	NUMBER OF Rx	NUMBER OF MONITOR RECEIVERS (R_{OUTB})	DATA RATE (kbps)	RECEIVER ENABLE FUNCTION?	READY OUTPUT?	MANUAL POWER-DOWN?	AUTOMATIC POWER-DOWN FUNCTION?
ICL3221E	1	1	0	250	Yes	No	Yes	Yes
ICL3222E	2	2	0	250	Yes	No	Yes	No
ICL3223E	2	2	0	250	Yes	No	Yes	Yes
ICL3232E	2	2	0	250	No	No	No	No
ICL3241E	3	5	2	250	Yes	No	Yes	No
ICL3243E	3	5	1	250	No	No	Yes	Yes

Typical Operating Circuits

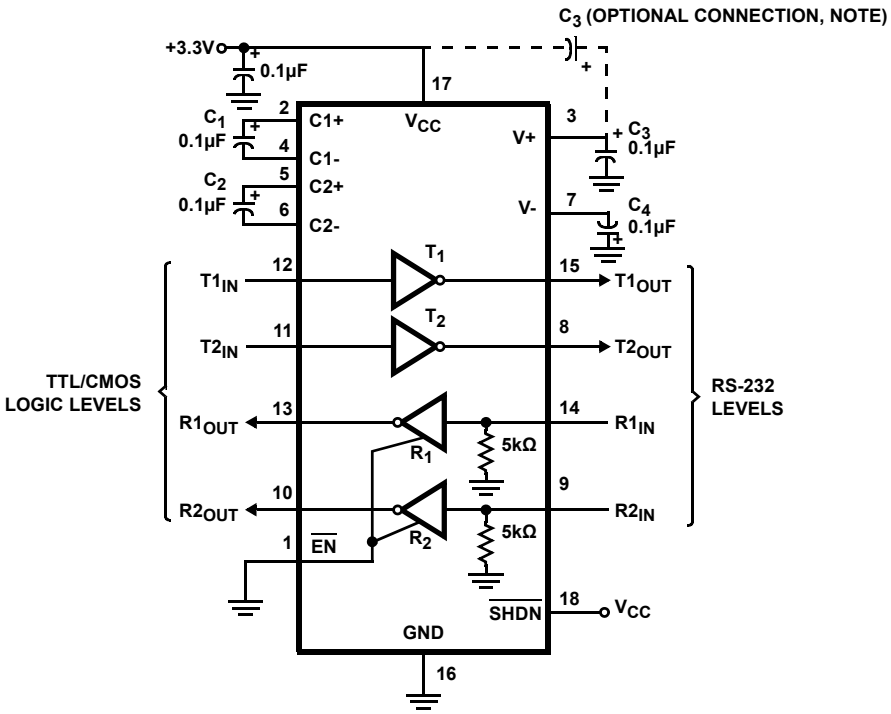
ICL3221E



NOTE: THE NEGATIVE TERMINAL OF C_3 CAN BE CONNECTED TO EITHER V_{CC} OR GND

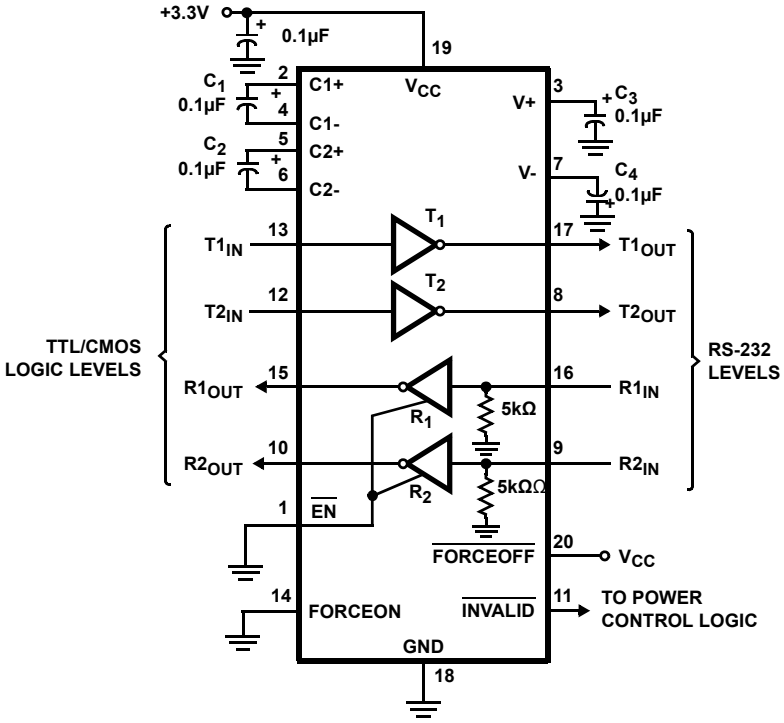
Typical Operating Circuits (Continued)

ICL3222E

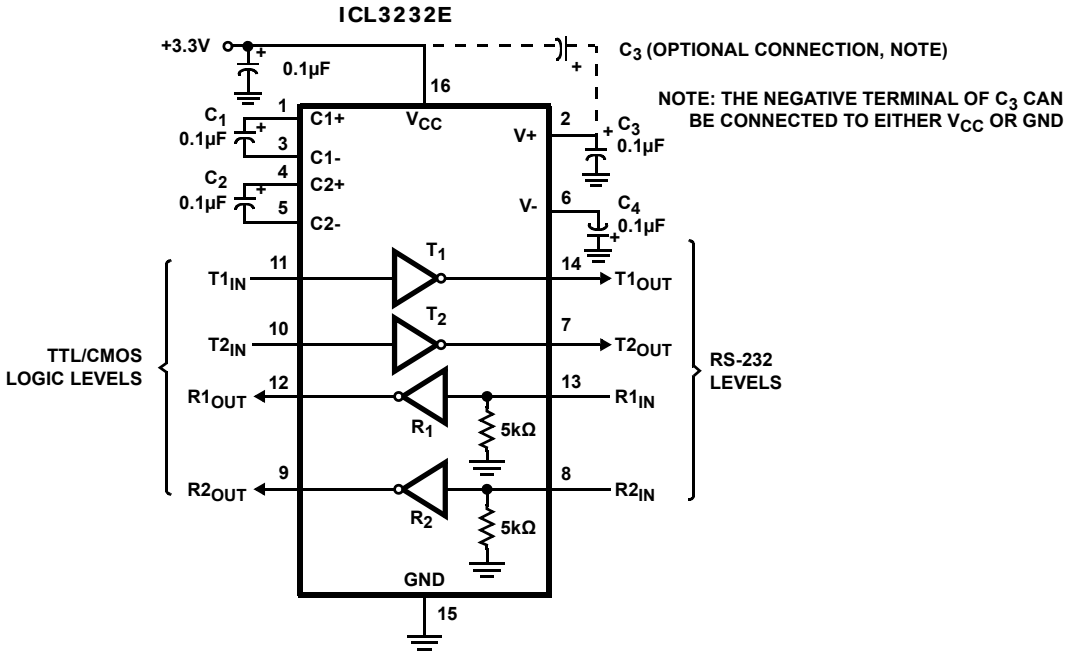


NOTE: THE NEGATIVE TERMINAL OF C_3 CAN BE CONNECTED TO EITHER V_{CC} OR GND

ICL3223E

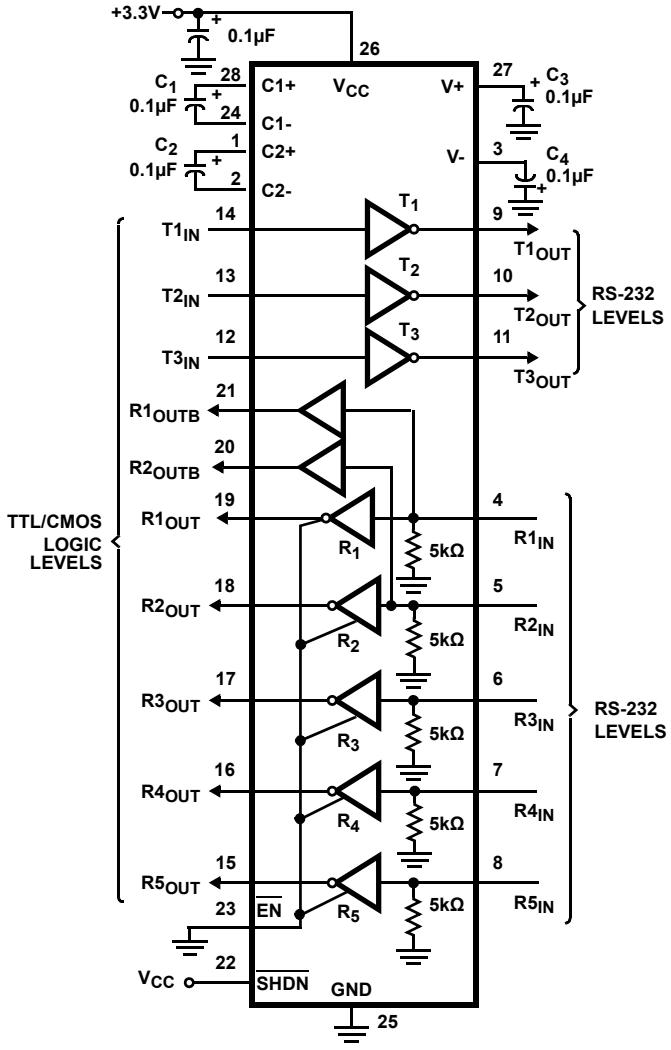


Typical Operating Circuits (Continued)

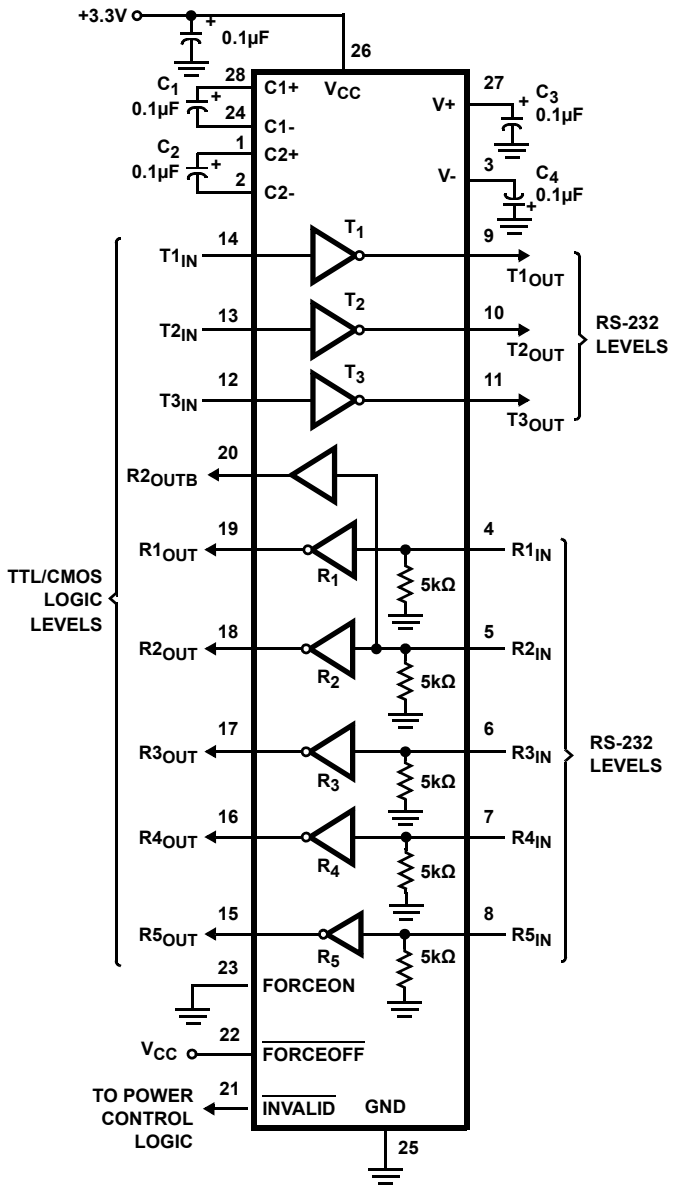


Typical Operating Circuits (Continued)

ICL3241E

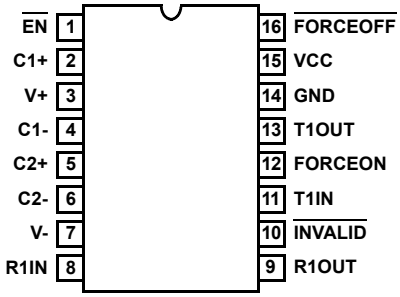


ICL3243E

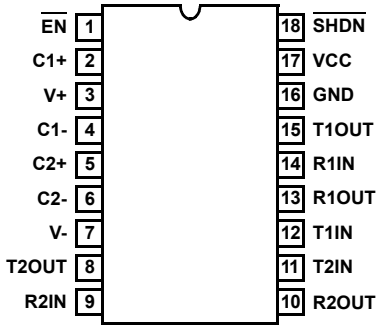


Pin Configurations

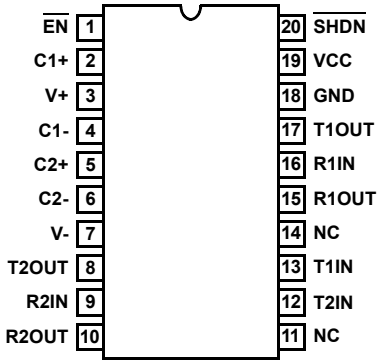
ICL3221E
(16 LD SSOP, TSSOP)
TOP VIEW



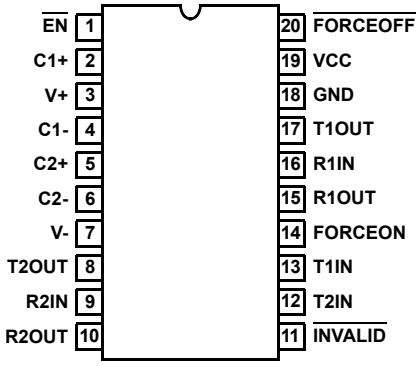
ICL3222E
(18 LD PDIP, SOIC)
TOP VIEW



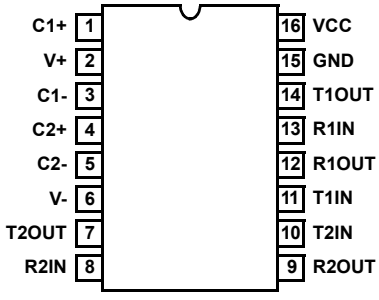
ICL3222E
(20 LD SSOP, TSSOP)
TOP VIEW



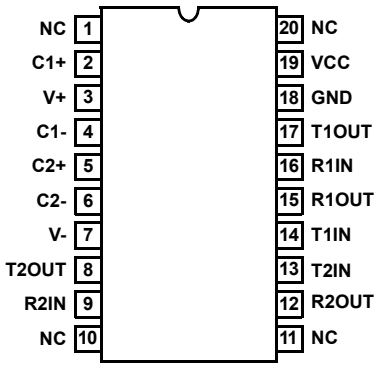
ICL3223E
(20 LD SSOP, TSSOP)
TOP VIEW



ICL3232E
(16 LD SOIC, SSOP, TSSOP-16)
TOP VIEW

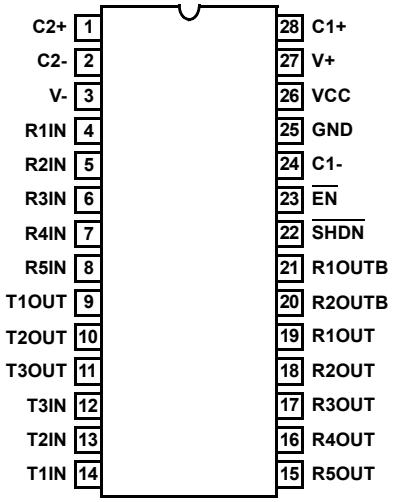


ICL3232E
(20 LD TSSOP-20)
TOP VIEW

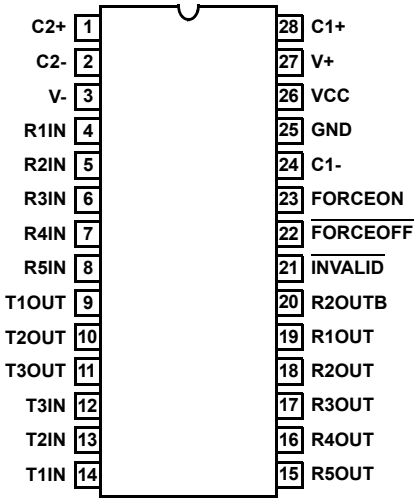


Pin Configurations (Continued)

ICL3241E
(28 LD SOIC, SSOP, TSSOP)
TOP VIEW



ICL3243E
(28 LD SOIC, SSOP, TSSOP)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
VCC	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
TIN	TTL/CMOS compatible transmitter Inputs.
TOUT	±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.
RIN	±15kV ESD Protected, RS-232 compatible receiver inputs.
ROUT	TTL/CMOS level receiver outputs.
ROUTB	TTL/CMOS level, noninverting, always enabled receiver outputs.
$\overline{\text{INVALID}}$	Active low output that indicates if no valid RS-232 levels are present on any receiver input.
$\overline{\text{EN}}$	Active low receiver enable control; doesn't disable R_{OUTB} outputs.
$\overline{\text{SHDN}}$	Active low input to shut down transmitters and on-board power supply, to place device in low power mode.
$\overline{\text{FORCEOFF}}$	Active low to shut down transmitters and on-chip power supply. This overrides any automatic circuitry and FORCEON (see Table 2).
FORCEON	Active high input to override automatic power-down circuitry thereby keeping transmitters active ($\overline{\text{FORCEOFF}}$ must be high).

Ordering Information

PART NUMBER (Note 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ICL3221ECA	ICL 3221ECA	0 to +70	16 Ld SSOP	M16.209
ICL3221ECA-T (Note 1)	ICL 3221ECA	0 to +70	16 Ld SSOP	M16.209
ICL3221ECAZ (Note 2)	ICL32 21ECAZ	0 to +70	16 Ld SSOP (Pb-free)	M16.209
ICL3221ECAZ-T (Notes 1, 2)	ICL32 21ECAZ	0 to +70	16 Ld SSOP (Pb-free)	M16.209
ICL3221ECAZA (Note 2)	ICL32 21ECAZ	0 to +70	16 Ld SSOP (Pb-free)	M16.209
ICL3221ECAZA-T (Notes 1, 2)	ICL32 21ECAZ	0 to +70	16 Ld SSOP (Pb-free)	M16.209
ICL3221ECV	3221 ECV	0 to +70	16 Ld TSSOP	M16.173
ICL3221ECVZ (Note 2)	3221 ECVZ	0 to +70	16 Ld TSSOP (Pb-free)	M16.173
ICL3221ECVZ-T (Notes 1, 2)	3221 ECVZ	0 to +70	16 Ld TSSOP (Pb-free)	M16.173
ICL3221EIA	ICL 3221EIA	-40 to +85	16 Ld SSOP	M16.209
ICL3221EIA-T (Note 1)	ICL 3221EIA	-40 to +85	16 Ld SSOP	M16.209
ICL3221EIAZ (Note 2)	ICL32 21EIAZ	-40 to +85	16 Ld SSOP (Pb-free)	M16.209
ICL3221EIAZ-T (Notes 1, 2)	ICL32 21EIAZ	-40 to +85	16 Ld SSOP (Pb-free)	M16.209
ICL3221EIVZ (Note 2)	3221 EIVZ	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173
ICL3221EIVZ-T (Notes 1, 2)	3221 EIVZ	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173
ICL3222ECA-T (Note 1)	ICL 3222ECA	0 to +70	20 Ld SSOP	M20.209
ICL3222ECAZ (Note 2)	ICL32 22ECAZ	0 to +70	20 Ld SSOP (Pb-free)	M20.209
ICL3222ECAZ-T (Notes 1, 2)	ICL32 22ECAZ	0 to +70	20 Ld SSOP (Pb-free)	M20.209
ICL3222ECP	ICL3222ECP	0 to +70	18 Ld PDIP	E18.3
ICL3222ECV-T (Note 1)	ICL 3222ECV	0 to +70	20 Ld TSSOP	M20.173
ICL3222ECVZ (Note 2)	ICL32 22ECVZ	0 to +70	20 Ld TSSOP (Pb-free)	M20.173
ICL3222ECVZ-T (Notes 1, 2)	ICL32 22ECVZ	0 to +70	20 Ld TSSOP (Pb-free)	M20.173
ICL3222EIAZ (Note 2)	ICL32 22EIAZ	-40 to +85	20 Ld SSOP (Pb-free)	M20.209
ICL3222EIAZ-T (Notes 1, 2)	ICL32 22EIAZ	-40 to +85	20 Ld SSOP (Pb-free)	M20.209
ICL3222EIB	ICL3222EIB	-40 to +85	18 Ld SOIC	M18.3
ICL3222EIB-T (Note 1)	ICL3222EIB	-40 to +85	18 Ld SOIC	M18.3
ICL3222EIBZ (Note 2)	3222EIBZ	-40 to +85	18 Ld SOIC (Pb-free)	M18.3
ICL3222EIBZ-T (Notes 1, 2)	3222EIBZ	-40 to +85	18 Ld SOIC (Pb-free)	M18.3
ICL3222EIV	ICL 3222EIV	-40 to +85	20 Ld TSSOP	M20.173
ICL3222EIV-T (Note 1)	ICL 3222EIV	-40 to +85	20 Ld TSSOP	M20.173
ICL3222EIVZ (Note 2)	ICL32 22EIVZ	-40 to +85	20 Ld TSSOP (Pb-free)	M20.173
ICL3222EIVZ-T (Notes 1, 2)	ICL32 22EIVZ	-40 to +85	20 Ld TSSOP (Pb-free)	M20.173
ICL3223ECA	ICL 3223ECA	0 to +70	20 Ld SSOP	M20.209
ICL3223ECA-T (Note 1)	ICL 3223ECA	0 to +70	20 Ld SSOP	M20.209
ICL3223ECAZ (Note 2)	ICL32 23ECAZ	0 to +70	20 Ld SSOP (Pb-free)	M20.209
ICL3223ECAZ-T (Notes 1, 2)	ICL32 23ECAZ	0 to +70	20 Ld SSOP (Pb-free)	M20.209
ICL3223ECV	ICL 3223ECV	0 to +70	20 Ld TSSOP	M20.173
ICL3223ECVZ (Note 2)	ICL32 23ECVZ	0 to +70	20 Ld TSSOP (Pb-free)	M20.173
ICL3223ECVZ-T (Notes 1, 2)	ICL32 23ECVZ	0 to +70	20 Ld TSSOP (Pb-free)	M20.173

Ordering Information (Continued)

PART NUMBER (Note 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ICL3223EIAZ (Note 2)	ICL32 23EIAZ	-40 to +85	20 Ld SSOP (Pb-free)	M20.209
ICL3223EIAZ-T (Notes 1, 2)	ICL32 23EIAZ	-40 to +85	20 Ld SSOP (Pb-free)	M20.209
ICL3223EIV	ICL 3223EIV	-40 to +85	20 Ld TSSOP	M20.173
ICL3223EIVZ (Note 2)	ICL32 23EIVZ	-40 to +85	20 Ld TSSOP (Pb-free)	M20.173
ICL3223EIVZ-T (Notes 1, 2)	ICL32 23EIVZ	-40 to +85	20 Ld TSSOP (Pb-free)	M20.173
ICL3232ECAZ (Note 2)	3232 ECAZ	0 to +70	16 Ld SSOP (Pb-free)	M16.209
ICL3232ECAZ-T (Notes 1, 2)	3232 ECAZ	0 to +70	16 Ld SSOP (Pb-free)	M16.209
ICL3232ECBZ (Note 2)	3232ECBZ	0 to +70	16 Ld SOIC (Pb-free)	M16.3
ICL3232ECBZ-T (Notes 1, 2)	3232ECBZ	0 to +70	16 Ld SOIC (Pb-free)	M16.3
ICL3232ECBNZ (Note 2)	3232ECBNZ	0 to +70	16 Ld SOIC (Pb-free)	M16.15
ICL3232ECBNZ-T (Notes 1, 2)	3232ECBNZ	0 to +70	16 Ld SOIC (Pb-free)	M16.15
ICL3232ECV-16Z (Note 2)	3232E CV-16Z	0 to +70	16 Ld TSSOP (Pb-free)	M16.173
ICL3232ECV-16Z-T (Notes 1, 2)	3232E CV-16Z	0 to +70	16 Ld TSSOP (Pb-free)	M16.173
ICL3232ECV-20Z (Note 2)	ICL3232 ECV-20Z	0 to +70	20 Ld TSSOP (Pb-free)	M20.173
ICL3232ECV-20Z-T (Notes 1, 2)	ICL3232 ECV-20Z	0 to +70	20 Ld TSSOP (Pb-free)	M20.173
ICL3232EFV-16Z (Note 2)	3232E FV-16Z	-40 to +125	16 Ld TSSOP (Pb-free)	M16.173
ICL3232EFV-16Z-T (Notes 1, 2)	3232E FV-16Z	-40 to +125	16 Ld TSSOP (Pb-free)	M16.173
ICL3232EIAZ (Note 2)	3232 EIAZ	-40 to +85	16 Ld SSOP (Pb-free)	M16.209
ICL3232EIAZ-T (Notes 1, 2)	3232 EIAZ	-40 to +85	16 Ld SSOP (Pb-free)	M16.209
ICL3232EIBZ (Note 2)	3232EIBZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.3
ICL3232EIBZ-T (Notes 1, 2)	3232EIBZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.3
ICL3232EIBNZ (Note 2)	3232EIBNZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
ICL3232EIBNZ-T (Notes 1, 2)	3232EIBNZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
ICL3232EIV-16Z (Note 2)	3232E IV-16Z	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173
ICL3232EIV-16Z-T (Notes 1, 2)	3232E IV-16Z	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173
ICL3232EIV-20Z (Note 2)	ICL3232 EIV-20Z	-40 to +85	20 Ld TSSOP (Pb-free)	M20.173
ICL3232EIV-20Z-T (Notes 1, 2)	ICL3232 EIV-20Z	-40 to +85	20 Ld TSSOP (Pb-free)	M20.173
ICL3241ECAZ (Note 2)	ICL3241 ECAZ	0 to +70	28 Ld SSOP (Pb-free)	M28.209
ICL3241ECAZ-T (Notes 1, 2)	ICL3241 ECAZ	0 to +70	28 Ld SSOP (Pb-free)	M28.209
ICL3241ECBZ (Note 2) **(No longer available, recommended replacement: ICL3241EIVZ)**	ICL3241ECBZ	0 to +70	28 Ld SOIC (Pb-free)	M28.3
ICL3241ECBZ-T (Notes 1, 2) **(No longer available, recommended replacement: ICL3241EIVZ)**	ICL3241ECBZ	0 to +70	28 Ld SOIC (Pb-free)	M28.3
ICL3241ECVZ (Note 2)	ICL3241 ECVZ	0 to +70	28 Ld TSSOP (Pb-free)	M28.173
ICL3241EIAZ (Note 2)	ICL3241 EIAZ	-40 to +85	28 Ld SSOP (Pb-free)	M28.209
ICL3241EIAZ-T (Notes 1, 2)	ICL3241 EIAZ	-40 to +85	28 Ld SSOP (Pb-free)	M28.209
ICL3241EIBZ (Note 2) **(No longer available, recommended replacement: ICL3241EIVZ)**	ICL3241EIBZ	-40 to +85	28 Ld SOIC (Pb-free)	M28.3
ICL3241EIBZ-T (Notes 1, 2) **(No longer available, recommended replacement: ICL3241EIVZ)**	ICL3241EIBZ	-40 to +85	28 Ld SOIC (Pb-free)	M28.3

Ordering Information (Continued)

PART NUMBER (Note 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ICL3241EIVZ (Note 2)	ICL3241 EIVZ	-40 to +85	28 Ld TSSOP (Pb-free)	M28.173
ICL3241EIVZ-T (Notes 1, 2)	ICL3241 EIVZ	-40 to +85	28 Ld TSSOP (Pb-free)	M28.173
ICL3243ECAZ (Note 2)	ICL32 43ECAZ	0 to +70	28 Ld SSOP (Pb-free)	M28.209
ICL3243ECAZ-T (Notes 1, 2)	ICL32 43ECAZ	0 to +70	28 Ld SSOP (Pb-free)	M28.209
ICL3243ECBZ (Note 2)	ICL3243ECBZ	0 to +70	28 Ld SOIC (Pb-free)	M28.3
ICL3243ECBZ-T (Notes 1, 2)	ICL3243ECBZ	0 to +70	28 Ld SOIC (Pb-free)	M28.3
ICL3243ECVZ (Note 2)	ICL3243 ECVZ	0 to +70	28 Ld TSSOP (Pb-free)	M28.173
ICL3243ECVZ-T (Notes 1, 2)	ICL3243 ECVZ	0 to +70	28 Ld TSSOP (Pb-free)	M28.173
ICL3243EIAZ (Note 2)	ICL32 43EIAZ	-40 to +85	28 Ld SSOP (Pb-free)	M28.209
ICL3243EIAZ-T (Notes 1, 2)	ICL32 43EIAZ	-40 to +85	28 Ld SSOP (Pb-free)	M28.209
ICL3243EIVZ (Note 2)	ICL3243 EIVZ	-40 to +85	28 Ld TSSOP (Pb-free)	M28.173
ICL3243EIVZ-T (Notes 1, 2)	ICL3243 EIVZ	-40 to +85	28 Ld TSSOP (Pb-free)	M28.173

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ICL3221E, ICL3222E, ICL3223E, ICL3232E, ICL3241E, ICL3243E. For more information on MSL please see techbrief TB363.

Table of Contents

Absolute Maximum Ratings

V_{CC} to GND . . . . . -0.3V to 6V
V+ to GND . . . . . -0.3V to 7V
V- to GND . . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
T_{IN}, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$, $\overline{SHDN}$ . . . . . -0.3V to 6V
R_{IN} . . . . . ±25V
Output Voltages
T_{OUT} . . . . . ±13.2V
R_{OUT}, $\overline{INVALID}$ . . . . . -0.3V to V_{CC} +0.3V
Short Circuit Duration
T_{OUT} . . . . . Continuous
ESD Rating . . . . . See Specification Table

Recommended Operating Conditions

Temperature Range
ICL32xxECX . . . . . 0°C to +70°C
ICL32xxEFX . . . . . -40°C to +125°C
ICL32xxEIX. . . . . -40°C to +85°C
Supply Voltage (V_{CC}) . . . . . 3.3V or 5V
Rx Input Voltage . . . . . -15V to +15V

Thermal Information

Thermal Resistance (Typical, Note 4)	Θ_{JA} (°C/W)
18 Ld PDIP Package*	80
16 Ld Wide SOIC Package	100
16 Ld Narrow SOIC Package	115
18 Ld SOIC Package	75
28 Ld SOIC Package	75
16 Ld SSOP Package	135
20 Ld SSOP Package	122
16 Ld TSSOP Package	145
20 Ld TSSOP Package	140
28 Ld SSOP and TSSOP Packages	100

Maximum Junction Temperature (Plastic Package) . +150°C
Maximum Storage Temperature Range . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range.**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
DC CHARACTERISTICS							
Supply Current, Automatic Power-Down	All R_{IN} Open, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC} (ICL3221E, ICL3223E, ICL3243E Only)		25	-	1.0	10	µA
Supply Current, Power-Down	$\overline{FORCEOFF}$ = $\overline{SHDN}$ = GND (Except ICL3232E)		25	-	1.0	10	µA
Supply Current, Automatic Power-Down Disabled	All Outputs Unloaded, FORCEON = $\overline{FORCEOFF}$ = $\overline{SHDN}$ = V_{CC}	V_{CC} = 3.0V, ICL3241, ICL3243	25	-	0.3	1.0	mA
		V_{CC} = 3.0V, ICL3223	25	-	0.7	3.0	mA
		V_{CC} = 3.15V, ICL3221, ICL3222, ICL3223, ICL3232	25	-	0.3	1.0	mA
LOGIC AND TRANSMITTER INPUTS AND RECEIVER OUTPUTS							
Input Logic Threshold Low	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$		Full	-	-	**0.8**	V
Input Logic Threshold High	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$	V_{CC} = 3.3V	Full	**2.0**	-	-	V
		V_{CC} = 5.0V	Full	**2.4**	-	-	V
Input Leakage Current	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$	All but ICL3232EF	Full	-	±0.01	**±1.0**	µA
		ICL3232EF	Full	-	±0.01	**±10**	µA
Output Leakage Current (Except ICL3232E)	$\overline{FORCEOFF}$ = GND or $\overline{EN}$ = V_{CC}		Full	-	±0.05	**±10**	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	**0.4**	V
Output Voltage High	I_{OUT} = -1.0mA	All but ICL3232EF	Full	**V_{CC} - 0.6**	V_{CC} - 0.1	-	V
		ICL3232EF	Full	**V_{CC} - 0.9**	V_{CC} - 0.1	-	V

Electrical Specifications Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
AUTOMATIC POWER-DOWN (ICL3221E, ICL3223E, ICL3243E Only, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC})							
Receiver Input Thresholds to Enable Transmitters	ICL32xxE Powers Up (see Figure 6)		Full	**-2.7**	-	**2.7**	V
Receiver Input Thresholds to Disable Transmitters	ICL32xxE Powers Down (see Figure 6)		Full	**-0.3**	-	**0.3**	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	**0.4**	V
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1.0mA		Full	**V_{CC} - 0.6**	-	-	V
Receiver Threshold to Transmitters Enabled Delay (t_{WU})			25	-	100	-	µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High Delay (t_{INVH})			25	-	1	-	µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low Delay (t_{INVL})			25	-	30	-	µs
RECEIVER INPUTS							
Input Voltage Range			25	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		25	0.6	1.2	-	V
	V_{CC} = 5.0V		25	0.8	1.5	-	V
Input Threshold High	V_{CC} = 3.3V		25	-	1.5	2.4	V
	V_{CC} = 5.0V		25	-	1.8	2.4	V
Input Hysteresis			25	-	0.5	-	V
Input Resistance			25	3	5	7	kΩ
TRANSMITTER OUTPUTS							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	**±5.0**	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	**300**	10M	-	Ω
Output Short-Circuit Current			Full	-	±35	**±60**	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 5.5V, Automatic Power-Down or $\overline{FORCEOFF}$ = $\overline{SHDN}$ = GND		Full	-	-	**±25**	µA
MOUSE DRIVEABILITY (ICL324XE Only)							
Transmitter Output Voltage (see Figure 9)	$T1_{IN}$ = $T2_{IN}$ = GND, $T3_{IN}$ = V_{CC}, $T3_{OUT}$ Loaded with 3kΩ to GND, $T1_{OUT}$ and $T2_{OUT}$ Loaded with 2.5mA Each		Full	**±5**	-	-	V
TIMING CHARACTERISTICS							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, One Transmitter Switching		Full	**250**	500	-	kbps
Receiver Propagation Delay	Receiver Input to Receiver Output, C_L = 150pF	t_{PHL}	25	-	0.15	-	µs
		t_{PLH}	25	-	0.15	-	µs
Receiver Output Enable Time	Normal Operation (Except ICL3232E)		25	-	200	-	ns

Electrical Specifications Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Receiver Output Disable Time	Normal Operation (Except ICL3232E)		25	-	200	-	ns
Transmitter Skew	t_{PHL} to t_{PLH} (Note 5)		25	-	100	-	ns
Receiver Skew	t_{PHL} to t_{PLH}		25	-	50	-	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, Measured from 3V to -3V or -3V to 3V	C_L = 150pF to 2500pF	25	4	-	30	V/µs
		C_L = 150pF to 1000pF	25	6	-	30	V/µs
ESD PERFORMANCE							
RS-232 Pins (TOUT, RIN)	Human Body Model		25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge		25	-	±8	-	kV
	IEC61000-4-2 Air Gap Discharge		25	-	±15	-	kV
All Other Pins	Human Body Model		25	-	±2	-	kV

NOTES:

5. Transmitter skew is measured at the transmitter zero crossing points.
6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Detailed Description

ICL32xxE interface ICs operate from a single +3V to +5.5V supply, guarantee a 250kbps minimum data rate, require only four small external 0.1µF capacitors, feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: charge pump, transmitters and receivers.

Charge-Pump

Intersil's new ICL32xxE family utilizes regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. This allows these devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions at V_{CC} = 3.3V. See "Capacitor Selection" on page 18 and Table 3 on page 18 for capacitor recommendations for other operating conditions. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip ±5.5V supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

Except for the ICL3232E, all transmitter outputs disable and assume a high impedance state when the device enters the power-down mode (see Table 2). These outputs may be driven to ±12V when disabled.

All devices guarantee a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 900kbps.

Transmitter inputs float if left unconnected, and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

Receivers

All the ICL32xxE devices contain standard inverting receivers that three-state (except for the ICL3232E) via the EN or FORCEOFF control lines. Additionally, the two ICL324XE products include noninverting (monitor) receivers (denoted by the ROUTB label) that are always active, regardless of the state of any control lines. All the receivers convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 1) even if the power is off (VCC = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

The ICL3221E, ICL3222E, ICL3223E, ICL3241E inverting receivers disable only when $\overline{EN}$ is driven high. ICL3243E receivers disable during forced (manual) power-down, but not during automatic power-down (see Table 2).

ICL3241E and ICL3243E monitor receivers remain active even during manual power-down and forced receiver disable, making them extremely useful for Ring Indicator monitoring. Standard receivers driving powered down peripherals must be disabled to prevent current flow through the peripheral's protection diodes (see Figures 2 and 3). This renders them useless for wake up functions, but the corresponding monitor receiver can be dedicated to this task as shown in Figure 3.

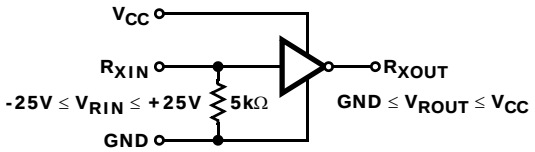


FIGURE 1. INVERTING RECEIVER CONNECTIONS

Low Power Operation

These 3V devices require a nominal supply current of 0.3mA, even at V_{CC} = 5.5V, during normal operation (not in power-down mode). This is considerably less than the 5mA to 11mA current required by comparable 5V RS-232 devices, allowing users to reduce system power simply by switching to this new family.

Pin Compatible Replacements for 5V Devices

The ICL3221E, ICL3222E, ICL3232E are pin compatible with existing 5V RS-232 transceivers - See the "Features" section on page 1 for details.

This pin compatibility coupled with the low I_{CC} and wide operating supply range, make the ICL32xxE potential lower power, higher performance drop-in replacements for existing 5V applications. As long as the ±5V RS-232 output swings are acceptable, and transmitter input pull-up resistors aren't required, the IICL32xxE should work in most 5V applications.

When replacing a device in an existing 5V application, it is acceptable to terminate C_3 to V_{CC} as shown on the "Typical Operating Circuits" on page 2. Nevertheless, terminate C_3 to GND if possible, as slightly better performance results from this configuration.

Power-Down Functionality (Except ICL3232E)

The already low current requirement drops significantly when the device enters power-down mode. In power-down, supply current drops to 1µA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND), and the transmitter outputs three-state. Inverting receiver outputs may or may not disable in power-down; refer to Table 2 for details. This micro-power mode makes these devices ideal for battery powered and portable applications.

Software Controlled (Manual) Power-Down

Most devices in the ICL32xxE family provide pins that allow the user to force the IC into the low power, standby state.

On the ICL3222E and ICL3241E, the power-down control is via a simple shutdown ($\overline{SHDN}$) pin. Driving this pin high enables normal operation, while driving it low forces the IC into its power-down state. Connect $\overline{SHDN}$ to V_{CC} if the power-down function isn't needed. Note that all the receiver outputs remain enabled during shutdown (see Table 2). For the lowest power consumption during power-down, the receivers should also be disabled by driving the $\overline{EN}$ input high (see next section, and Figures 2 and 3).

The ICL3221E, ICL3223E, and ICL3243E utilize a two pin approach where the FORCEON and $\overline{FORCEOFF}$ inputs determine the IC's mode. For always enabled operation, FORCEON and $\overline{FORCEOFF}$ are both strapped high. To switch between active and power-down modes, under logic or software control, only the $\overline{FORCEOFF}$ input need be driven. The FORCEON state isn't critical, as $\overline{FORCEOFF}$ dominates over FORCEON. Nevertheless, if strictly manual control over power-down is desired, the user must strap FORCEON high to disable the automatic power-down circuitry. ICL3243E inverting (standard) receiver outputs also disable when the device is in manual power-down, thereby eliminating the possible current path through a shutdown peripheral's input protection diode (see Figures 2 and 3).

TABLE 2. POWER-DOWN AND ENABLE LOGIC TRUTH TABLE

RS-232 SIGNAL PRESENT AT RECEIVER INPUT?	$\overline{FORCEOFF}$ OR SHDN INPUT	FORCEON INPUT	$\overline{EN}$ INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	R_{OUTB} OUTPUTS (NOTE 7)	$\overline{INVALID}$ OUTPUT	MODE OF OPERATION
ICL3222E, ICL3241E								
N/A	L	N/A	L	High-Z	Active	Active	N/A	Manual Power-Down
N/A	L	N/A	H	High-Z	High-Z	Active	N/A	Manual Power-Down with Receiver Disabled
N/A	H	N/A	L	Active	Active	Active	N/A	Normal Operation
N/A	H	N/A	H	Active	High-Z	Active	N/A	Normal Operation with Receiver Disabled

TABLE 2. POWER-DOWN AND ENABLE LOGIC TRUTH TABLE (Continued)

RS-232 SIGNAL PRESENT AT RECEIVER INPUT?	$\overline{\text{FORCEOFF}}$ OR $\overline{\text{SHDN}}$ INPUT	FORCEON INPUT	$\overline{\text{EN}}$ INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	R_{OUTB} OUTPUTS (NOTE 7)	$\overline{\text{INVALID}}$ OUTPUT	MODE OF OPERATION
ICL3221E, ICL3223E								
No	H	H	L	Active	Active	N/A	L	Normal Operation (Auto Power-Down Disabled)
No	H	H	H	Active	High-Z	N/A	L	
Yes	H	L	L	Active	Active	N/A	H	Normal Operation (Auto Power-Down Enabled)
Yes	H	L	H	Active	High-Z	N/A	H	
No	H	L	L	High-Z	Active	N/A	L	Power-Down Due to Auto Power-Down Logic
No	H	L	H	High-Z	High-Z	N/A	L	
Yes	L	X	L	High-Z	Active	N/A	H	Manual Power-Down
Yes	L	X	H	High-Z	High-Z	N/A	H	Manual Power-Down with Receiver Disabled
No	L	X	L	High-Z	Active	N/A	L	Manual Power-Down
No	L	X	H	High-Z	High-Z	N/A	L	Manual Power-Down with Receiver Disabled
ICL3243E								
No	H	H	N/A	Active	Active	Active	L	Normal Operation (Auto Power-Down Disabled)
Yes	H	L	N/A	Active	Active	Active	H	Normal Operation (Auto Power-Down Enabled)
No	H	L	N/A	High-Z	Active	Active	L	Power-Down Due to Auto Power-Down Logic
Yes	L	X	N/A	High-Z	High-Z	Active	H	Manual Power-Down
No	L	X	N/A	High-Z	High-Z	Active	L	Manual Power-Down

NOTE:

7. Applies only to the ICL3241E and ICL3243E.

The $\overline{\text{INVALID}}$ output always indicates whether or not a valid RS-232 signal is present at any of the receiver inputs (see Table 2), giving the user an easy way to determine when the interface block should power down. In the case of a disconnected interface cable where all the receiver inputs are floating (but pulled to GND by the internal receiver pull down resistors), the $\overline{\text{INVALID}}$ logic detects the invalid levels and drives the output low. The power management logic then uses this indicator to power down the interface block. Reconnecting the cable restores valid levels at the receiver inputs, $\overline{\text{INVALID}}$ switches high, and the power management logic wakes up the interface block. $\overline{\text{INVALID}}$ can also be used to indicate the DTR or RING INDICATOR signal, as long as the other receiver inputs are floating, or driven to GND (as in the case of a powered down driver). Connecting $\overline{\text{FORCEOFF}}$ and FORCEON together disables the automatic power-down feature, enabling them to function as a manual $\overline{\text{SHUTDOWN}}$ input (see Figure 4).

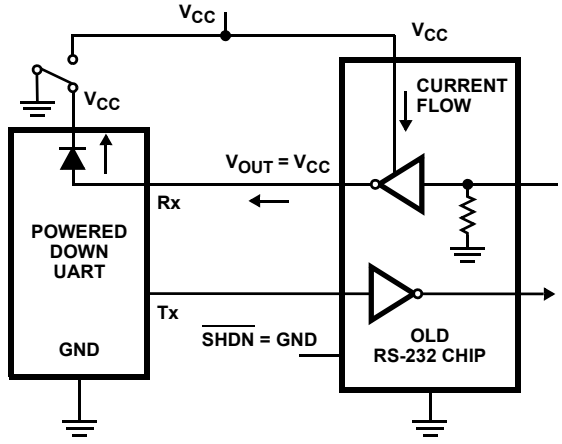


FIGURE 2. POWER DRAIN THROUGH POWERED DOWN PERIPHERAL

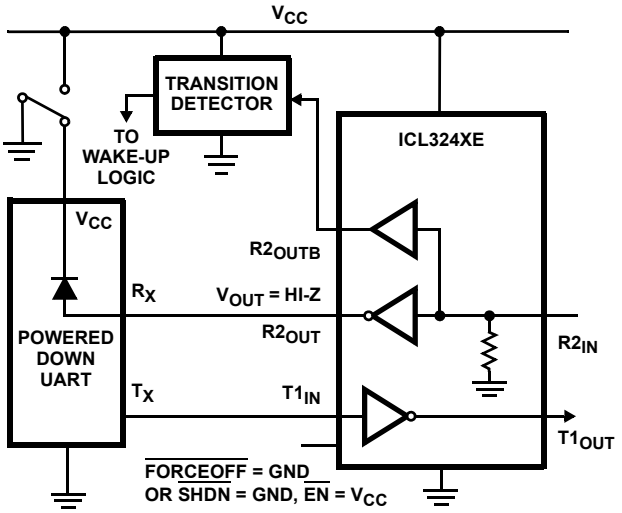


FIGURE 3. DISABLED RECEIVERS PREVENT POWER DRAIN

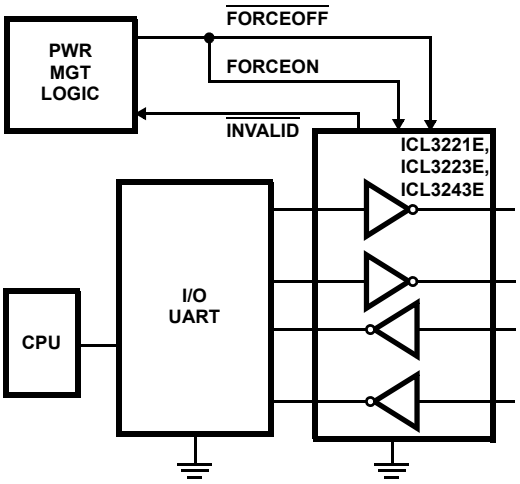


FIGURE 4. CONNECTIONS FOR MANUAL POWER-DOWN WHEN NO VALID RECEIVER SIGNALS ARE PRESENT

With any of the control schemes, the time required to exit power-down, and resume transmission is only 100µs. A mouse, or other application, may need more time to wake up from shutdown. If automatic power-down is being utilized, the RS-232 device will reenter power-down if valid receiver levels aren't reestablished within 30µs of the ICL32xxE powering up. Figure 5 illustrates a circuit that keeps the ICL32xxE from initiating automatic power-down for 100ms after powering up. This gives the slow-to-wake peripheral circuit time to reestablish valid RS-232 output levels.

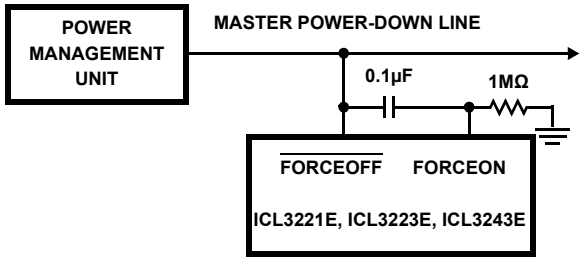


FIGURE 5. CIRCUIT TO PREVENT AUTO POWER-DOWN FOR 100ms AFTER FORCED POWER-UP

Automatic Power-Down (ICL3221E, ICL3223E, ICL3243E Only)

Even greater power savings is available by using the devices which feature an *automatic* power-down function. When no valid RS-232 voltages (see Figure 6) are sensed on any receiver input for 30µs, the charge pump and transmitters power-down, thereby reducing supply current to 1µA. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. The ICL32xxE powers back up whenever it detects a valid RS-232 voltage level on any receiver input. This automatic power-down feature provides additional system power savings without changes to the existing operating system.

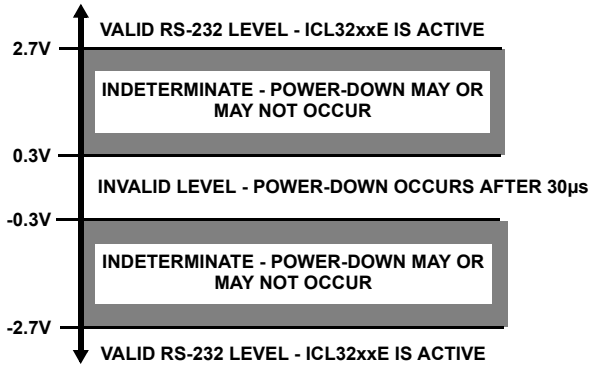


FIGURE 6. DEFINITION OF VALID RS-232 RECEIVER LEVELS

Automatic power-down operates when the FORCEON input is low, and the $\overline{\text{FORCEOFF}}$ input is high. Tying FORCEON high disables automatic power-down, but manual power-down is always available via the overriding $\overline{\text{FORCEOFF}}$ input. Table 2 summarizes the automatic power-down functionality.

Devices with the automatic power-down feature include an $\overline{\text{INVALID}}$ output signal, which switches low to indicate that invalid levels have persisted on all of the receiver inputs for more than 30µs (see Figure 7). $\overline{\text{INVALID}}$ switches high 1µs after detecting a valid RS-232 level on a receiver input. $\overline{\text{INVALID}}$ operates in all modes (forced or automatic power-down, or forced on), so it is also useful for systems employing manual power-down circuitry. When automatic power-down is utilized, $\overline{\text{INVALID}}$ = 0 indicates that the ICL32xxE is in power-down mode.

The time to recover from automatic power-down mode is typically 100µs.

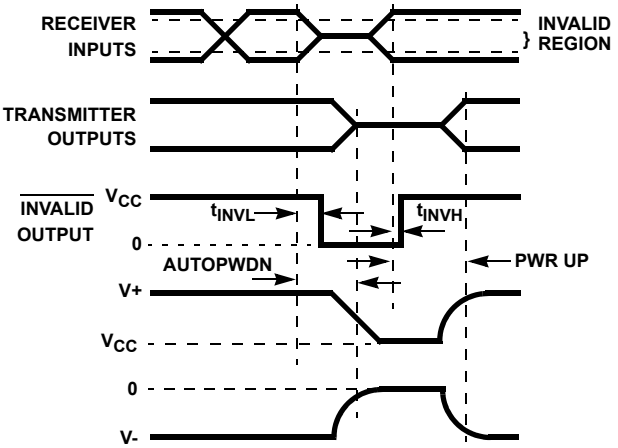


FIGURE 7. $\overline{\text{AUTOMATIC}}$ POWER-DOWN AND $\overline{\text{INVALID}}$ TIMING DIAGRAMS

Receiver ENABLE Control (ICL3221E, ICL3222E, ICL3223E, ICL3241E Only)

Several devices also feature an $\overline{\text{EN}}$ input to control the receiver outputs. Driving $\overline{\text{EN}}$ high disables all the inverting (standard) receiver outputs placing them in a high impedance state. This is useful to eliminate supply current, due to a receiver output forward biasing the protection diode, when driving the input of a powered down (V_{CC} = GND) peripheral (see Figure 2). The enable input has no effect on transmitter nor monitor (R_{OUTB}) outputs.

Capacitor Selection

The charge pumps require 0.1µF capacitors for 3.3V operation. For other supply voltages refer to Table 3 for capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C_2, C_3, and C_4 can be increased without increasing C_1's value, however, do not increase C_1 without also increasing C_2, C_3, and C_4 to maintain the proper ratios (C_1 to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

TABLE 3. REQUIRED CAPACITOR VALUES

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

Operation Down to 2.7V

ICL32xxE transmitter outputs meet RS-562 levels (±3.7V), at full data rate, with V_{CC} as low as 2.7V. RS-562 levels typically ensure interoperability with RS-232 devices.

Transmitter Outputs when Exiting Power-Down

Figure 8 shows the response of two transmitter outputs when exiting power-down mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V..

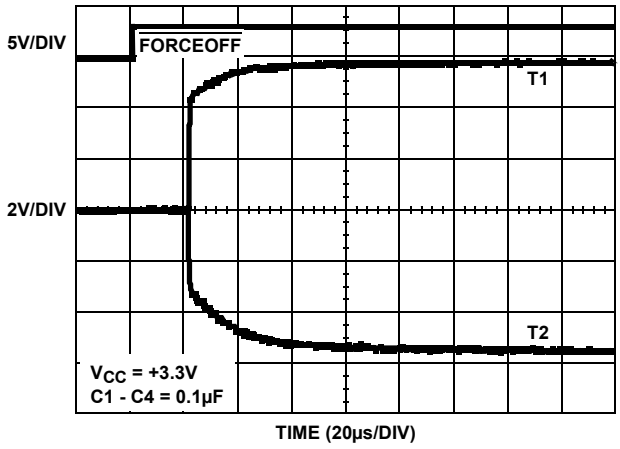


FIGURE 8. TRANSMITTER OUTPUTS WHEN EXITING POWER-DOWN

Mouse Driveability

The ICL3241E and ICL3243E have been specifically designed to power a serial mouse while operating from low voltage supplies. Figure 9 shows the transmitter

output voltages under increasing load current. The on-chip switching regulator ensures the transmitters will supply at least ±5V during worst case conditions (15mA for paralleled V+ transmitters, 7.3mA for single V- transmitter). The Automatic Power-Down feature does not work with a mouse, so $\overline{\text{FORCEOFF}}$ and FORCEON should be connected to V_{CC}.

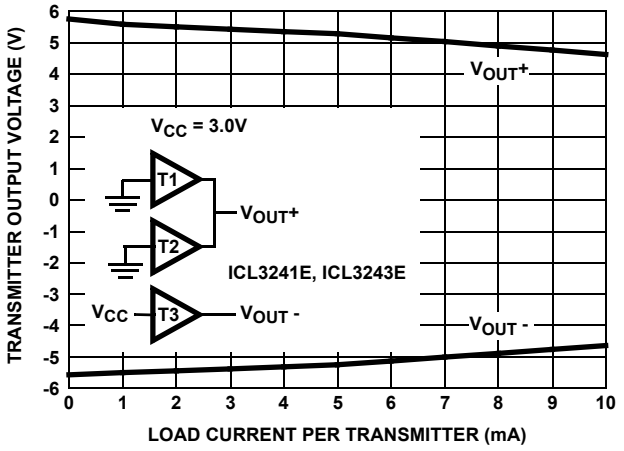


FIGURE 9. TRANSMITTER OUTPUT VOLTAGE vs LOAD CURRENT (PER TRANSMITTER, i.e., DOUBLE CURRENT AXIS FOR TOTAL V_{OUT+} CURRENT)

High Data Rates

The ICL32xxE maintain the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 10 details a transmitter loopback test circuit, and Figure 11 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 12 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

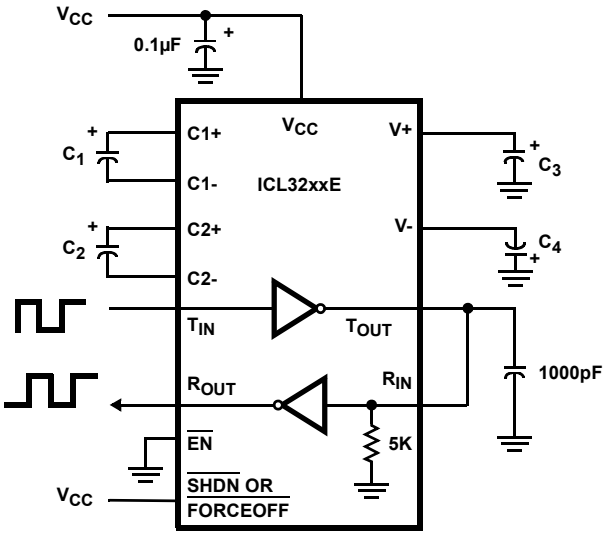


FIGURE 10. TRANSMITTER LOOPBACK TEST CIRCUIT

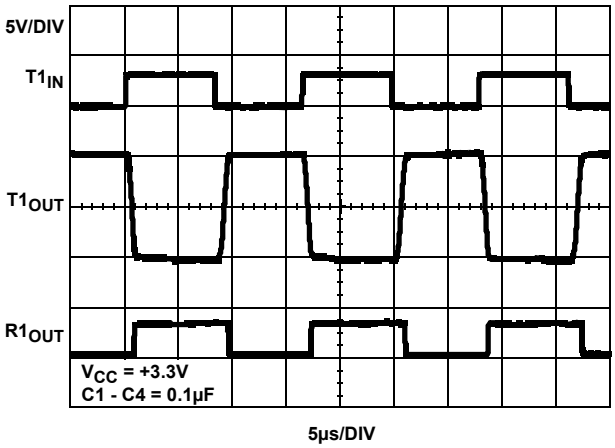


FIGURE 11. LOOPBACK TEST AT 120kbps

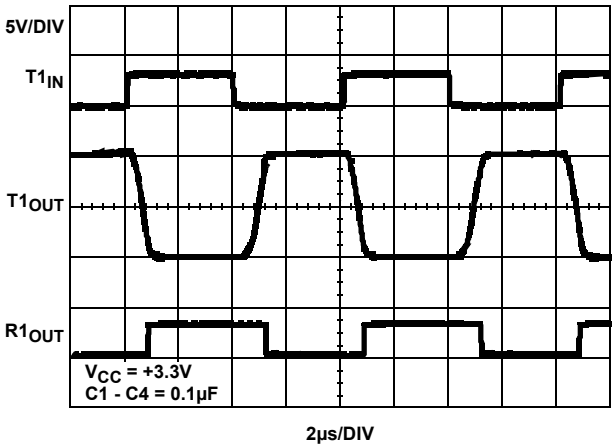


FIGURE 12. LOOPBACK TEST AT 250kbps

Interconnection with 3V and 5V Logic

The ICL32XX directly interface with 5V CMOS and TTL logic families. Nevertheless, with the ICL32XX at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can drive ICL32XX inputs, but ICL32XX outputs do not reach the minimum V_{IH} for these logic families. See Table 4 for more information.

TABLE 4. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.

TABLE 4. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES (Continued)

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ICL32XX outputs are incompatible with AC, HC, and CD4000 CMOS inputs.

±15kV ESD Protection

All pins on ICL32XX devices include ESD protection structures, but the ICL32xxE family incorporates advanced structures which allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latch-up mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330Ω limiting resistor. The HBM method determines an IC's ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C.

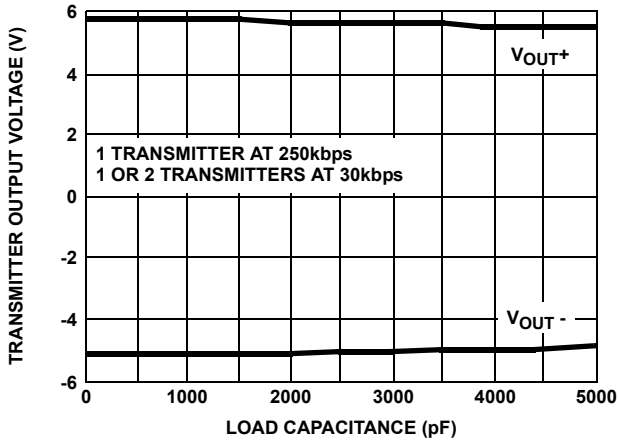


FIGURE 13. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

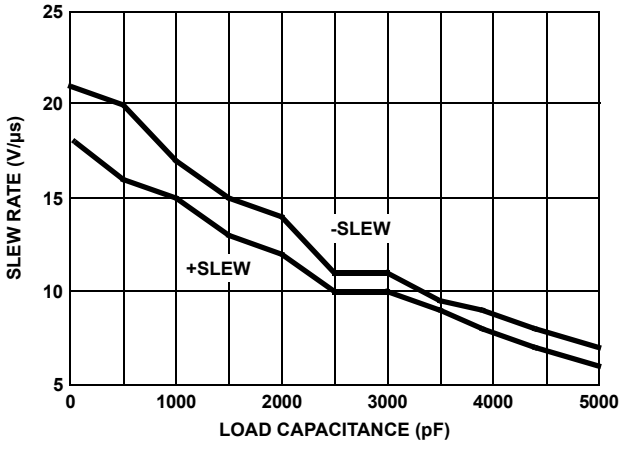


FIGURE 14. SLEW RATE vs LOAD CAPACITANCE

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C. **(Continued)**

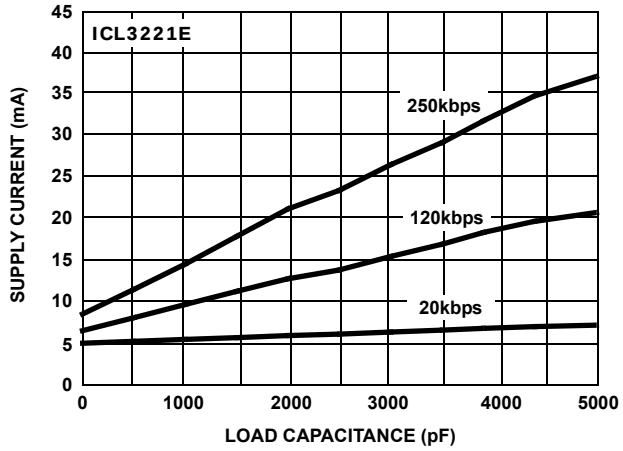


FIGURE 15. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

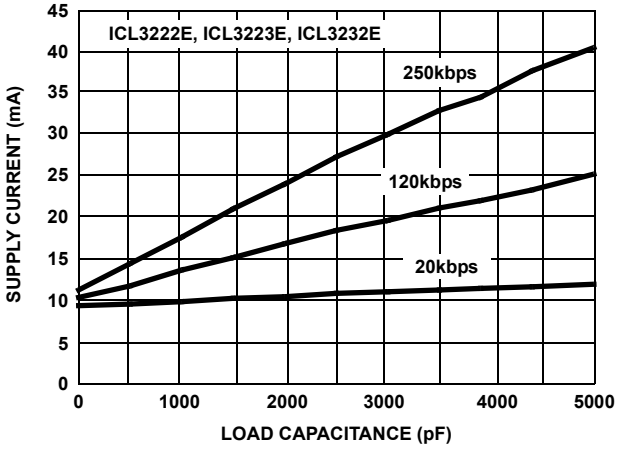


FIGURE 16. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

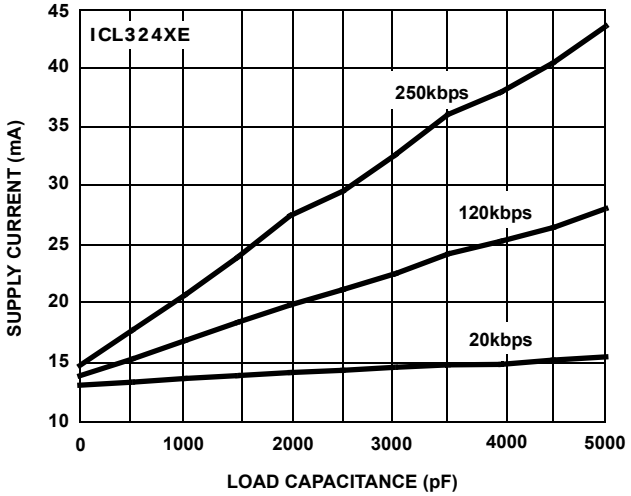


FIGURE 17. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

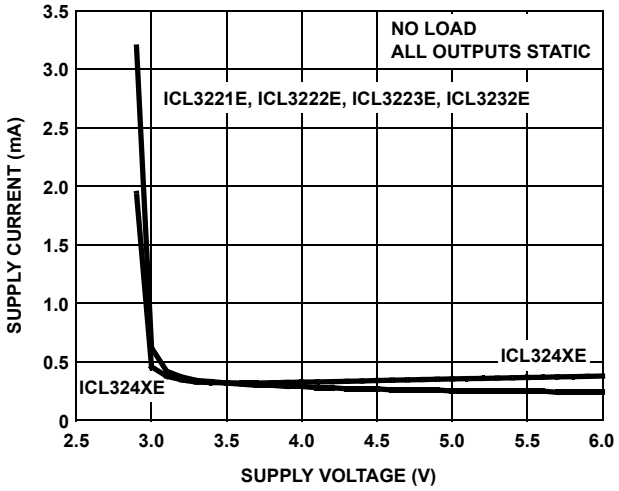


FIGURE 18. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

ICL3221E: 286
ICL3222E: 338
ICL3223E: 357
ICL3232E: 296
ICL324XE: 464

PROCESS:

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
12/9/15	FN4910.22	Updated Ordering Information table starting on page 8 Updated “Products” section to “About Intersil” POD E18.3 updated from rev 2 to rev 3. Changes since rev 2: 1) Removed the dimension chart and replaced with new standard format values for each dimension letter. 2) Updated D dimension (in side view; length of package) from 0.845(min) : 0.880(max) to 0.880(33.27)(min) : 0.920(34.65)(max) 3) Change JEDEC reference from MS-001-BC issue D to MS-001-AC issue D POD M16.173 updated from rev 1 to rev 2. Changes since rev 1: Converted to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. POD M20.173 updated from rev 1 to rev 2. Changes since rev 1: Converted to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. POD M28.173 udpated from rev 0 to rev 1. Changes since rev 1: Converted to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. POD M28.3 updated from rev 0 to rev 1. Changes since rev 1: Added land pattern
2/22/10	FN4910.21	Revision history begins with this revision. Converted to new Intersil template. Added new temp grade (F = extended industrial) to ICL3232. Updated ordering info table, Operating Conditions, and added 125°C specs for input lkg currents, and rcvr output high voltage. Pages 8-10: Removed all withdrawn devices from Ordering Information table. Pages 12-14: Added "Boldface limits apply over the operating temperature range." to common conditions of Electrical Specs table. Replaced Note 6 "Parts are 100% tested at +25°C. Full temp limits are guaranteed by bench and tester characterization." with "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested."

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

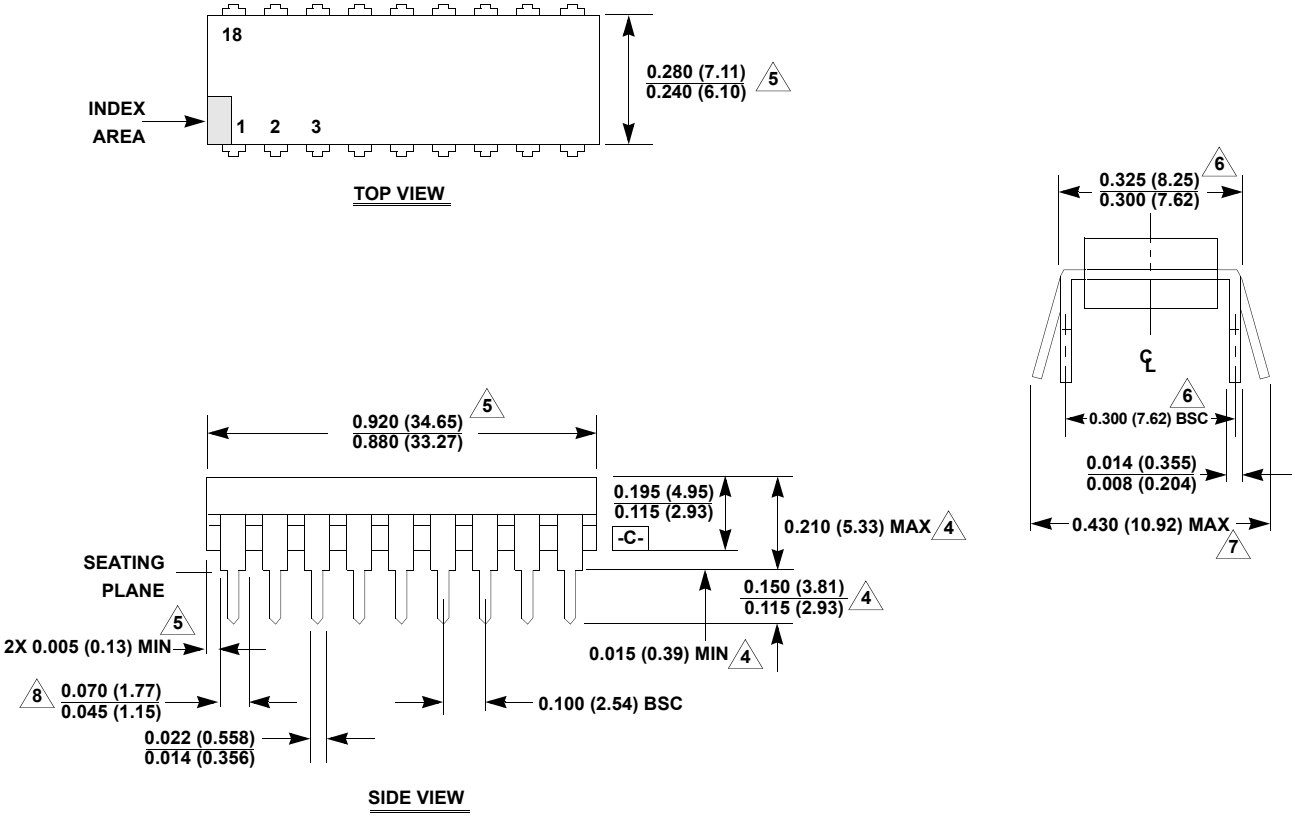
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

E18.3

18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

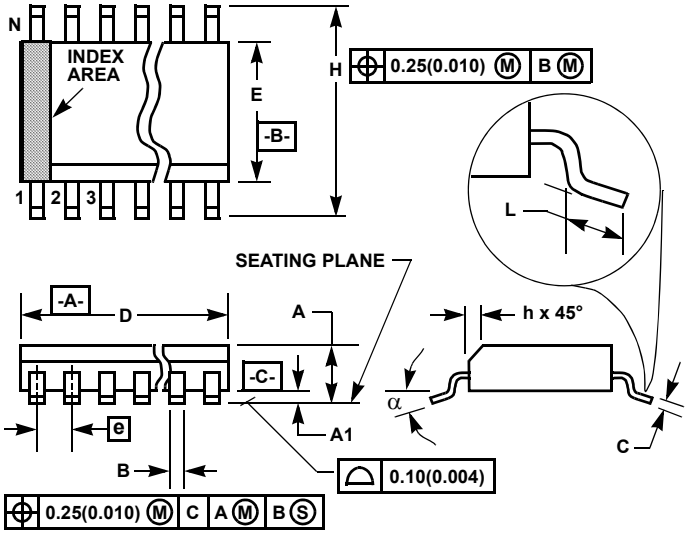
Rev. 3, 11/11



NOTES:

1. Controlling Dimensions: INCH (Metric dimensions in parentheses).
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.
5. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. Dimensions are measured with the leads constrained to be perpendicular to datum -C-.
7. Dimension measured at the lead tips with the leads unconstrained.
8. Maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. Package outline compliant to JEDEC MS-001-AC ISSUE D.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

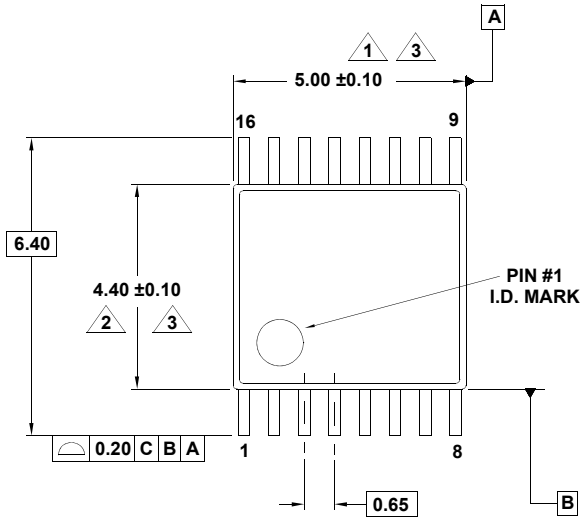
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

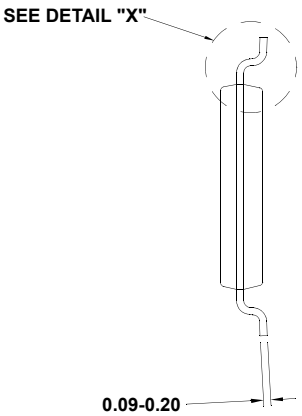
Package Outline Drawing

M16.173

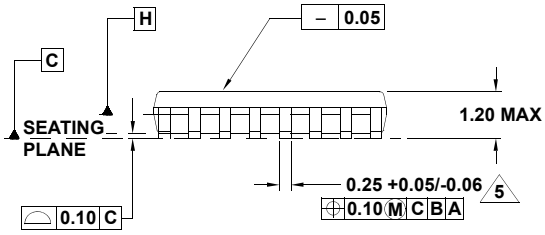
16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



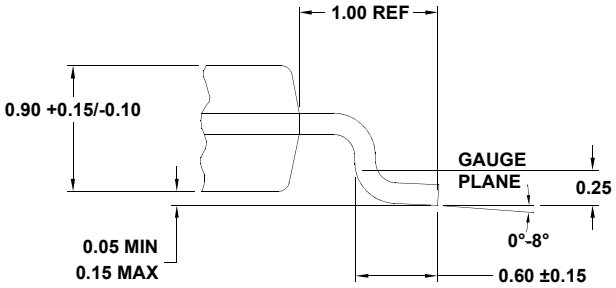
TOP VIEW



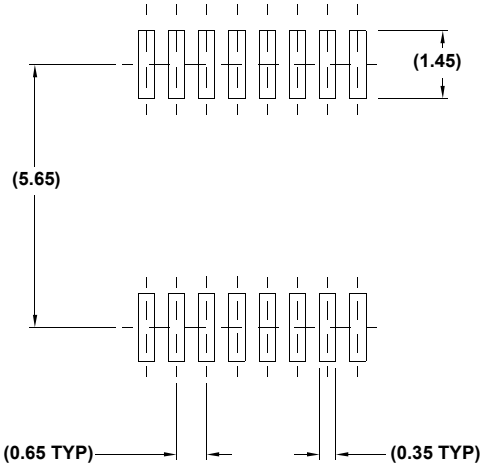
END VIEW



SIDE VIEW



DETAIL "X"

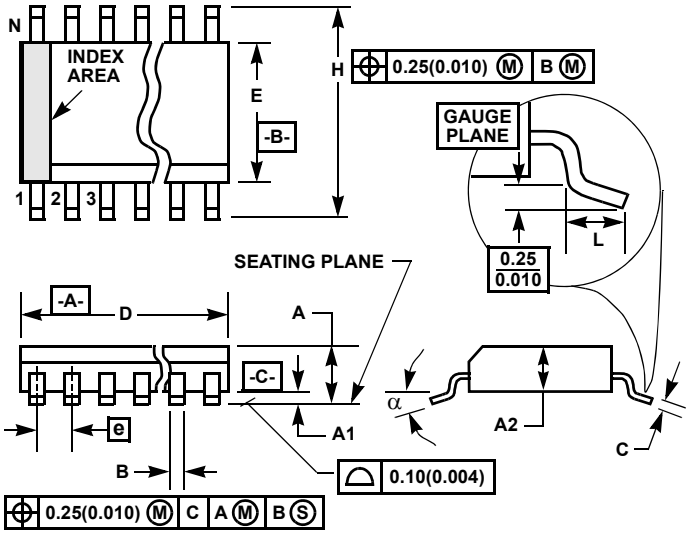


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

Small Outline Plastic Packages (SSOP)



NOTES:

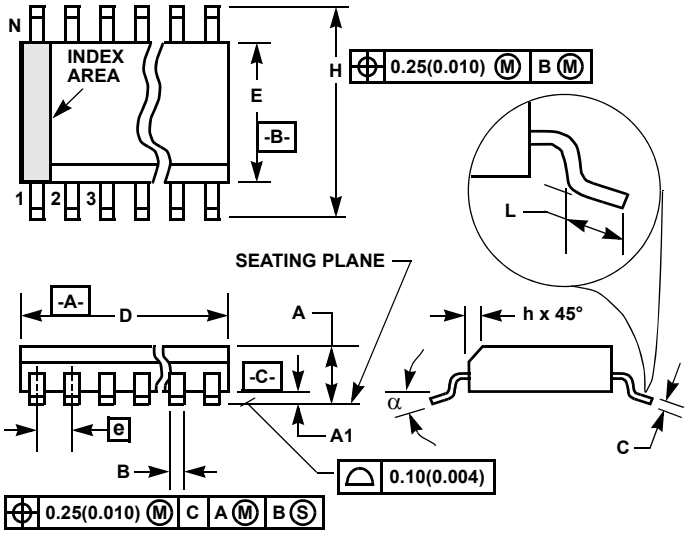
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.209 **(JEDEC MO-150-AC ISSUE B)**
16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.233	0.255	5.90	6.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 3 6/05

Small Outline Plastic Packages (SOIC)



NOTES:

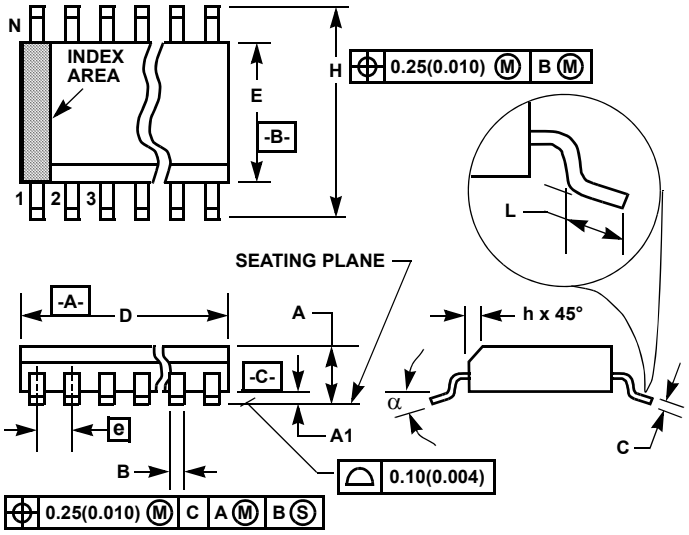
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M18.3 (JEDEC MS-013-AB ISSUE C)
18 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

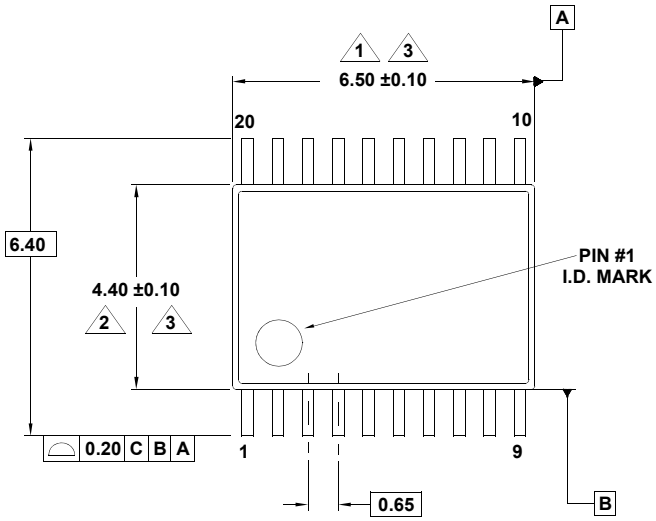
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4469	0.4625	11.35	11.75	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	18		18		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

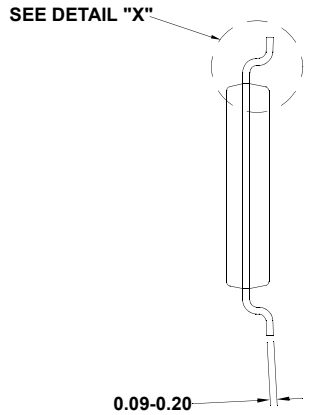
Package Outline Drawing

M20.173

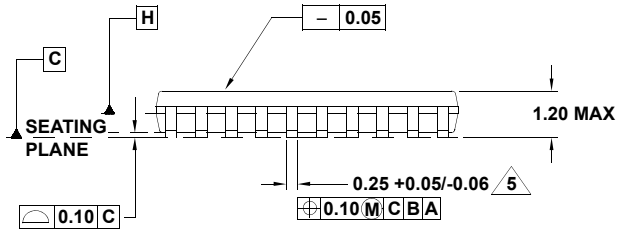
20 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



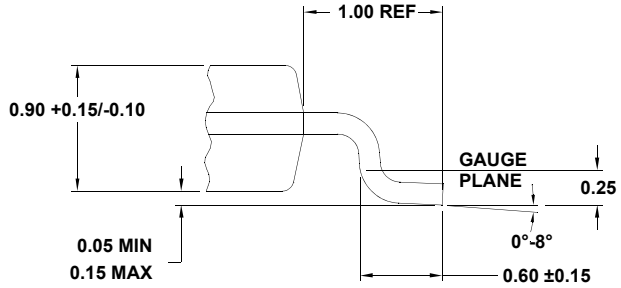
TOP VIEW



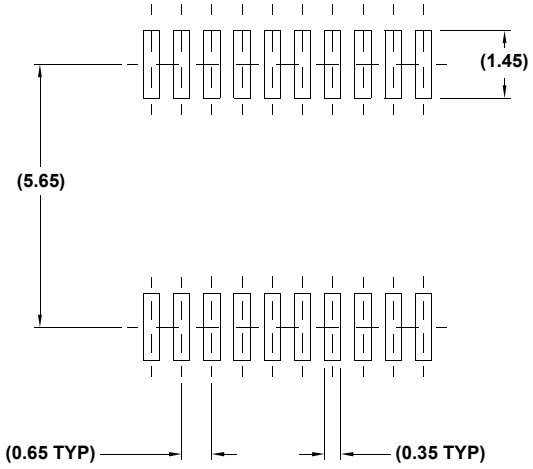
END VIEW



SIDE VIEW



DETAIL "X"

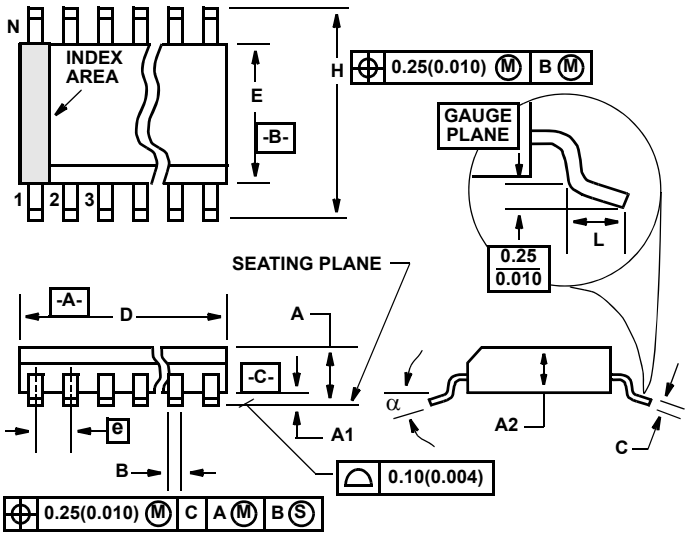


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

Shrink Small Outline Plastic Packages (SSOP)



M20.209 **(JEDEC MO-150-AE ISSUE B)**
20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.068	0.078	1.73	1.99	
A1	0.002	0.008’	0.05	0.21	
A2	0.066	0.070’	1.68	1.78	
B	0.010’	0.015	0.25	0.38	9
C	0.004	0.008	0.09	0.20’	
D	0.278	0.289	7.07	7.33	3
E	0.205	0.212	5.20’	5.38	4
e	0.026 BSC		0.65 BSC		
H	0.301	0.311	7.65	7.90’	
L	0.025	0.037	0.63	0.95	6
N	20		20		7
α	0 deg.	8 deg.	0 deg.	8 deg.	

Rev. 3 11/02

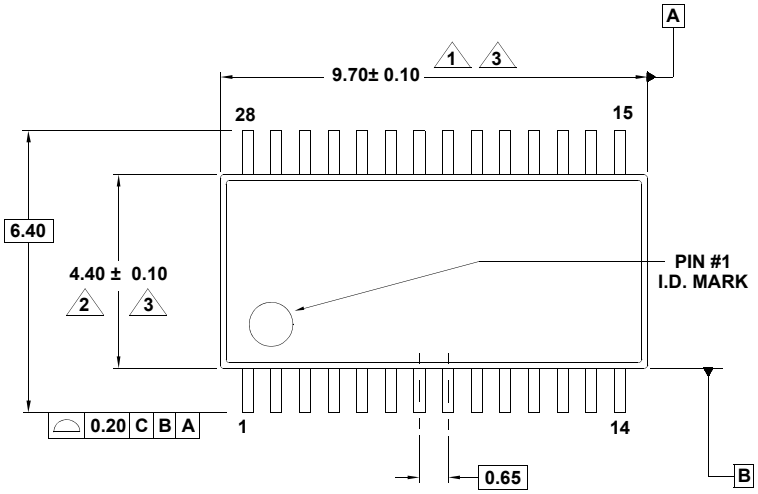
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

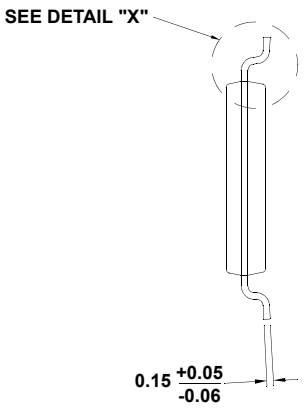
Package Outline Drawing

M28.173

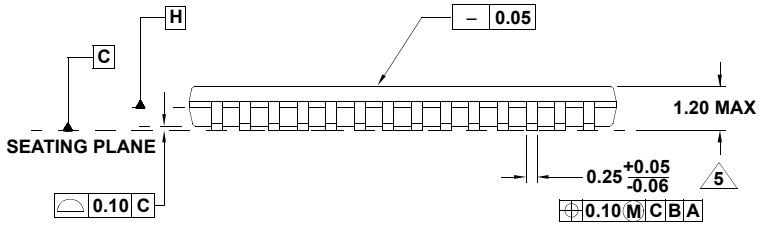
28 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 1, 5/10



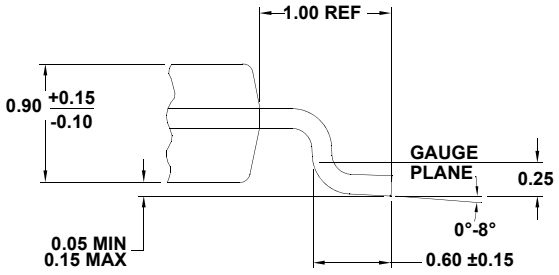
TOP VIEW



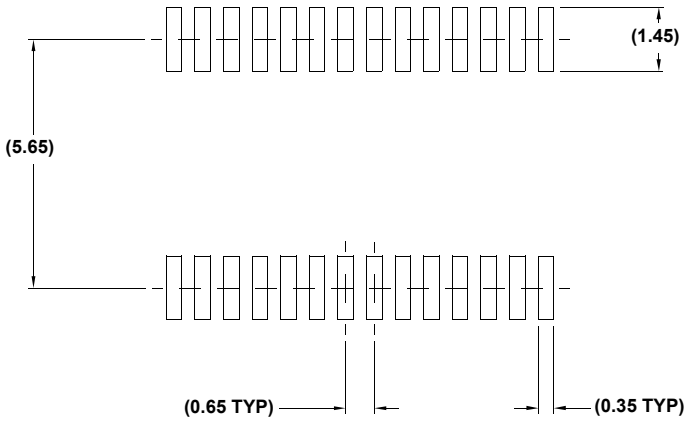
END VIEW



SIDE VIEW



DETAIL "X"

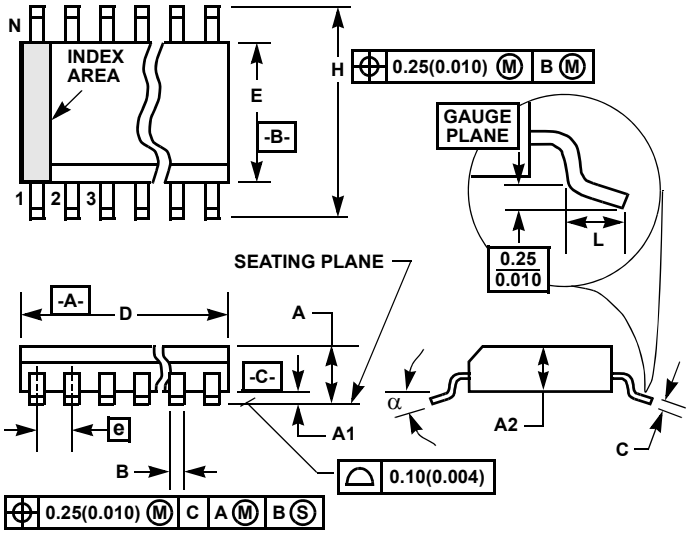


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

Shrink Small Outline Plastic Packages (SSOP)



NOTES:

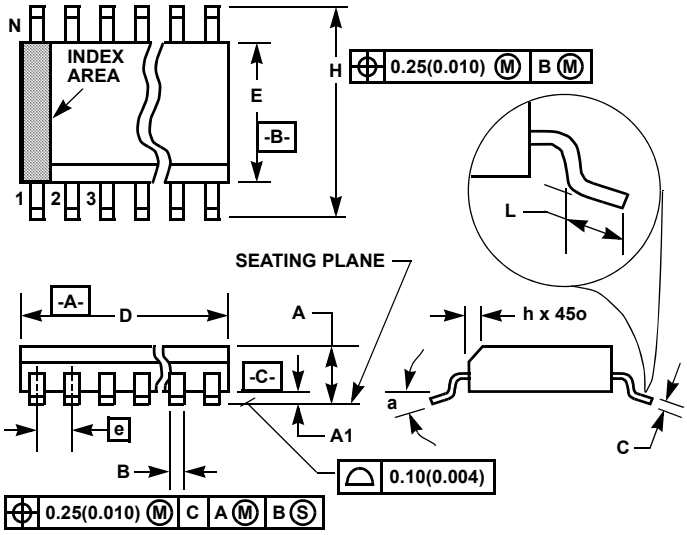
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.209 **(JEDEC MO-150-AH ISSUE B)**
28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 2 6/05

Small Outline Plastic Packages (SOIC)

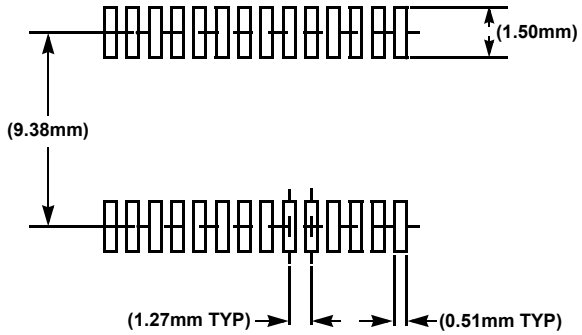


M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 1, 1/13

TYPICAL RECOMMENDED LAND PATTERN



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Intersil:

ICL3221ECAZ ICL3221ECAZ-T ICL3221ECVZ ICL3221ECVZ-T ICL3221EIAZ ICL3221EIAZ-T ICL3223ECAZ ICL3223ECAZ-T ICL3232ECBNZ ICL3232ECBNZ-T ICL3232ECV-16Z ICL3232ECV-16Z-T ICL3232EIBNZ ICL3232EIBNZ-T ICL3232EIV-16Z ICL3232EIV-16Z-T ICL3243ECAZ ICL3243ECAZ-T ICL3243ECVZ ICL3243ECVZ-T ICL3243EIAZ ICL3243EIAZ-T ICL3243EIVZ ICL3243EIVZ-T ICL3221ECAZ-T7A ICL3221EIAZ-T7A ICL3221EIVZ ICL3221EIVZ-T ICL3221EIVZ-T7A ICL3222ECAZ ICL3222ECAZ-T ICL3222ECVZ ICL3222ECVZ-T ICL3222EIAZ ICL3222EIAZ-T ICL3222EIBZ ICL3222EIBZ-T ICL3222EIVZ ICL3222EIVZ-T ICL3223ECVZ ICL3223ECVZ-T ICL3223EIAZ ICL3223EIAZ-T ICL3223EIVZ ICL3223EIVZ-T ICL3223EIVZ-T7A ICL3232ECAZ ICL3232ECAZ-T ICL3232ECAZ-T7A ICL3232ECBNZ-T7A ICL3232ECBZ ICL3232ECBZ-T ICL3232ECV-16Z-T7A ICL3232ECV-20Z ICL3232ECV-20ZT ICL3232EFV-16Z ICL3232EFV-16Z-T ICL3232EIAZ ICL3232EIAZ-T ICL3232EIBZ ICL3232EIBZ-T ICL3232EIV-16Z-T7A ICL3232EIV-20Z ICL3232EIV-20ZT ICL3241ECAZ ICL3241ECAZ-T ICL3241ECVZ ICL3241ECVZ-T ICL3241EIAZ ICL3241EIAZ-T ICL3241EIVZ ICL3241EIVZ-T ICL3243ECBZ ICL3243ECBZ-T ICL3243EIVZ-T7A