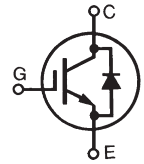
IXYS

High Voltage, High Gain BIMOSFET™

IXBF55N300

V_{CES} = 3000V
I_{C110} = 34A
$V_{CE(sat)}$ ≤ 3.2V

Monolithic Bipolar MOS Transistor

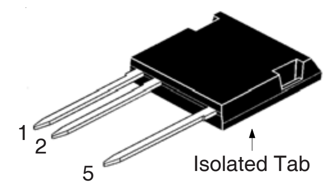


(Electrically Isolated Tab)

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	3000	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	3000	V
V_{GES}	Continuous	± 25	V
V_{GEM}	Transient	± 35	V
I_{C25}	T_C = 25°C	86	A
I_{C110}	T_C = 110°C	34	A
I_{CM}	T_C = 25°C, 1ms	600	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 2Ω Clamped Inductive Load	I_{CM} = 110 $V_{CE} \leq$ 0.8 • V_{CES}	A
T_{SC} **(SCSOA)**	V_{GE} = 15V, T_J = 125°C, R_G = 10Ω, V_{CE} = 1250V, Non-Repetitive	10	µs
P_C	T_C = 25°C	357	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10 seconds	260	°C
F_C	Mounting Force	20..120 / 4.5..27	Nm/lb.in.
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		5	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 1mA, V_{GE} = 0V	3000			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			50	µA
	Note 2, T_J = 125°C			3	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 25V			±200	nA
$V_{CE(sat)}$	I_C = 55A, V_{GE} = 15V, Note 1		2.7	3.2	V
	T_J = 125°C		3.3		V

ISOPLUS i4-Pak™



1 = Gate
2 = Emitter
5 = Collector

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

Advantages

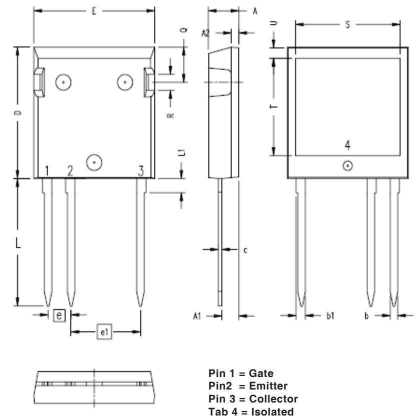
- Low Gate Drive Requirement
- High Power Density

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fS}	I_C = 55A, V_{CE} = 10V, Note 1	32	50		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		7300		pF
C_{oes}			275		pF
C_{res}			83		pF
Q_g	I_C = 55A, V_{GE} = 15V, V_{CE} = 1000V		335		nC
Q_{ge}			47		nC
Q_{gc}			130		nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		54		ns
t_r	I_C = 110A, V_{GE} = 15V		307		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 2Ω		230		ns
t_f			268		ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		52		ns
t_r	I_C = 110A, V_{GE} = 15V		585		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 2Ω		215		ns
t_f			260		ns
R_{thJC}				0.35	°C/W
R_{thCS}			0.15		°C/W

ISOPLUS i4-Pak™ (HV) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

Reverse Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
V_F	I_F = 55A, V_{GE} = 0V, Note 1			2.5	V
t_{rr}	I_F = 28A, V_{GE} = 0V, -di_F/dt = 100A/μs		1.9		μs
I_{RM}	V_R = 100V, V_{GE} = 0V		54		A

Notes:

1. Pulse test, t < 300μs, duty cycle, d < 2%.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

Fig. 1. Output Characteristics @ T_J = 25ºC

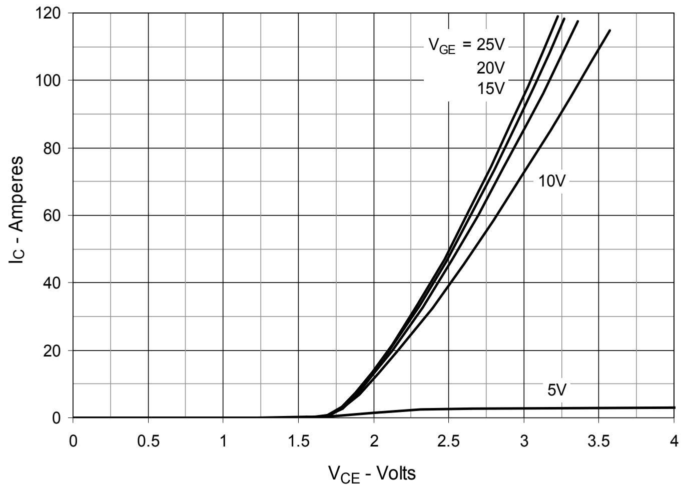


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

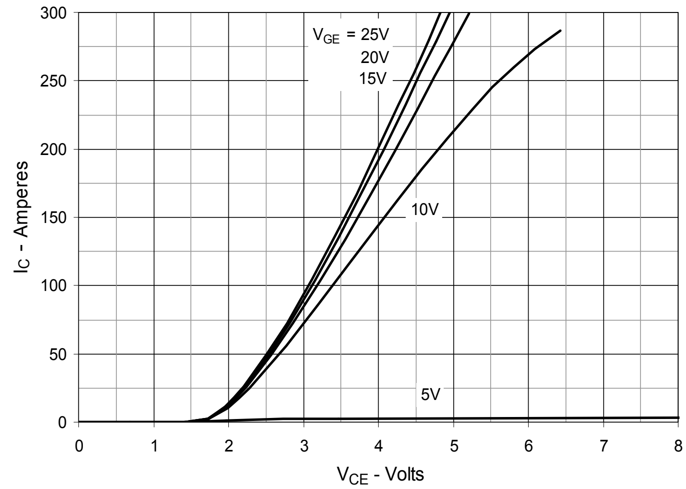


Fig. 3. Output Characteristics @ T_J = 125ºC

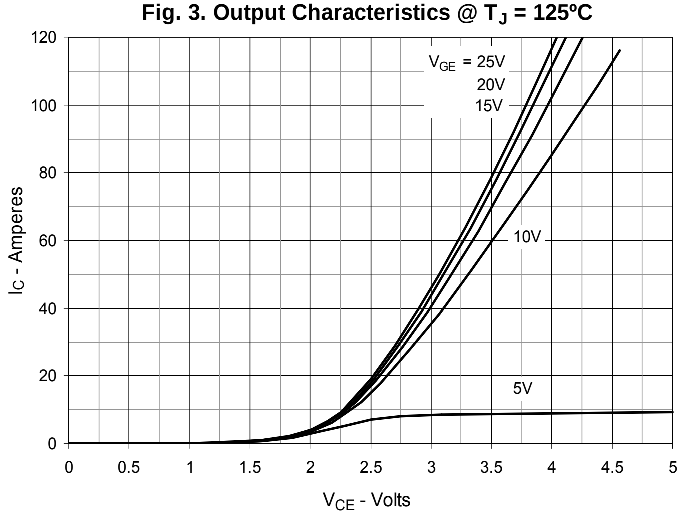


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

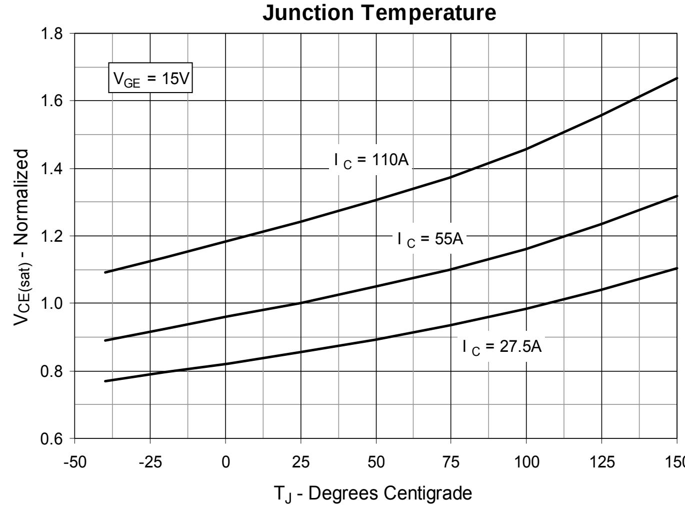


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

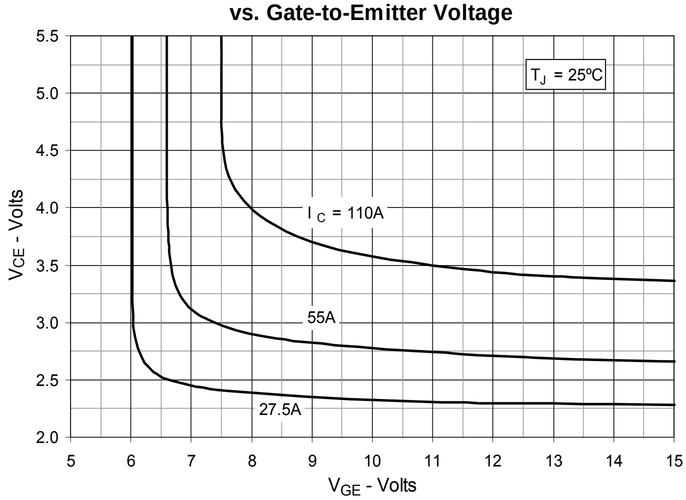


Fig. 6. Input Admittance

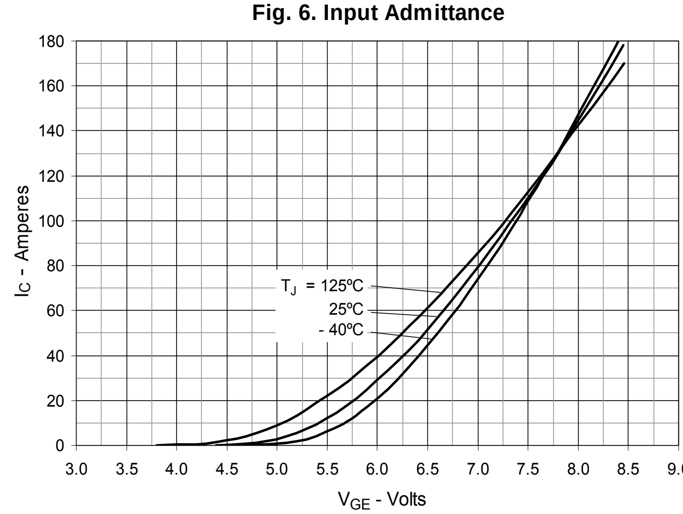


Fig. 7. Transconductance

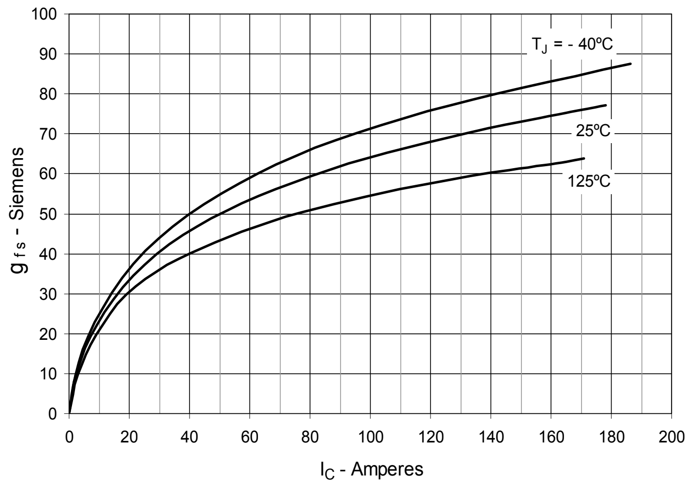


Fig. 8. Forward Voltage Drop of Intrinsic Diode

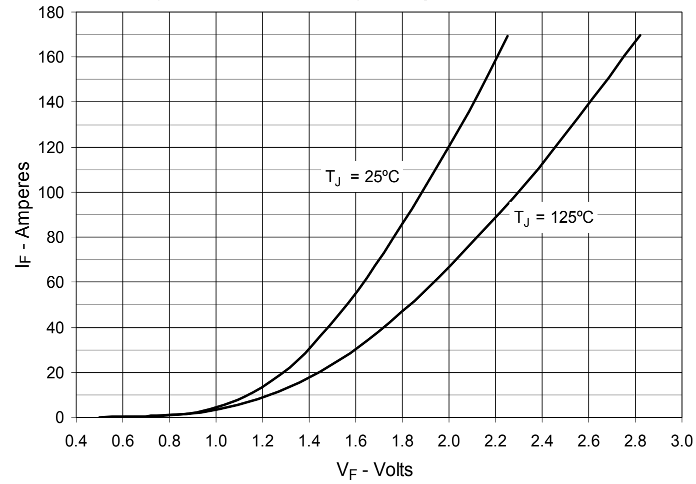


Fig. 9. Gate Charge

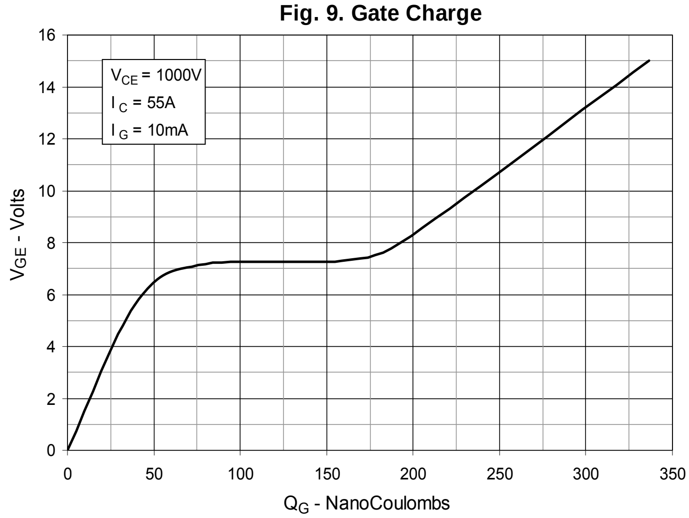


Fig. 10. Capacitance

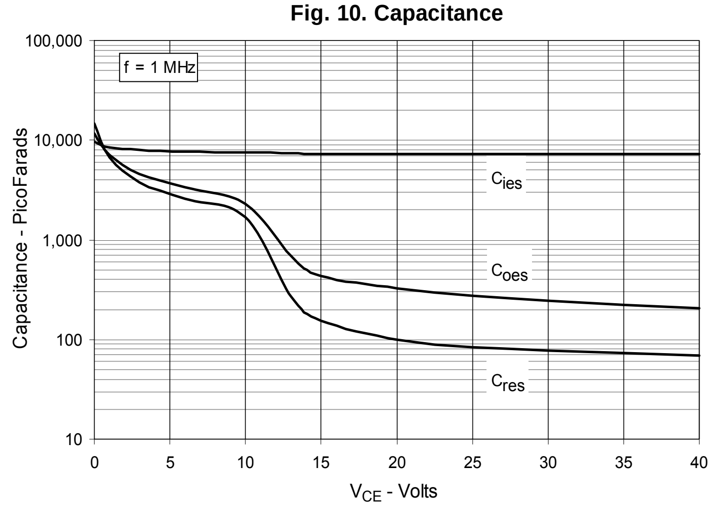


Fig. 11. Reverse-Bias Safe Operating Area

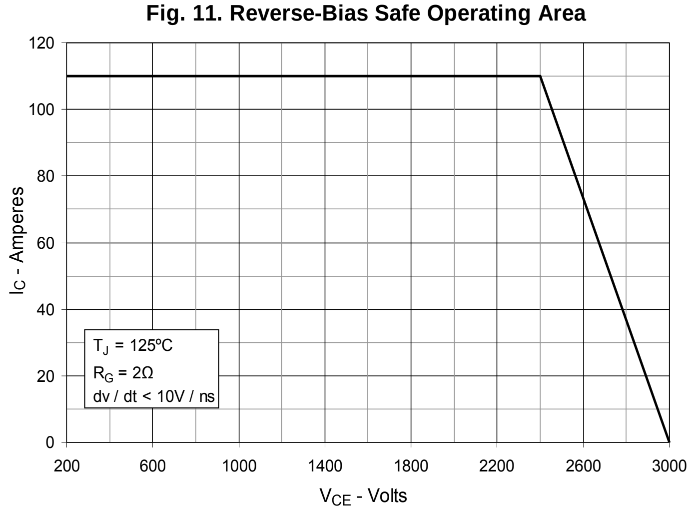


Fig. 12. Maximum Transient Thermal Impedance

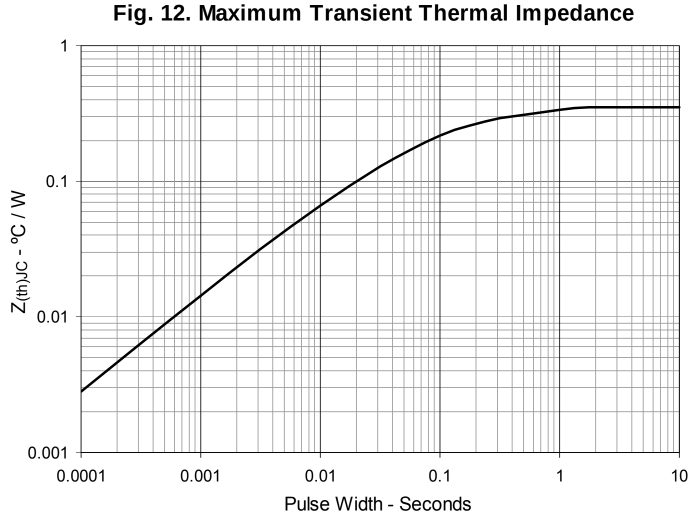


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

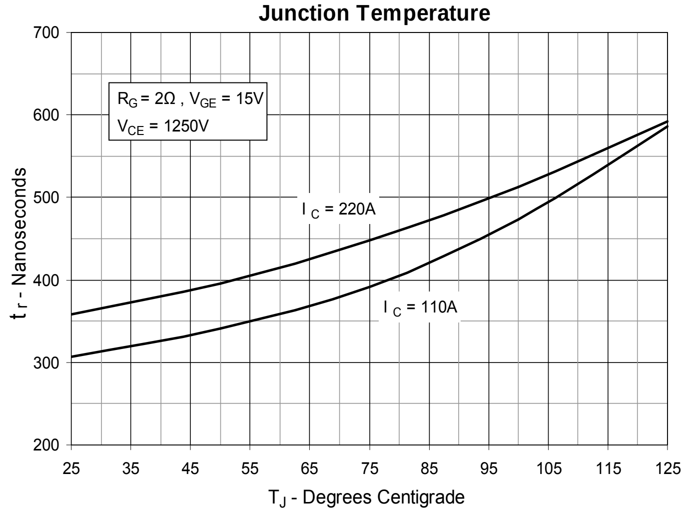


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

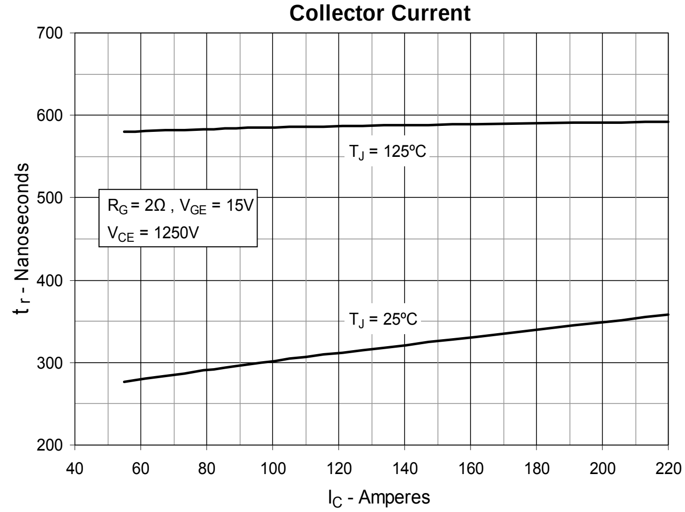


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

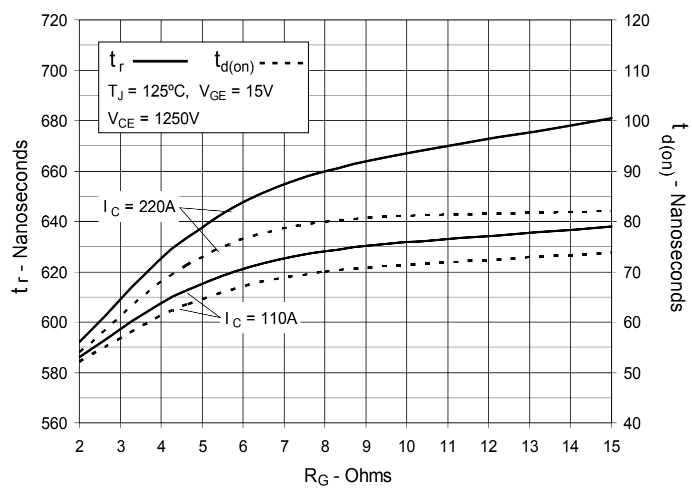


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

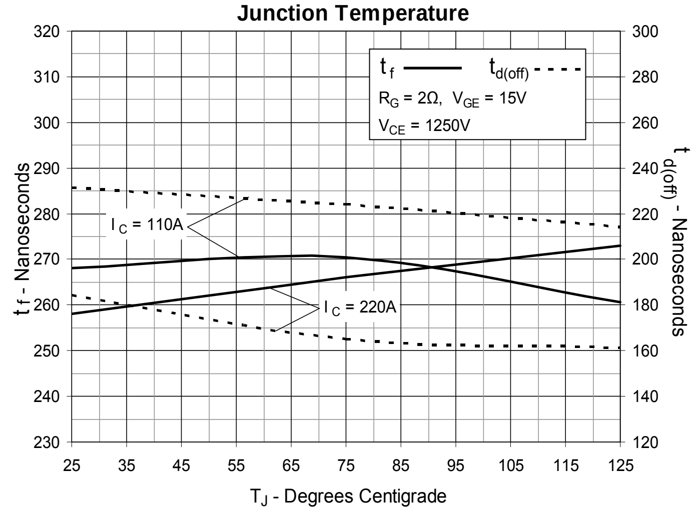


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

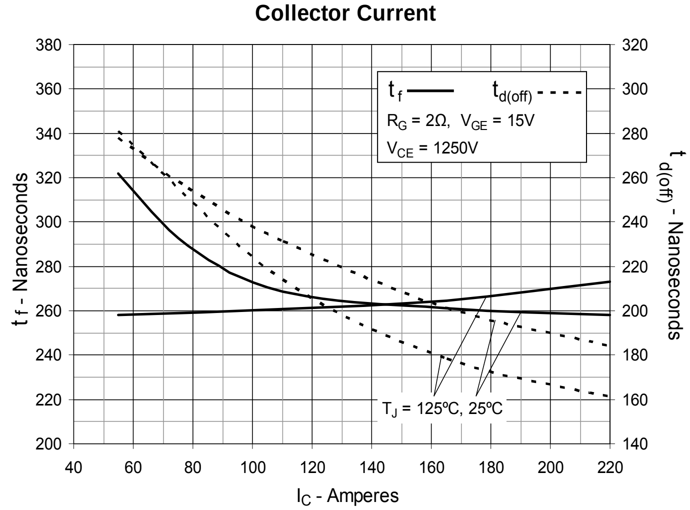
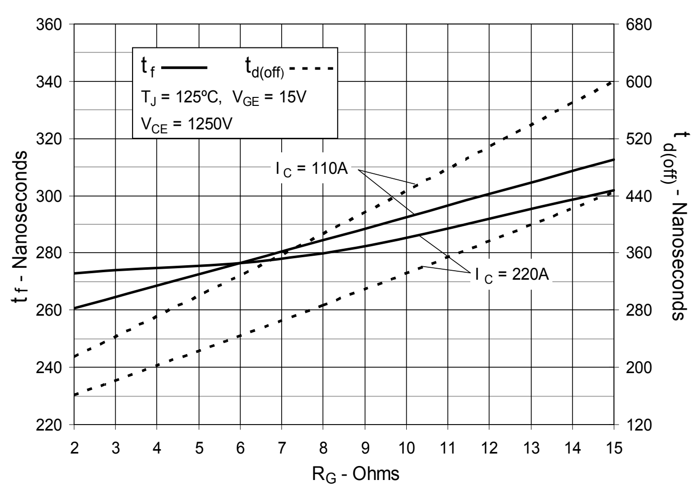


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance



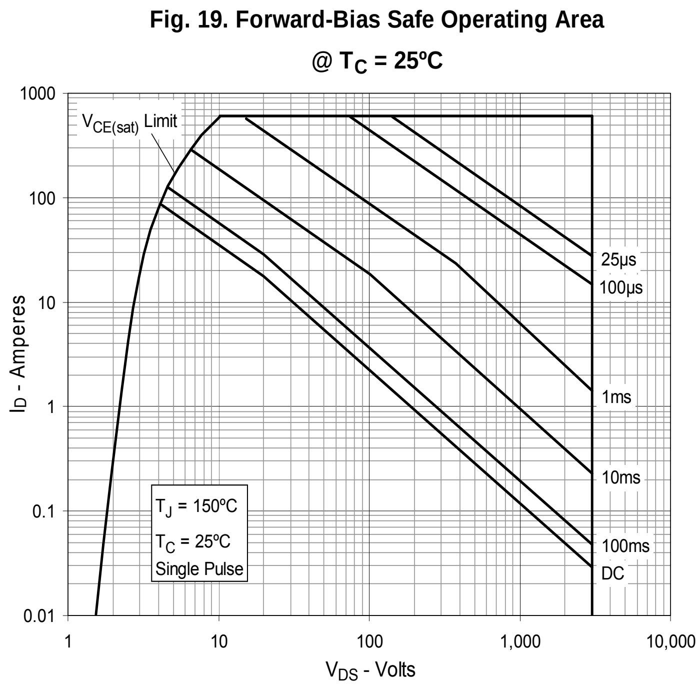


Fig. 19. Forward-Bias Safe Operating Area
@ T_C = 25ºC
1000
100
10
1
0.1
0.01
1
10
100
1,000
10,000
$V_{CE(sat)}$ Limit
25µs
100µs
1ms
10ms
100ms
DC
T_J = 150ºC
T_C = 25ºC
Single Pulse
I_D - Amperes
V_{DS} - Volts

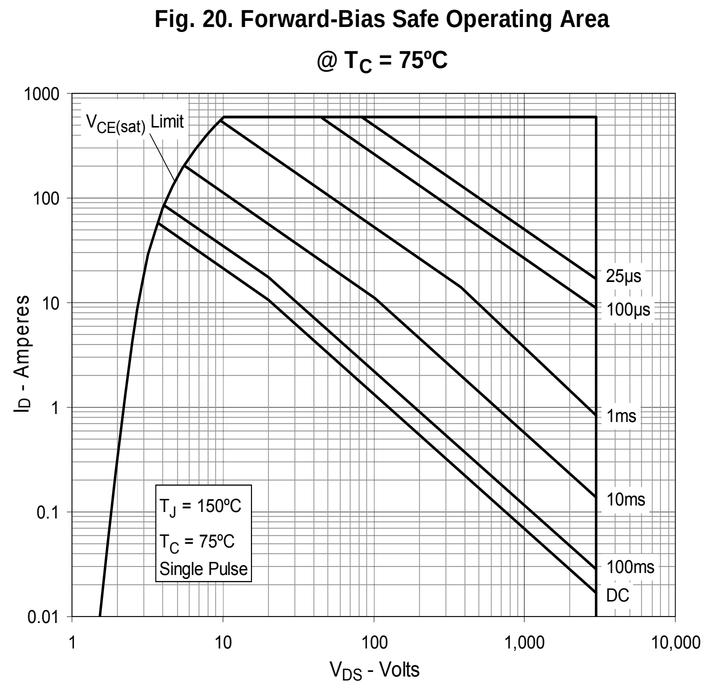


Fig. 20. Forward-Bias Safe Operating Area
@ T_C = 75ºC
1000
100
10
1
0.1
0.01
1
10
100
1,000
10,000
$V_{CE(sat)}$ Limit
25µs
100µs
1ms
10ms
100ms
DC
T_J = 150ºC
T_C = 75ºC
Single Pulse
I_D - Amperes
V_{DS} - Volts