# MCP6V81/1U

## 5 MHz, 0.5 mA, Zero-Drift Op Amps

### Features

- High DC Precision:
  - $V_{OS}$ Drift: ±20 nV/°C (maximum, $V_{DD}$ = 5.5V)
  - $V_{OS}$: ±9 µV (maximum)
  - $A_{OL}$: 126 dB (minimum, $V_{DD}$ = 5.5V)
  - PSRR: 117 dB (minimum, $V_{DD}$ = 5.5V)
  - CMRR: 118 dB (minimum, $V_{DD}$ = 5.5V)
  - $E_{ni}$: 0.28 µ$V_{P-P}$ (typical), f = 0.1 Hz to 10 Hz
  - $E_{ni}$: 0.1 µ$V_{P-P}$ (typical), f = 0.01 Hz to 1 Hz
- Enhanced EMI Protection:
  - Electromagnetic Interference Rejection Ratio (EMIRR) at 1.8 GHz: 101 dB
- Low Power and Supply Voltages:
  - $I_Q$: 0.5 mA/amplifier (typical)
  - Wide supply voltage range: 2.2V to 5.5V
- Small Packages:
  - Singles in SC70, SOT-23
- Easy to Use:
  - Rail-to-rail input/output
  - Gain Bandwidth Product: 5 MHz (typical)
  - Unity Gain Stable
- Extended Temperature Range: -40°C to +125°C

### Typical Applications

- Portable Instrumentation
- Sensor Conditioning
- Temperature Measurement
- DC Offset Correction
- Medical Instrumentation

### Design Aids

- SPICE Macro Models
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

### Related Parts

- MCP6V01/2/3: Auto-Zeroed, Spread Clock
- MCP6V06/7/8: Auto-Zeroed
- MCP6V26/7/8: Auto-Zeroed, Low Noise
- MCP6V11/1U/2/4: Zero-Drift, Low Power
- MCP6V31/1U/2/4: Zero-Drift, Low Power
- MCP6V61/1U: Zero-Drift, 1 MHz
- MCP6V71/1U: Zero-Drift, 2 MHz

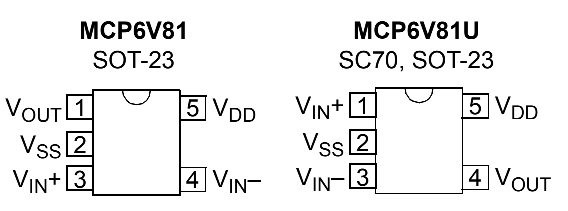
### General Description

The Microchip Technology Inc. MCP6V81/1U family of operational amplifiers provides input offset voltage correction for very low offset and offset drift. These devices have a gain bandwidth product of 5 MHz (typical). They are unity-gain stable, have virtually no 1/f noise and have good Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR). These products operate with a single supply voltage as low as 2.2V, while drawing 500 µA/amplifier (typical) of quiescent current.

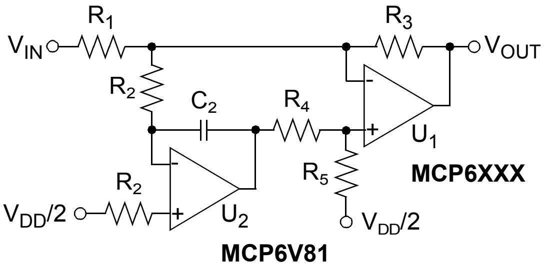
The MCP6V81/1U family has enhanced EMI protection to minimize any electromagnetic interference from external sources. This feature makes it well suited for EMI-sensitive applications such as power lines, radio stations and mobile communications, etc.

The Microchip Technology Inc. MCP6V81/1U op amps are offered in single (MCP6V81 and MCP6V81U) packages. They were designed using an advanced CMOS process.

### Package Types



### Typical Application Circuit



**Offset Voltage Correction for Power Driver**

Figures 1 and 2 show input offset voltage versus ambient temperature for different power supply voltages.

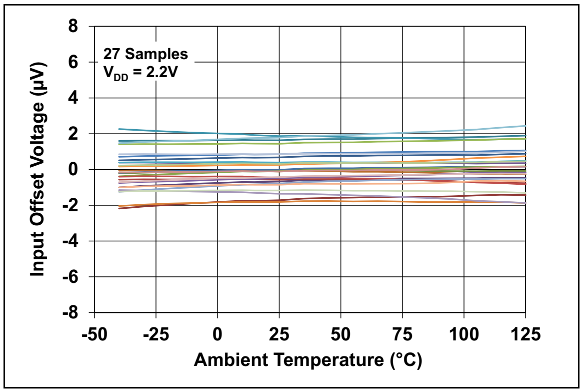


**FIGURE 1:** *Input Offset Voltage vs. Ambient Temperature with $V_{DD}$ = 2.2V.*

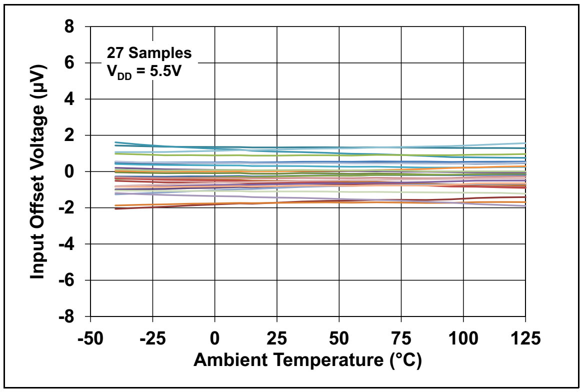


**FIGURE 2:** *Input Offset Voltage vs. Ambient Temperature with $V_{DD}$ = 5.5V.*

As seen in Figures 1 and 2, the MCP6V81/1U op amps have excellent performance across temperature.

The input offset voltage temperature drift ($TC_1$) shown is well within the specified maximum values of 20 nV/°C at $V_{DD}$ = 5.5V and 25 nV/°C at $V_{DD}$ = 2.2V.

This performance supports applications with stringent DC precision requirements. In many cases, it will not be necessary to correct for temperature effects (i.e., calibrate) in a design. In the other cases, the correction will be small.

# 1.0 ELECTRICAL CHARACTERISTICS

## 1.1 Absolute Maximum Ratings †

| | |
|---|---|
| $V_{DD} – V_{SS}$ | 6.5V |
| Current at Input Pins | ±2 mA |
| Analog Inputs ($V_{IN}$+ and $V_{IN}$–)(1) | $V_{SS}$ – 1.0V to $V_{DD}$ + 1.0V |
| All Other Inputs and Outputs | $V_{SS}$ – 0.3V to $V_{DD}$ + 0.3V |
| Difference Input Voltage | $\lvert V_{DD} – V_{SS}\rvert$ |
| Output Short Circuit Current | Continuous |
| Current at Output and Supply Pins | ±30 mA |
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature | +150°C |
| ESD protection on all pins (HBM, CDM, MM) | ≥ 2 kV, 1.5 kV, 400V. |

**† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** See **Section 4.2.1 “Rail-to-Rail Inputs”**.

## 1.2 Specifications

**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS**

**Electrical Characteristics:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to +5.5V, $V_{SS}$ = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF (refer to Figures 1-4 and 1-5).

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Input Offset** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | -9 | — | +9 | µV | $T_A$ = +25°C |
| Input Offset Voltage Drift with Temperature (Linear Temperature Coefficient) | $TC_1$ | -25 | — | +25 | nV/°C | $T_A$ = -40 to +125°C, $V_{DD}$ = 2.2V (**Note 1**) |
| | $TC_1$ | -20 | — | +20 | nV/°C | $T_A$ = -40 to +125°C, $V_{DD}$ = 5.5V (**Note 1**) |
| Input Offset Voltage Quadratic Temperature Coefficient | $TC_2$ | — | ±14 | — | pV/°C$^2$ | $T_A$ = -40 to +125°C $V_{DD}$ = 2.2V |
| | $TC_2$ | — | ±9 | — | pV/°C$^2$ | $T_A$ = -40 to +125°C $V_{DD}$ = 5.5V |
| Input Offset Voltage Aging | $\Delta V_{OS}$ | — | ±0.25 | — | µV | 408 hours Life Test at +150°, measured at +25°C. |
| Power Supply Rejection Ratio | PSRR | 117 | 127 | — | dB | |
| **Input Bias Current and Impedance** | | | | | | |
| Input Bias Current | $I_B$ | -50 | ±2 | +50 | pA | |
| Input Bias Current across Temperature | $I_B$ | — | +10 | — | pA | $T_A$ = +85°C |
| | $I_B$ | 0 | +0.24 | +1 | nA | $T_A$ = +125°C |

**Note 1:** For design guidance only; not tested.

**2:** Figure 2-19 shows how $V_{CML}$ and $V_{CMH}$ changed across temperature for the first production lot.

**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)**

| **Electrical Characteristics:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to +5.5V, $V_{SS}$ = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF (refer to Figures 1-4 and 1-5). | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Input Offset Current | $I_{OS}$ | -400 | ±100 | +400 | pA | |
| Input Offset Current across Temperature | $I_{OS}$ | — | ±75 | — | pA | $T_A$ = +85°C |
| | $I_{OS}$ | -500 | ±100 | +500 | pA | $T_A$ = +125°C |
| Common-mode Input Impedance | $Z_{CM}$ | — | $10^{13}$‖14 | — | Ω‖pF | |
| Differential Input Impedance | $Z_{DIFF}$ | — | $10^{13}$‖3 | — | Ω‖pF | |
| **Common Mode** | | | | | | |
| Common-mode Input Voltage Range Low | $V_{CML}$ | — | — | $V_{SS}$–0.2 | V | **Note 2** |
| Common-mode Input Voltage Range High | $V_{CMH}$ | $V_{DD}$+0.3 | — | — | V | **Note 2** |
| Common-mode Rejection Ratio | CMRR | 112 | 128 | — | dB | $V_{DD}$ = 2.2V,<br>$V_{CM}$ = -0.2V to 2.5V<br>**(Note 2)** |
| | CMRR | 118 | 136 | — | dB | $V_{DD}$ = 5.5V,<br>$V_{CM}$ = -0.2V to 5.8V<br>**(Note 2)** |
| **Open-Loop Gain** | | | | | | |
| DC Open-Loop Gain (Large Signal) | $A_{OL}$ | 119 | 146 | — | dB | $V_{DD}$ = 2.2V,<br>$V_{OUT}$ = 0.3V to 2.0V |
| | $A_{OL}$ | 126 | 151 | — | dB | $V_{DD}$ = 5.5V,<br>$V_{OUT}$ = 0.3V to 5.3V |
| **Output** | | | | | | |
| Minimum Output Voltage Swing | $V_{OL}$ | $V_{SS}$ | $V_{SS}$+35 | $V_{SS}$+120 | mV | $R_L$ = 1 kΩ, G = +2,<br>0.5V input overdrive |
| | $V_{OL}$ | — | $V_{SS}$+5 | — | mV | $R_L$ = 10 kΩ, G = +2,<br>0.5V input overdrive |
| Maximum Output Voltage Swing | $V_{OH}$ | $V_{DD}$–120 | $V_{DD}$–45 | $V_{DD}$ | mV | $R_L$ = 1 kΩ, G = +2,<br>0.5V input overdrive |
| | $V_{OH}$ | — | $V_{DD}$–5 | — | mV | $R_L$ = 10 kΩ, G = +2,<br>0.5V input overdrive |
| Output Short-Circuit Current | $I_{SC}$ | — | ±15 | — | mA | $V_{DD}$ = 2.2V |
| | $I_{SC}$ | — | ±40 | — | mA | $V_{DD}$ = 5.5V |
| **Power Supply** | | | | | | |
| Supply Voltage | $V_{DD}$ | 2.2 | — | 5.5 | V | |
| Quiescent Current per Amplifier | $I_Q$ | 250 | 500 | 770 | µA | $I_O$ = 0 |
| Power-on Reset (POR) Trip Voltage | $V_{POR}$ | 1.2 | 1.6 | 1.9 | V | |

**Note 1:** For design guidance only; not tested.

**2:** Figure 2-19 shows how $V_{CML}$ and $V_{CMH}$ changed across temperature for the first production lot.

## TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}/3$, $V_{OUT}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF (refer to Figures 1-4 and 1-5).

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Amplifier AC Response** | | | | | | |
| Gain Bandwidth Product | GBWP | — | 5 | — | MHz | |
| Slew Rate | SR | — | 4 | — | V/µs | |
| Phase Margin | PM | — | 60 | — | °C | G = +1 |
| **Amplifier Noise Response** | | | | | | |
| Input Noise Voltage | $E_{ni}$ | — | 0.1 | — | $µV_{P-P}$ | f = 0.01 Hz to 1 Hz |
| | $E_{ni}$ | — | 0.28 | — | $µV_{P-P}$ | f = 0.1 Hz to 10 Hz |
| Input Noise Voltage Density | $e_{ni}$ | — | 13 | — | nV/√Hz | f < 2 kHz |
| Input Noise Current Density | $i_{ni}$ | — | 6 | — | fA/√Hz | |
| **Amplifier Distortion**(1) | | | | | | |
| Intermodulation Distortion (AC) | IMD | — | 100 | — | $µV_{PK}$ | $V_{CM}$ tone = 100 $mV_{PK}$ at 1 kHz, $G_N$ = 11, RTI |
| **Amplifier Step Response** | | | | | | |
| Start-Up Time | $t_{STR}$ | — | 100 | — | µs | G = +1, 0.1% $V_{OUT}$ settling **(Note 2)** |
| Offset Correction Settling Time | $t_{STL}$ | — | 30 | — | µs | G = +1, $V_{IN}$ step of 2V, $V_{OS}$ within 100 µV of its final value |
| Output Overdrive Recovery Time | $t_{ODR}$ | — | 60 | — | µs | G = -10, ±0.5V input overdrive to $V_{DD}/2$, $V_{IN}$ 50% point to $V_{OUT}$ 90% point **(Note 3)** |
| **EMI Protection** | | | | | | |
| EMI Rejection Ratio | EMIRR | — | 90 | — | dB | $V_{IN}$ = 0.1 $V_{PK}$, f = 400 MHz |
| | | — | 100 | — | | $V_{IN}$ = 0.1 $V_{PK}$, f = 900 MHz |
| | | — | 101 | — | | $V_{IN}$ = 0.1 $V_{PK}$, f = 1800 MHz |
| | | — | 105 | — | | $V_{IN}$ = 0.1 $V_{PK}$, f = 2400 MHz |

**Note 1:** These parameters were characterized using the circuit in Figure 1-6. In Figures 2-39 and 2-40, there is an IMD tone at DC, a residual tone at 1 kHz and other IMD tones and clock tones. IMD is Referred to Input (RTI).

**2:** High gains behave differently; see **Section 4.3.3 "Offset at Power-Up"**.

**3:** $t_{STL}$ and $t_{ODR}$ include some uncertainty due to clock edge timing.

## TABLE 1-3: TEMPERATURE SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: $V_{DD}$ = +2.2V to +5.5V, $V_{SS}$ = GND.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | **Note 1** |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 5LD-SC70 | $\theta_{JA}$ | — | 209 | — | °C/W | |
| Thermal Resistance, 5LD-SOT-23 | $\theta_{JA}$ | — | 201 | — | °C/W | |

**Note 1:** Operation must not cause $T_J$ to exceed Maximum Junction Temperature specification (+150°C).

## 1.3 Timing Diagrams

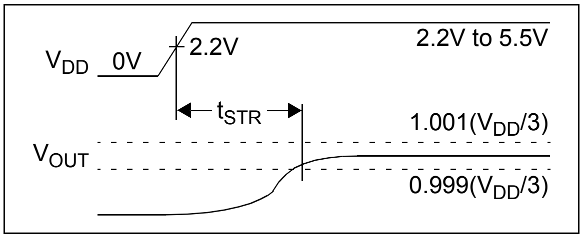


**FIGURE 1-1:** *Amplifier Start-Up.*

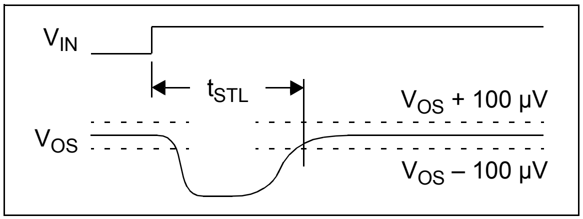


**FIGURE 1-2:** *Offset Correction Settling Time.*

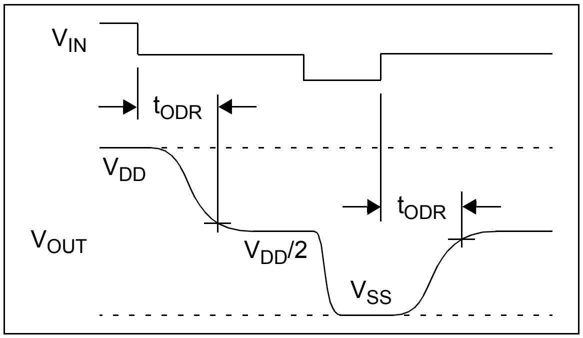


**FIGURE 1-3:** *Output Overdrive Recovery.*

## 1.4 Test Circuits

The circuits used for most DC and AC tests are shown in Figures 1-4 and 1-5. Lay the bypass capacitors out as discussed in **Section 4.3.10 "Supply Bypassing and Filtering"**. $R_N$ is equal to the parallel combination of $R_F$ and $R_G$ to minimize bias current effects.

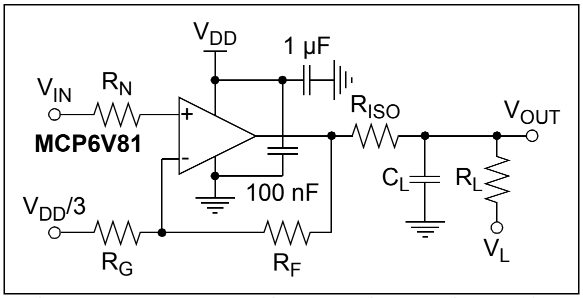


**FIGURE 1-4:** *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

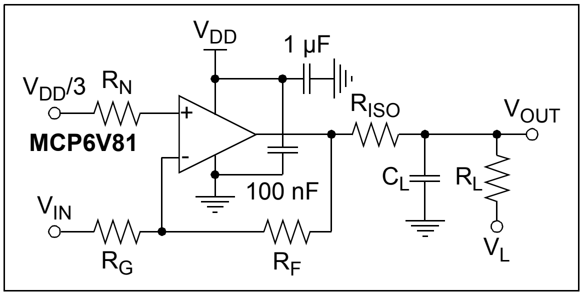


**FIGURE 1-5:** *AC and DC Test Circuit for Most Inverting Gain Conditions.*

The circuit in Figure 1-6 tests the input's dynamic behavior (i.e., IMD, $t_{STR}$, $t_{STL}$ and $t_{ODR}$). The potentiometer balances the resistor network ($V_{OUT}$ should equal $V_{REF}$ at DC). The op amp's common-mode input voltage is $V_{CM} = V_{IN}/2$. The error at the input ($V_{ERR}$) appears at $V_{OUT}$ with a noise gain of 10 V/V.

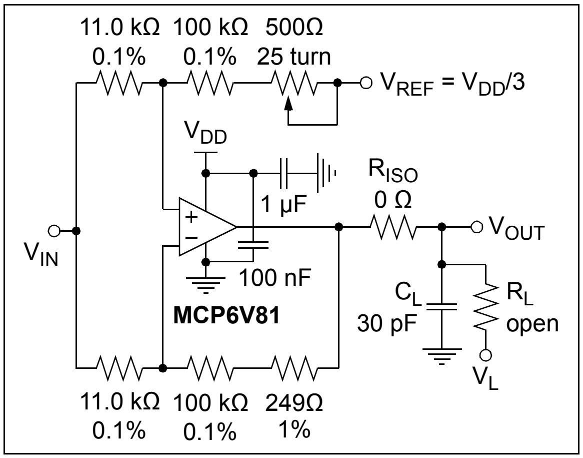


**FIGURE 1-6:** *Test Circuit for Dynamic Input Behavior.*

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to 5.5V, $V_{SS}$ = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF.

### 2.1 DC Input Precision

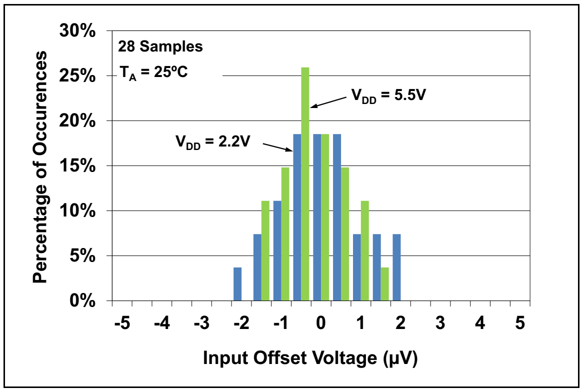


*FIGURE 2-1: Input Offset Voltage.*

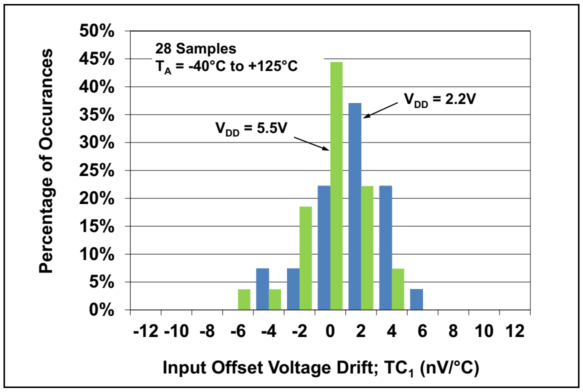


*FIGURE 2-2: Input Offset Voltage Drift.*

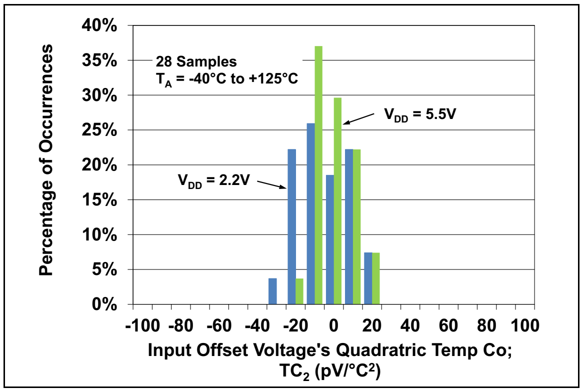


*FIGURE 2-3: Input Offset Voltage Quadratic Temperature Coefficient.*

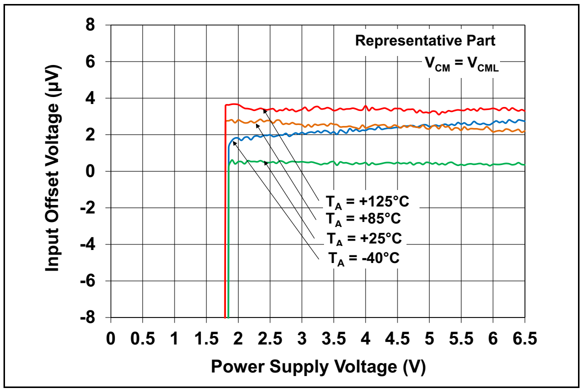


*FIGURE 2-4: Input Offset Voltage vs. Power Supply Voltage with $V_{CM} = V_{CML}$.*

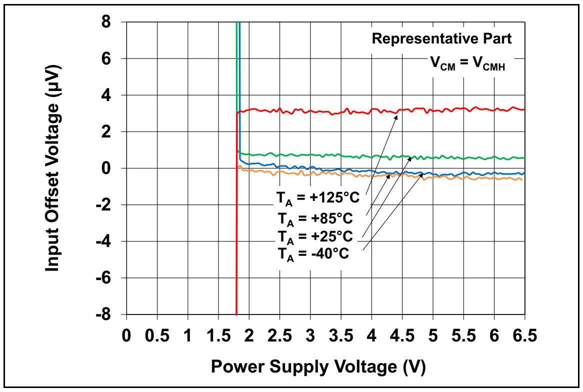


*FIGURE 2-5: Input Offset Voltage vs. Power Supply Voltage with $V_{CM} = V_{CMH}$.*

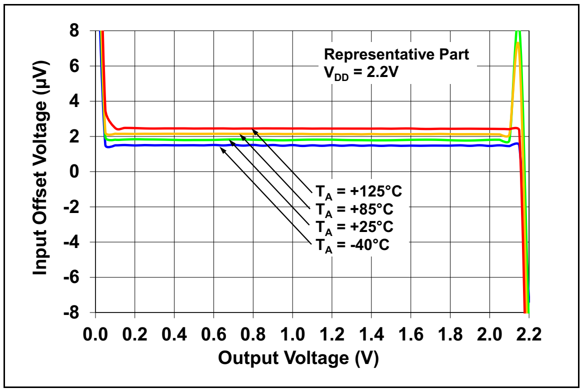


*FIGURE 2-6: Input Offset Voltage vs. Output Voltage with $V_{DD}$ = 2.2V.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to 5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/3, $V_{OUT}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF.

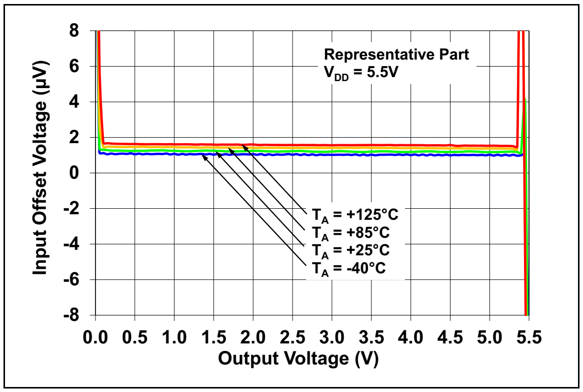


***FIGURE 2-7:*** *Input Offset Voltage vs. Output Voltage with $V_{DD}$ = 5.5V.*

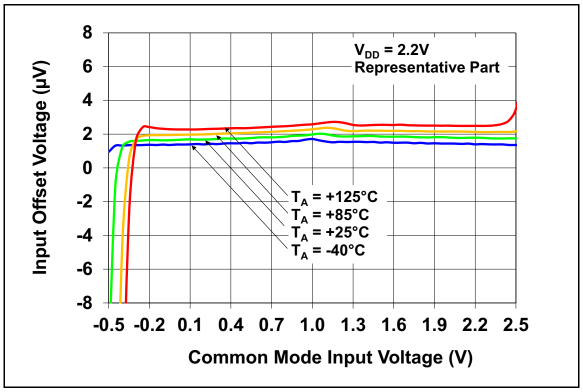


***FIGURE 2-8:*** *Input Offset Voltage vs. Common-Mode Voltage with $V_{DD}$ = 2.2V.*

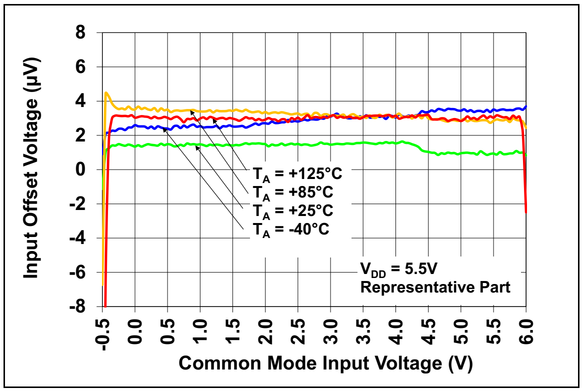


***FIGURE 2-9:*** *Input Offset Voltage vs. Common-Mode Voltage with $V_{DD}$ = 5.5V.*

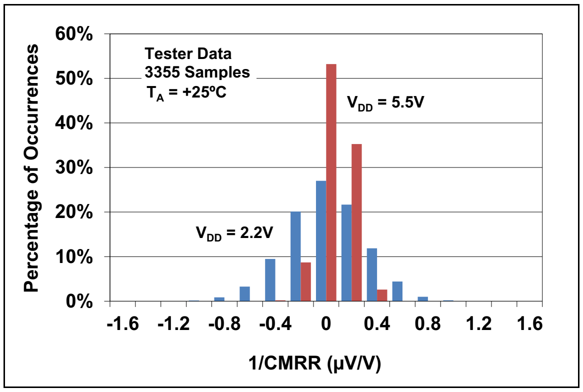


***FIGURE 2-10:*** *Common-Mode Rejection Ratio.*

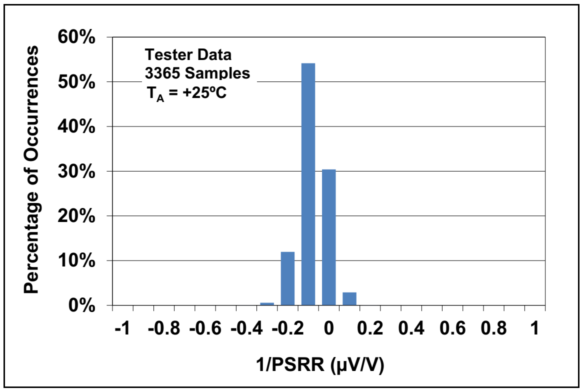


***FIGURE 2-11:*** *Power Supply Rejection Ratio.*

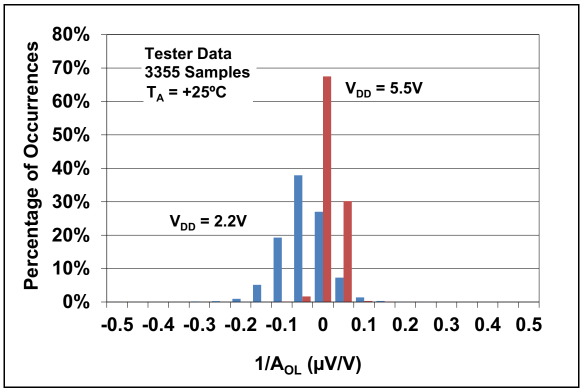


***FIGURE 2-12:*** *DC Open-Loop Gain.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to 5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}/3$, $V_{OUT}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF.

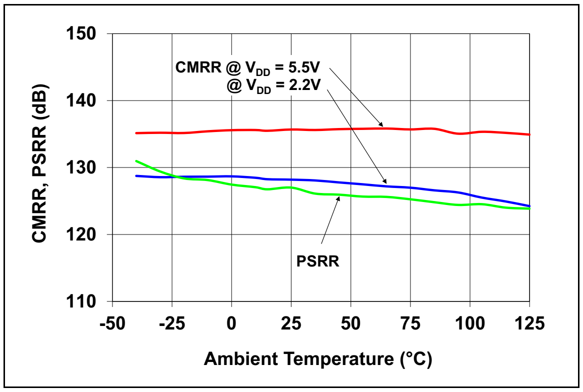


***FIGURE 2-13:*** *CMRR and PSRR vs. Ambient Temperature.*

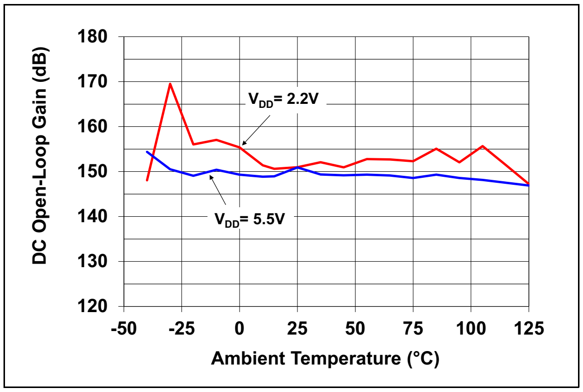


***FIGURE 2-14:*** *DC Open-Loop Gain vs. Ambient Temperature.*

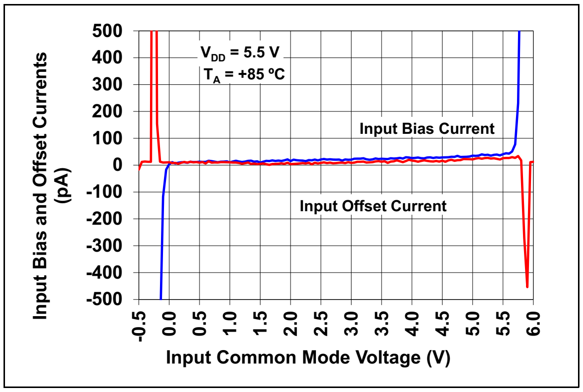


***FIGURE 2-15:*** *Input Bias and Offset Currents vs. Common-Mode Input Voltage with $T_A$ = +85°C.*

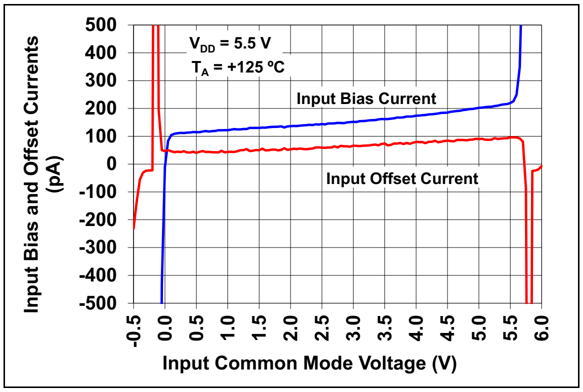


***FIGURE 2-16:*** *Input Bias and Offset Currents vs. Common-Mode Input Voltage with $T_A$ = +125°C.*

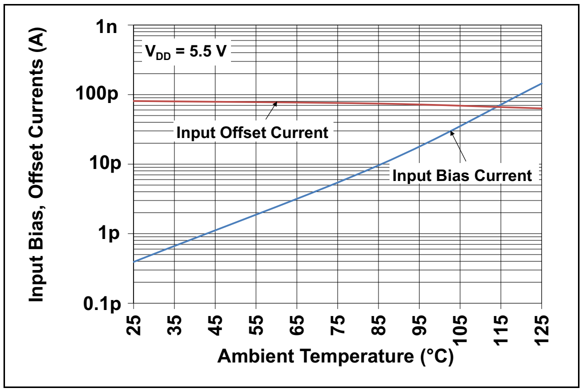


***FIGURE 2-17:*** *Input Bias and Offset Currents vs. Ambient Temperature with $V_{DD}$ = 5.5V.*

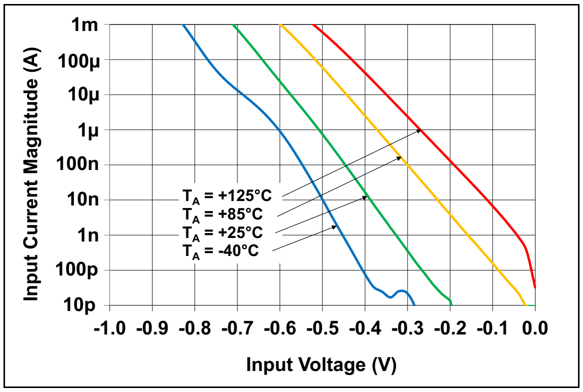


***FIGURE 2-18:*** *Input Bias Current vs. Input Voltage (Below $V_{SS}$).*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to 5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}/3$, $V_{OUT}$ = $V_{DD}/2$, $V_L$ = $V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF.

## 2.2 Other DC Voltages and Currents

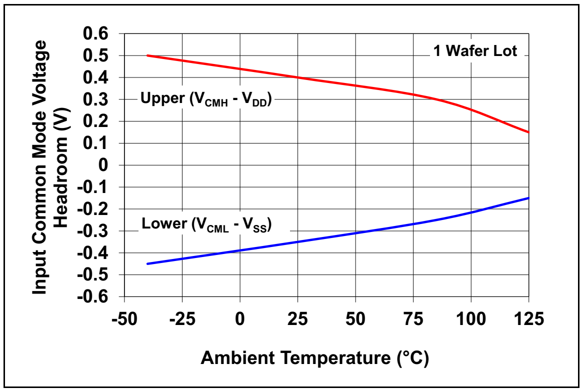


***FIGURE 2-19:*** *Input Common-Mode Voltage Headroom (Range) vs. Ambient Temperature.*

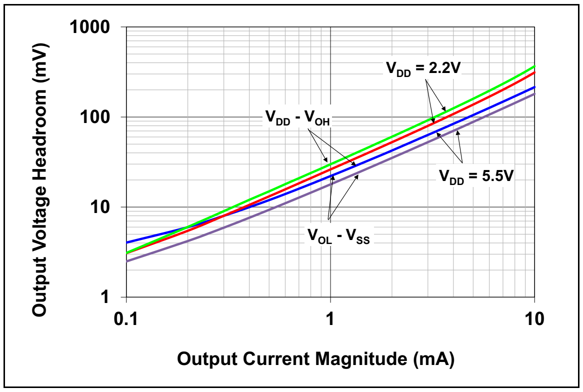


***FIGURE 2-20:*** *Output Voltage Headroom vs. Output Current.*

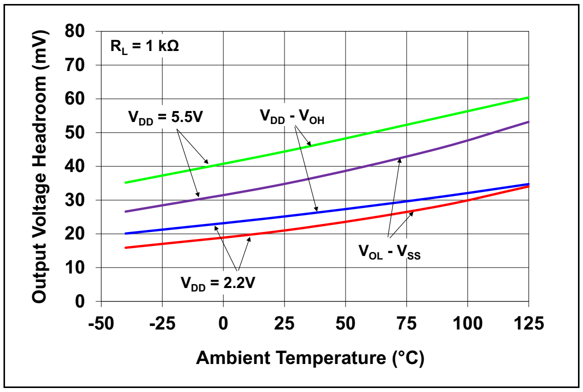


***FIGURE 2-21:*** *Output Voltage Headroom vs. Ambient Temperature.*

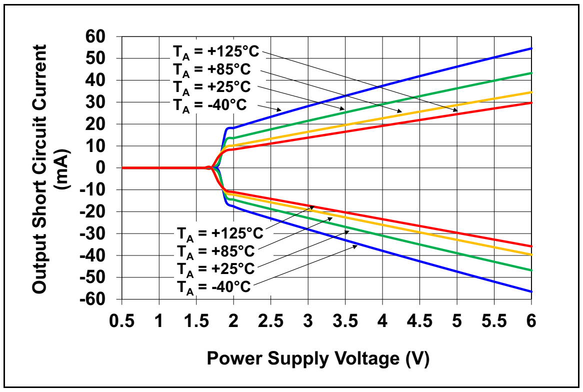


***FIGURE 2-22:*** *Output Short-Circuit Current vs. Power Supply Voltage.*

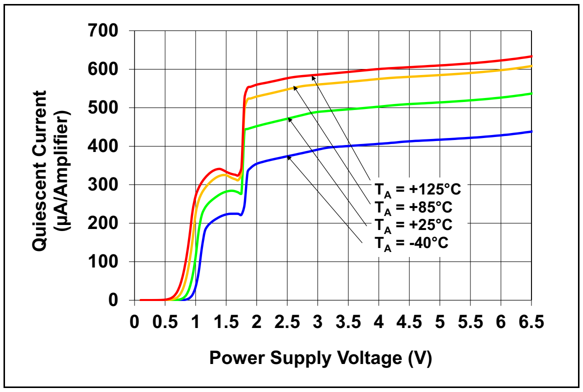


***FIGURE 2-23:*** *Supply Current vs. Power Supply Voltage.*

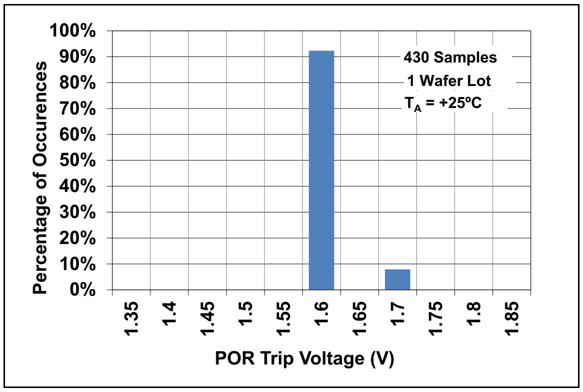


***FIGURE 2-24:*** *Power-On Reset Trip Voltage.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to 5.5V, $V_{SS}$ = GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF.

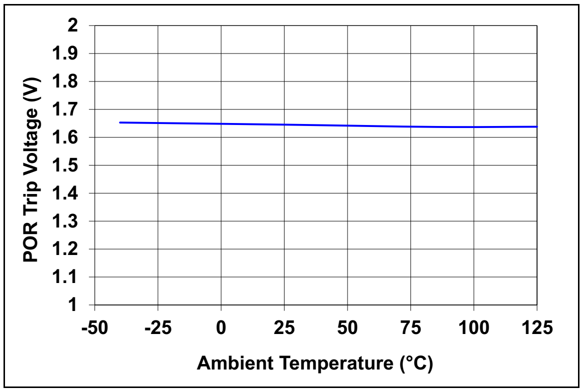


***FIGURE 2-25:*** *Power-On Reset Voltage vs. Ambient Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to 5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/3, $V_{OUT}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF.

## 2.3 Frequency Response

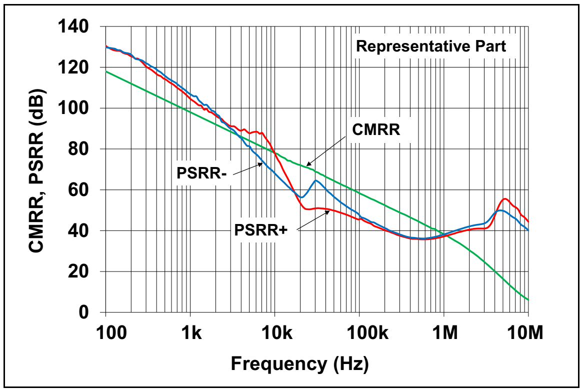


***FIGURE 2-26:*** *CMRR and PSRR vs. Frequency.*

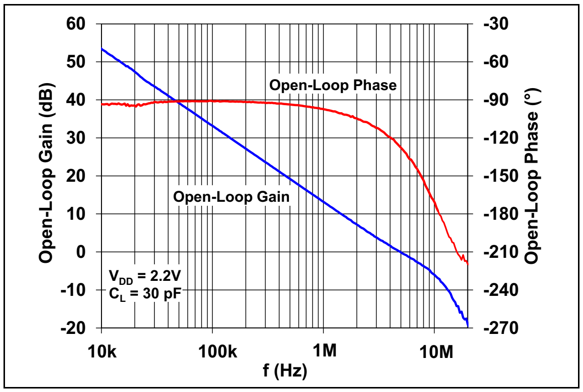


***FIGURE 2-27:*** *Open-Loop Gain vs. Frequency with $V_{DD}$ = 2.2V.*

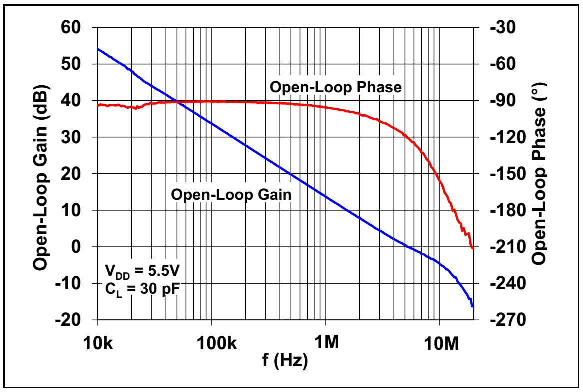


***FIGURE 2-28:*** *Open-Loop Gain vs. Frequency with $V_{DD}$ = 5.5V.*

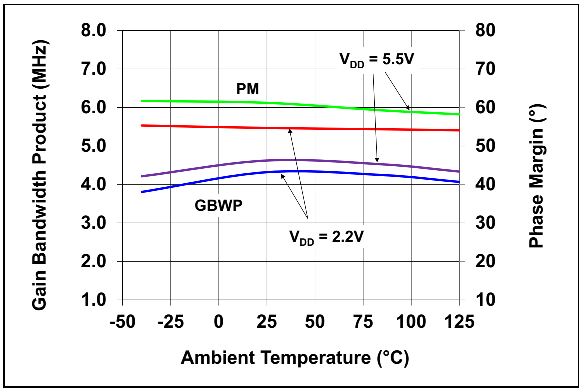


***FIGURE 2-29:*** *Gain Bandwidth Product and Phase Margin vs. Ambient Temperature.*

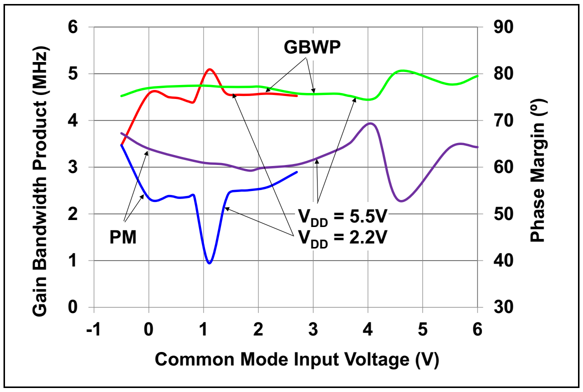


***FIGURE 2-30:*** *Gain Bandwidth Product and Phase Margin vs. Common-Mode Input Voltage.*

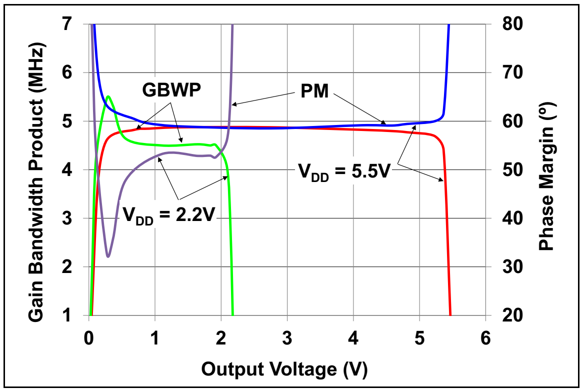


***FIGURE 2-31:*** *Gain Bandwidth Product and Phase Margin vs. Output Voltage.*

**Note:** Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = +2.2V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to $V_L$ and $C_L = 30\ pF$.

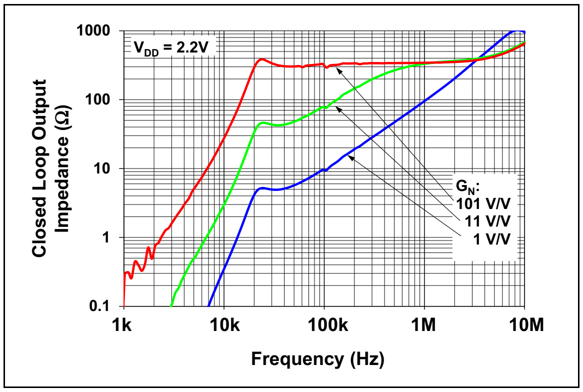


***FIGURE 2-32:*** *Closed-Loop Output Impedance vs. Frequency with $V_{DD}$ = 2.2V.*

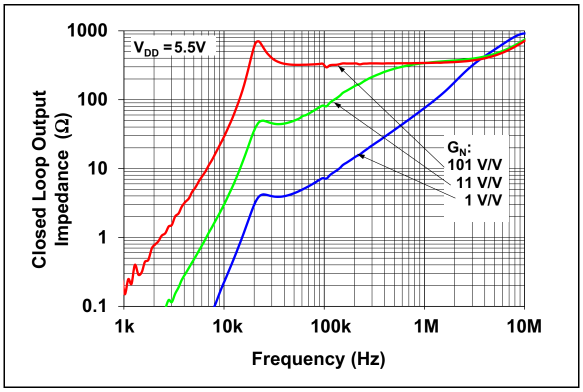


***FIGURE 2-33:*** *Closed-Loop Output Impedance vs. Frequency with $V_{DD}$ = 5.5V.*

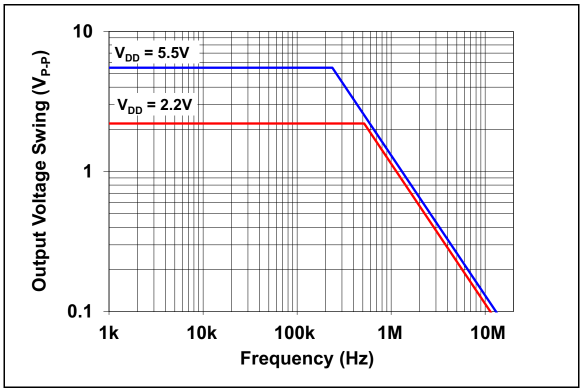


***FIGURE 2-34:*** *Maximum Output Voltage Swing vs. Frequency.*

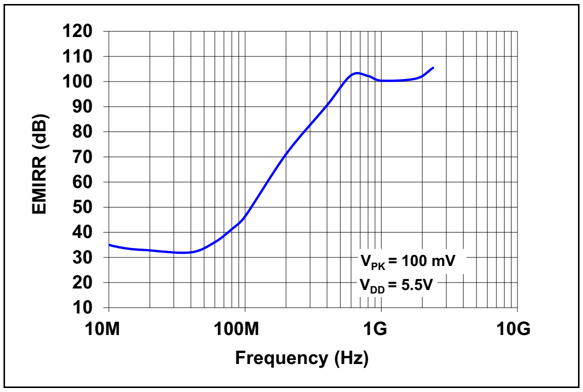


***FIGURE 2-35:*** *EMIRR vs. Frequency.*

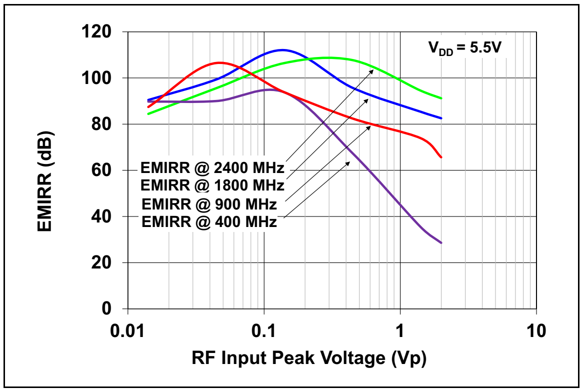


***FIGURE 2-36:*** *EMIRR vs. Input Voltage.*

**Note:** Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = +2.2V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to $V_L$ and $C_L = 30\ pF$.

## 2.4 Input Noise and Distortion

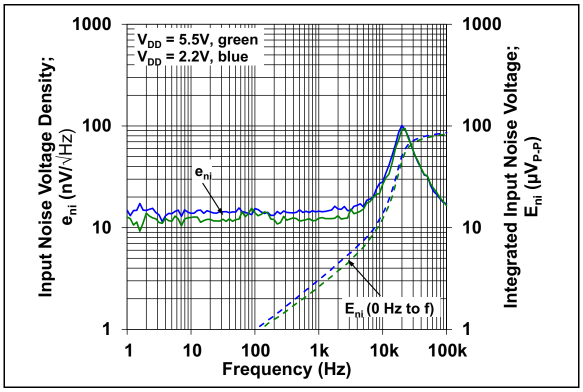


***FIGURE 2-37:*** *Input Noise Voltage Density and Integrated Input Noise Voltage vs. Frequency.*

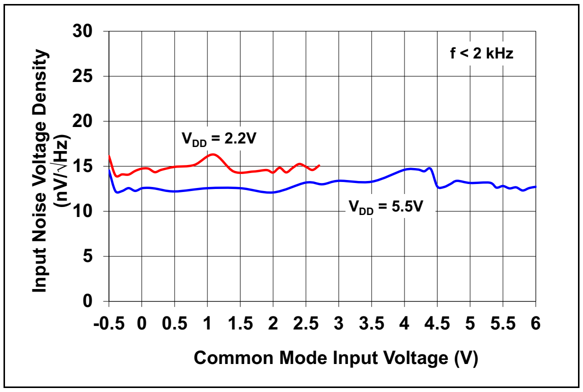


***FIGURE 2-38:*** *Input Noise Voltage Density vs. Input Common-Mode Voltage.*

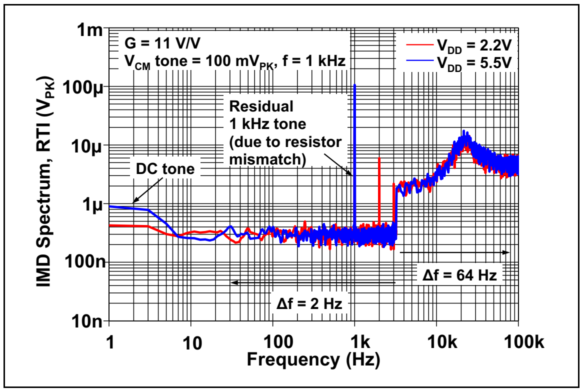


***FIGURE 2-39:*** *Intermodulation Distortion vs. Frequency with $V_{CM}$ Disturbance (see Figure 1-6).*

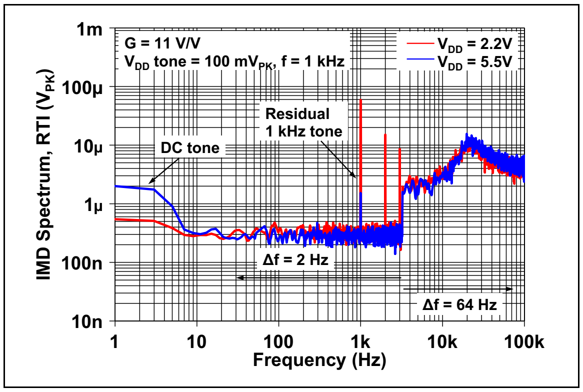


***FIGURE 2-40:*** *Intermodulation Distortion vs. Frequency with $V_{DD}$ Disturbance (see Figure 1-6).*

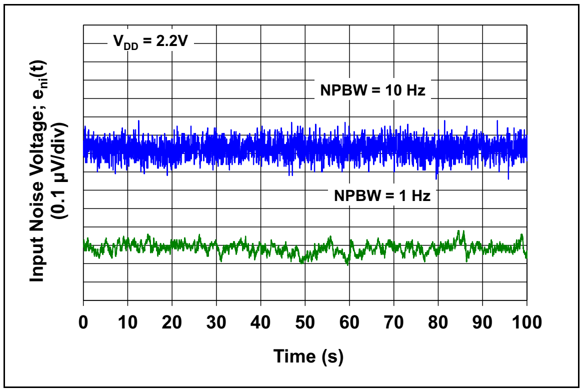


***FIGURE 2-41:*** *Input Noise vs. Time with 1 Hz and 10 Hz Filters and $V_{DD}$ = 2.2V.*

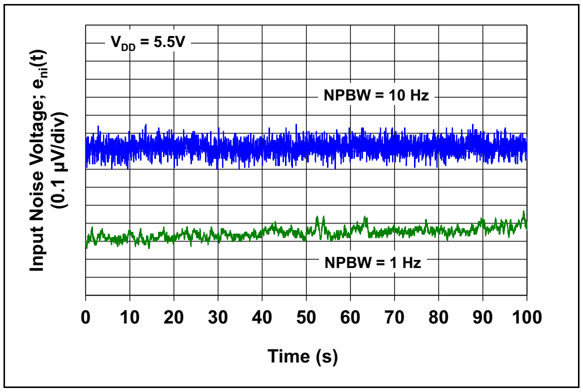


***FIGURE 2-42:*** *Input Noise vs. Time with 1 Hz and 10 Hz Filters and $V_{DD}$ = 5.5V.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to 5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/3, $V_{OUT}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF.

## 2.5 Time Response

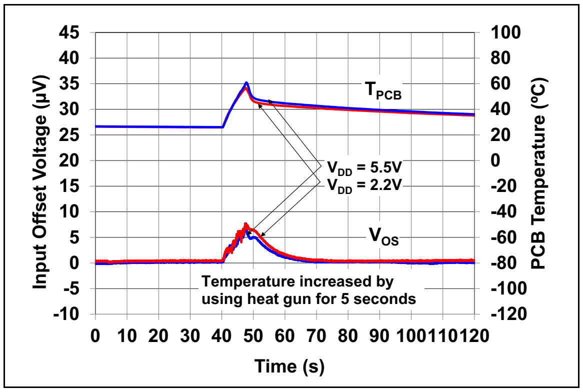


***FIGURE 2-43:*** *Input Offset Voltage vs. Time with Temperature Change.*

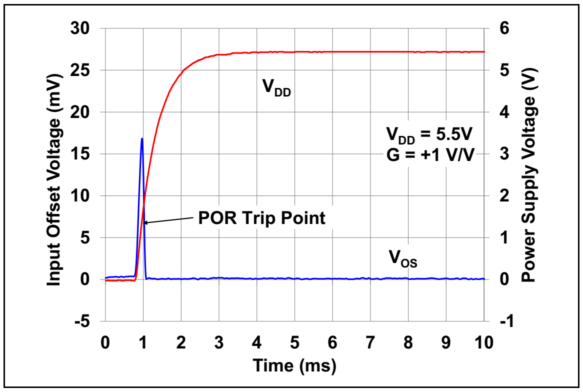


***FIGURE 2-44:*** *Input Offset Voltage vs. Time at Power-Up.*

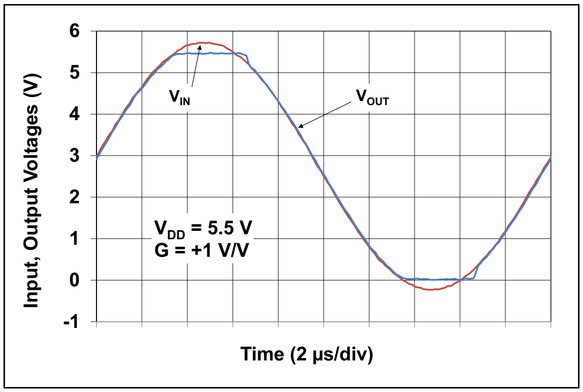


***FIGURE 2-45:*** *The MCP6V81/1U Family Shows No Input Phase Reversal with Overdrive.*

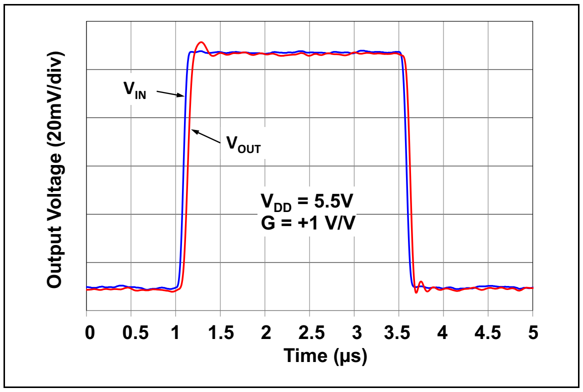


***FIGURE 2-46:*** *Non-Inverting Small Signal Step Response.*

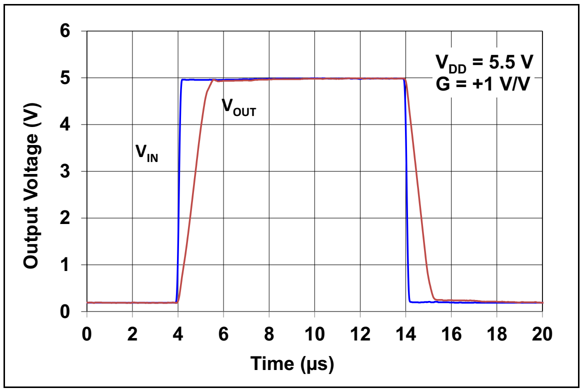


***FIGURE 2-47:*** *Non-Inverting Large Signal Step Response.*

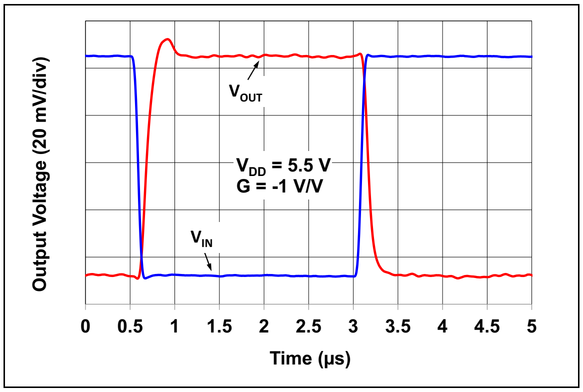


***FIGURE 2-48:*** *Inverting Small Signal Step Response.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +2.2V to 5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/3, $V_{OUT}$ = $V_{DD}$/2, $V_L$ = $V_{DD}$/2, $R_L$ = 10 kΩ to $V_L$ and $C_L$ = 30 pF.

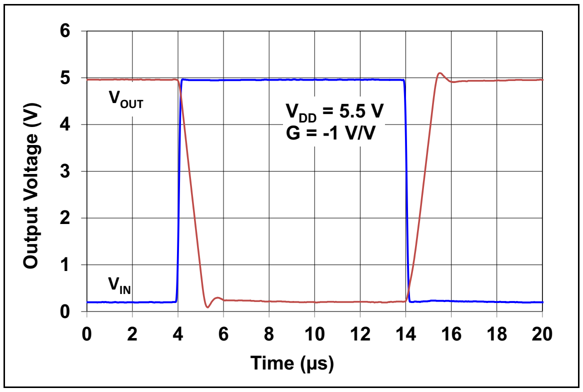


***FIGURE 2-49:*** *Inverting Large Signal Step Response.*

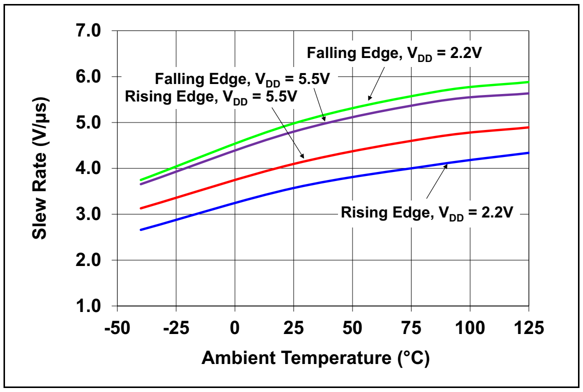


***FIGURE 2-50:*** *Slew Rate vs. Ambient Temperature.*

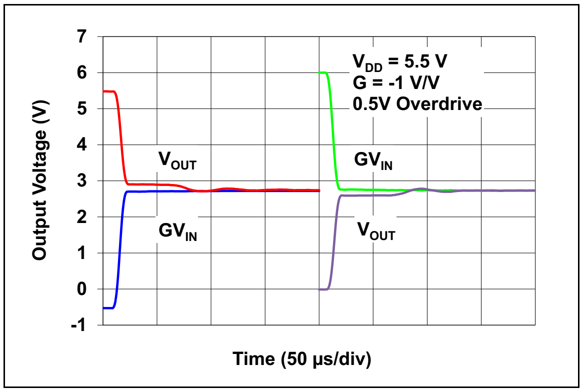


***FIGURE 2-51:*** *Output Overdrive Recovery vs. Time with G = -10 V/V.*

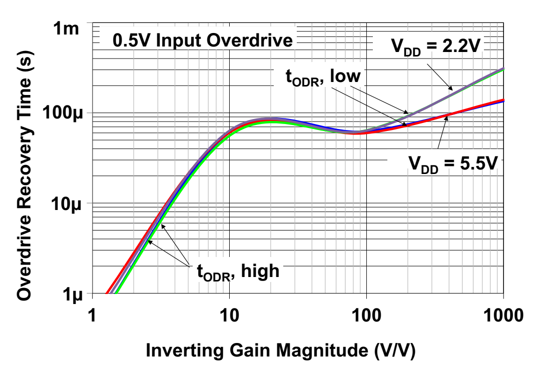


***FIGURE 2-52:*** *Output Overdrive Recovery Time vs. Inverting Gain.*

## 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| MCP6V81 | MCP6V81U | Symbol | Description |
|---|---|---|---|
| SOT-23 | SOT-23, SC70 | | |
| 1 | 4 | $V_{OUT}$ | Output |
| 2 | 2 | $V_{SS}$ | Negative Power Supply |
| 3 | 1 | $V_{IN}+$ | Non-Inverting Input |
| 4 | 3 | $V_{IN}-$ | Inverting Input |
| 5 | 5 | $V_{DD}$ | Positive Power Supply |

### 3.1 Analog Outputs

The analog output pins ($V_{OUT}$) are low-impedance voltage sources.

### 3.2 Analog Inputs

The non-inverting and inverting inputs ($V_{IN}+$, $V_{IN}-$, …) are high-impedance CMOS inputs with low bias currents.

### 3.3 Power Supply Pins

The positive power supply ($V_{DD}$) is 2.2V to 5.5V higher than the negative power supply ($V_{SS}$). For normal operation, the other pins are between $V_{SS}$ and $V_{DD}$.

Typically, these parts are used in a single (positive) supply configuration. In this case, $V_{SS}$ is connected to ground and $V_{DD}$ is connected to the supply. $V_{DD}$ will need bypass capacitors.

NOTES:

## 4.0 APPLICATIONS

The MCP6V81/1U family of zero-drift op amps is manufactured using Microchip's state-of-the-art CMOS process. It is designed for precision applications with requirements for small packages and low power. Its low supply voltage and low quiescent current make the MCP6V81/1U devices ideal for battery-powered applications.

### 4.1 Overview of Zero-Drift Operation

Figure 4-1 shows a simplified diagram of the MCP6V81/1U zero-drift op amp. This diagram will be used to explain how slow voltage errors are reduced in this architecture (much better $V_{OS}$, $\Delta V_{OS}/\Delta T_A$ ($TC_1$), CMRR, PSRR, $A_{OL}$ and 1/f noise).

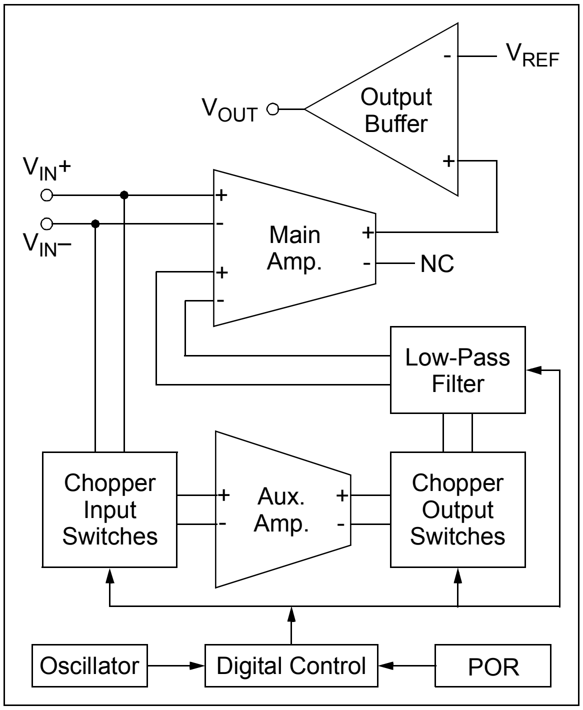


**FIGURE 4-1:** *Simplified Zero-Drift Op Amp Functional Diagram.*

#### 4.1.1 BUILDING BLOCKS

The main amplifier is designed for high gain and bandwidth, with a differential topology. Its main input pair (+ and - pins at the top left) is used for the higher frequency portion of the input signal. Its auxiliary input pair (+ and - pins at the bottom left) is used for the low-frequency portion of the input signal and corrects the op amp's input offset voltage. Both inputs are added together internally.

The auxiliary amplifier, chopper input switches and chopper output switches provide a high DC gain to the input signal. DC errors are modulated to higher frequencies, while white noise is modulated to a low frequency.

The low-pass filter reduces high-frequency content, including harmonics of the chopping clock.

The output buffer drives external loads at the $V_{OUT}$ pin ($V_{REF}$ is an internal reference voltage).

The oscillator runs at $f_{OSC1}$ = 200 kHz. Its output is divided by two, to produce the chopping clock rate of $f_{CHOP}$ = 100 kHz.

The internal Power-on Reset (POR) starts the part in a known good state, protecting against power supply brown-outs.

The digital control block controls switching and POR events.

#### 4.1.2 CHOPPING ACTION

Figure 4-2 shows the amplifier connections for the first phase of the chopping clock and Figure 4-3 shows the connections for the second phase. Its slow voltage errors alternate in polarity, making the average error small.

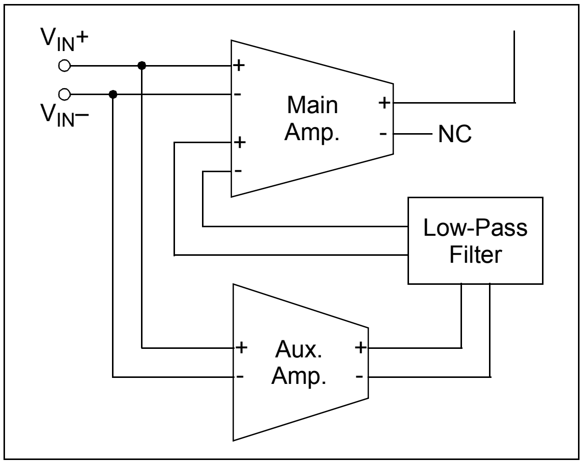


**FIGURE 4-2:** *First Chopping Clock Phase; Equivalent Amplifier Diagram.*

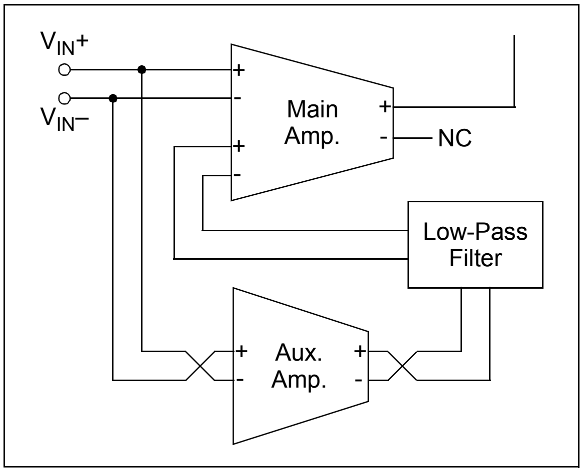


**FIGURE 4-3:** *Second Chopping Clock Phase; Equivalent Amplifier Diagram.*

### 4.1.3 INTERMODULATION DISTORTION (IMD)

These op amps will show intermodulation distortion (IMD) products when an AC signal is present.

The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the zero-drift circuitry's nonlinear response to produce IMD tones at sum and difference frequencies. Each of the square wave clock's harmonics has a series of IMD tones centered on it (see Figures 2-39 and 2-40).

## 4.2 Other Functional Blocks

### 4.2.1 RAIL-TO-RAIL INPUTS

The input stage of the MCP6V81/1U op amps uses two differential CMOS input stages in parallel. One operates at low common-mode input voltage ($V_{CM}$, which is approximately equal to $V_{IN}+$ and $V_{IN}-$ in normal operation), and the other operates at high $V_{CM}$. With this topology, the input operates with $V_{CM}$ up to $V_{DD}$ + 0.3V and down to $V_{SS}$ – 0.2V, at +25°C (see Figure 2-19). The input offset voltage ($V_{OS}$) is measured at $V_{CM} = V_{SS}$ – 0.2V and $V_{DD}$ + 0.3V to ensure proper operation.

#### 4.2.1.1 Phase Reversal

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-45 shows an input voltage exceeding both supplies with no phase inversion.

#### 4.2.1.2 Input Voltage Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). This requirement is independent of the input current limits discussed later on.

The ESD protection on the inputs can be depicted as shown in Figure 4-4. This structure was chosen to protect the input transistors against many (but not all) overvoltage conditions and to minimize input bias current ($I_B$).

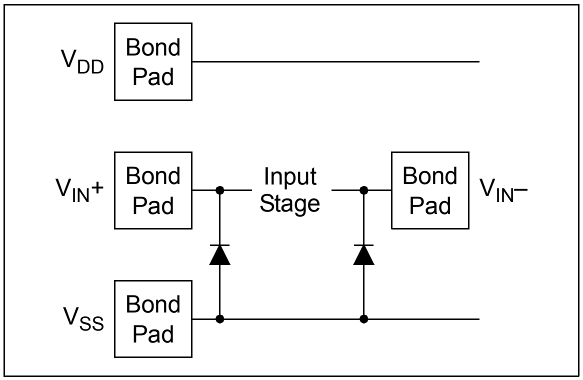


***FIGURE 4-4:*** *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below $V_{SS}$. They also clamp any voltages well above $V_{DD}$; their breakdown voltage is high enough to allow normal operation but not low enough to protect against slow overvoltage (beyond $V_{DD}$) events. Very fast ESD events (that meet the specification) are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs; Figure 4-5 shows one approach to protecting these inputs. $D_1$ and $D_2$ may be small signal silicon diodes, Schottky diodes for lower clamping voltages or diode-connected FETs for low leakage.

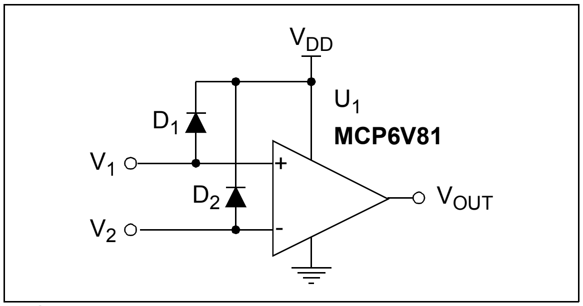
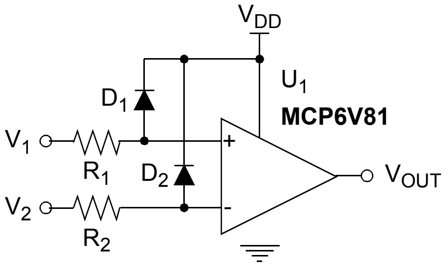


***FIGURE 4-5:*** *Protecting the Analog Inputs Against High Voltages.*

#### 4.2.1.3 Input Current Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). This requirement is independent of the voltage limits discussed previously.

Figure 4-6 shows one approach to protecting these inputs. The $R_1$ and $R_2$ resistors limit the possible current in or out of the input pins (and into $D_1$ and $D_2$). The diode currents will dump onto $V_{DD}$.



$$min(R_1, R_2) > \frac{V_{SS} - min(V_1, V_2)}{2\ mA}$$

$$min(R_1, R_2) > \frac{max(V_1, V_2) - V_{DD}}{2\ mA}$$

***FIGURE 4-6:*** *Protecting the Analog Inputs Against High Currents.*

It is also possible to connect the diodes to the left of the $R_1$ and $R_2$ resistors. In this case, the currents through the $D_1$ and $D_2$ diodes need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins ($V_{IN}+$ and $V_{IN}-$) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common-mode input voltage ($V_{CM}$) is below ground ($V_{SS}$) (see Figure 2-18).

### 4.2.2 RAIL-TO-RAIL OUTPUT

The output voltage range of the MCP6V81/1U zero-drift op amps is $V_{DD}$ – 5 mV (typical) and $V_{SS}$ + 5 mV (typical) when $R_L = 10\ k\Omega$ is connected to $V_{DD}/2$ and $V_{DD} = 5.5V$. Refer to Figures 2-20 and 2-21 for more information.

This op amp is designed to drive light loads; use another amplifier to buffer the output from heavy loads.

## 4.3 Application Tips

### 4.3.1 INPUT OFFSET VOLTAGE OVER TEMPERATURE

Table 1-1 gives both the linear and quadratic temperature coefficients ($TC_1$ and $TC_2$) of input offset voltage. The input offset voltage, at any temperature in the specified range, can be calculated as follows:

**EQUATION 4-1:**

$$V_{OS}(T_A) = V_{OS} + TC_1 \Delta T + TC_2 \Delta T^2$$

Where:

$\Delta T$ = $T_A$ – 25°C
$V_{OS}(T_A)$ = Input offset voltage at $T_A$
$V_{OS}$ = Input offset voltage at +25°C
$TC_1$ = Linear temperature coefficient
$TC_2$ = Quadratic temperature coefficient

### 4.3.2 DC GAIN PLOTS

Figures 2-10 to 2-12 are histograms of the reciprocals (in units of µV/V) of CMRR, PSRR and $A_{OL}$, respectively. They represent the change in input offset voltage ($V_{OS}$) with a change in common-mode input voltage ($V_{CM}$), power supply voltage ($V_{DD}$) and output voltage ($V_{OUT}$). The histograms are based on data taken with the production test equipment and the results reflect the trade-off between accuracy and test time. The actual performance of the devices is typically higher than shown in Figures 2-10 to 2-12.

The $1/A_{OL}$ histogram is centered near 0 µV/V because the measurements are dominated by the op amp's input noise. The negative values shown represent noise and tester limitations, *not* unstable behavior. Production tests make multiple $V_{OS}$ measurements, which validates an op amp's stability; an unstable part would show greater $V_{OS}$ variability or the output would stick at one of the supply rails.

### 4.3.3 OFFSET AT POWER-UP

When these parts power up, the input offset ($V_{OS}$) starts at its uncorrected value (usually less than ±5 mV). Circuits with high DC gain can cause the output to reach one of the two rails. In this case, the time to a valid output is delayed by an output overdrive time (like $t_{ODR}$) in addition to the start-up time (like $t_{STR}$).

It can be simple to avoid this extra start-up time. Reducing the gain is one method. Adding a capacitor across the feedback resistor ($R_F$) is another method.

### 4.3.4 SOURCE RESISTANCES

The input bias currents have two significant components: switching glitches that dominate at room temperature and below, and input ESD diode leakage currents that dominate at +85°C and above.

Make the resistances seen by the inputs small and equal. This minimizes the output offset caused by the input bias currents.

The inputs should see a resistance on the order of 10Ω to 1 kΩ at high frequencies (i.e., above 1 MHz). This helps minimize the impact of switching glitches, which are very fast, on overall performance. In some cases, it may be necessary to add resistors in series with the inputs to achieve this improvement in performance.

Small input resistances may be needed for high gains. Without them, parasitic capacitances might cause positive feedback and instability.

### 4.3.5 SOURCE CAPACITANCE

The capacitances seen by the two inputs should be small. Large input capacitances and source resistances, together with high gain, can lead to positive feedback and instability.

### 4.3.6 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. These zero-drift op amps have a different output impedance than most op amps, due to their unique topology.

When driving a capacitive load with these op amps, a series resistor at the output ($R_{ISO}$ in Figure 4-7) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

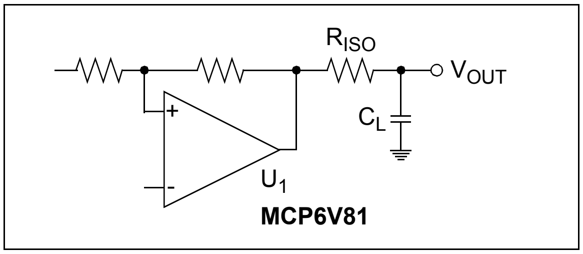


***FIGURE 4-7:*** *Output Resistor, $R_{ISO}$, Stabilizes Capacitive Loads.*

Figure 4-8 gives recommended $R_{ISO}$ values for different capacitive loads and gains. The x-axis is the load capacitance ($C_L$). The y-axis is the resistance ($R_{ISO}$).

$G_N$ is the circuit's noise gain. For non-inverting gains, $G_N$ and the Signal Gain are equal. For inverting gains, $G_N$ is 1+|Signal Gain| (e.g., -1 V/V gives $G_N$ = +2 V/V).

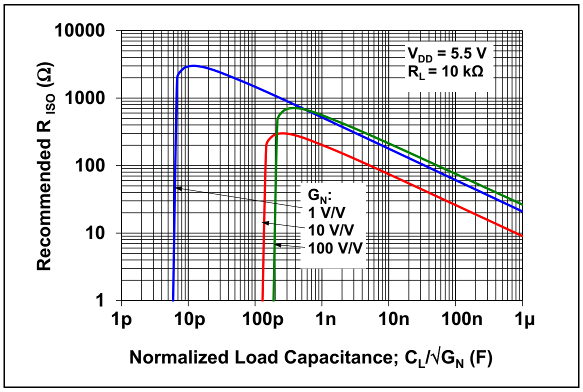


***FIGURE 4-8:*** *Recommended $R_{ISO}$ values for Capacitive Loads.*

After selecting $R_{ISO}$ for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify the $R_{ISO}$ value until the response is reasonable. Bench evaluation is helpful.

### 4.3.7 STABILIZING OUTPUT LOADS

This family of zero-drift op amps has an output impedance that has a double zero when the gain is low (see Figures 2-32 and 2-33). This can cause a large phase shift in feedback networks that have low-impedance near the part's bandwidth. This large phase shift can cause stability problems.

Figure 4-9 shows that the load on the output is $(R_L + R_{ISO})||(R_F + R_G)$, where $R_{ISO}$ is before the load (like Figure 4-7). This load needs to be large enough to maintain stability; it should be at least 10 kΩ.

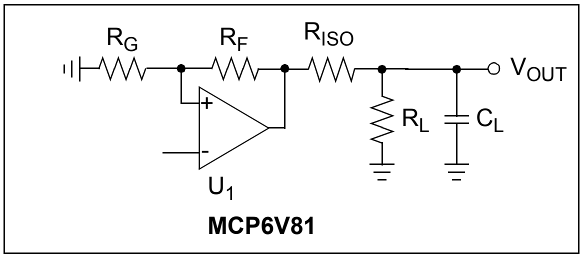


***FIGURE 4-9:*** *Output Load.*

### 4.3.8 GAIN PEAKING

Figure 4-10 shows an op amp circuit that represents non-inverting amplifiers ($V_M$ is a DC voltage and $V_P$ is the input) or inverting amplifiers ($V_P$ is a DC voltage and $V_M$ is the input). The $C_N$ and $C_G$ capacitances represent the total capacitance at the input pins; they include the op amp's common-mode input capacitance ($C_{CM}$), board parasitic capacitance and any capacitor placed in parallel. The $C_{FP}$ capacitance represents the parasitic capacitance coupling the output and non-inverting input pins.

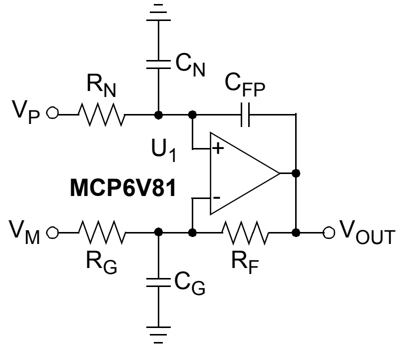


***FIGURE 4-10:*** *Amplifier with Parasitic Capacitance.*

$C_G$ acts in parallel with $R_G$ (except for a gain of +1 V/V), which causes an increase in gain at high frequencies. $C_G$ also reduces the phase margin of the feedback loop, which becomes less stable. This effect can be reduced by reducing either $C_G$ or $R_F||R_G$.

$C_N$ and $R_N$ form a low-pass filter that affects the signal at $V_P$. This filter has a single real pole at $1/(2\pi R_N C_N)$.

The largest value of $R_F$ that should be used depends on noise gain (see $G_N$ in **Section 4.3.6 "Capacitive Loads"**), $C_G$ and the open-loop gain's phase shift. An approximate limit for $R_F$ is:

**EQUATION 4-2:**

$$R_F \leq 10\,k\Omega \times \frac{3.5\,pF}{C_G} \times G_N^2$$

Some applications may modify these values to reduce either output loading or gain peaking (step-response overshoot).

At high gains, $R_N$ needs to be small in order to prevent positive feedback and oscillations. Large $C_N$ values can also help.

### 4.3.9 REDUCING UNDESIRED NOISE AND SIGNALS

Reduce undesired noise and signals with:

- Low-bandwidth signal filters:
  - Minimize random analog noise
  - Reduce interfering signals
- Good PCB layout techniques:
  - Minimize crosstalk
  - Minimize parasitic capacitances and inductances that interact with fast-switching edges
- Good power supply design:
  - Isolation from other parts
  - Filtering of interference on supply line(s)

### 4.3.10 SUPPLY BYPASSING AND FILTERING

With this family of operational amplifiers, the power supply pin ($V_{DD}$ for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm of the pin for good high-frequency performance.

These parts also need a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other low-noise analog parts.

In some cases, high-frequency power supply noise (e.g., switched mode power supplies) may cause undue intermodulation distortion with a DC offset shift; this noise needs to be filtered. Adding a small resistor into the supply connection can be helpful.

### 4.3.11 PCB DESIGN FOR DC PRECISION

In order to achieve DC precision on the order of ±1 µV, many physical errors need to be minimized. The design of the Printed Circuit Board (PCB), the wiring and the thermal environment have a strong impact on the precision achieved. A poor PCB design can easily be more than 100 times worse than the MCP6V81/1U op amps' minimum and maximum specifications.

#### 4.3.11.1 PCB Layout

Any time two dissimilar metals are joined together, a temperature-dependent voltage appears across the junction (the Seebeck or thermojunction effect). This effect is used in thermocouples to measure temperature. The following are examples of thermojunctions on a PCB:

- Components (resistors, op amps, …) soldered to a copper pad
- Wires mechanically attached to the PCB
- Jumpers
- Solder joints
- PCB vias

Typical thermojunctions have temperature-to-voltage conversion coefficients of 1 to 100 µV/°C (sometimes higher).

Microchip's AN1258 "*Op Amp Precision Design: PCB Layout Techniques*" (DS01258) contains in-depth information on PCB layout techniques that minimize thermojunction effects. It also discusses other effects, such as crosstalk, impedances, mechanical stresses and humidity.

#### 4.3.11.2 Crosstalk

DC crosstalk causes offsets that appear as a larger input offset voltage. Common causes include:

- Common-mode noise (remote sensors)
- Ground loops (current return paths)
- Power supply coupling

Interference from the mains (usually 50 Hz or 60 Hz) and other AC sources can also affect the DC performance. Nonlinear distortion can convert these signals to multiple tones, including a DC shift in voltage. When the signal is sampled by an ADC, these AC signals can also be aliased to DC, causing an apparent shift in offset.

To reduce interference:

- Keep traces and wires as short as possible
- Use shielding
- Use ground plane (at least a star ground)
- Place the input signal source near the DUT
- Use good PCB layout techniques
- Use a separate power supply filter (bypass capacitors) for these zero-drift op amps

#### 4.3.11.3 Miscellaneous Effects

Keep the resistances seen by the input pins as small and as near to equal as possible, to minimize bias current-related offsets.

Make the (trace) capacitances seen by the input pins small and equal. This is helpful in minimizing switching glitch-induced offset voltages.

Bending a coax cable with a radius that is too small causes a small voltage drop to appear on the center conductor (the triboelectric effect). Make sure the bending radius is large enough to keep the conductors and insulation in full contact.

Mechanical stresses can make some capacitor types (such as some ceramics) output small voltages. Use more appropriate capacitor types in the signal path and minimize mechanical stresses and vibration.

Humidity can cause electrochemical potential voltages to appear in a circuit. Proper PCB cleaning helps, as does the use of encapsulants.

## 4.4 Typical Applications

### 4.4.1 WHEATSTONE BRIDGE

Many sensors are configured as Wheatstone bridges. Strain gauges and pressure sensors are two common examples. These signals can be small and the common-mode noise large. Amplifier designs with high differential gain are desirable.

Figure 4-11 shows how to interface to a Wheatstone bridge with a minimum of components. Because the circuit is not symmetric, the ADC input is single-ended and there is a minimum of filtering; the CMRR is good enough for moderate common-mode noise.

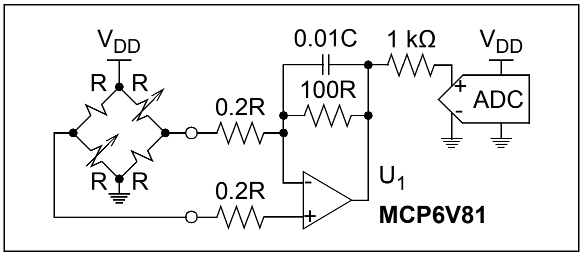


***FIGURE 4-11:*** *Simple Design.*

### 4.4.2 RTD SENSOR

The ratiometric circuit in Figure 4-12 conditions a two-wire RTD for applications with a limited temperature range. $U_1$ acts as a difference amplifier with a low-frequency pole. The sensor's wiring resistance ($R_W$) is corrected in firmware. Failure (open) of the RTD is detected by an out-of-range voltage.

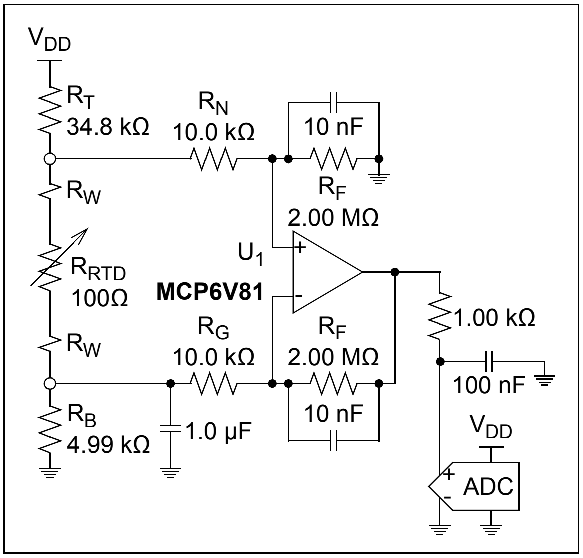


***FIGURE 4-12:*** *RTD Sensor.*

### 4.4.3 OFFSET VOLTAGE CORRECTION

Figure 4-13 shows MCP6V81 ($U_2$) correcting the input offset voltage of another op amp ($U_1$). $R_2$ and $C_2$ integrate the offset error seen at $U_1$'s input. The integration needs to be slow enough to be stable (with the feedback provided by $R_1$ and $R_3$). $R_4$ and $R_5$ attenuate the integrator's output. This shifts the integrator pole down in frequency.

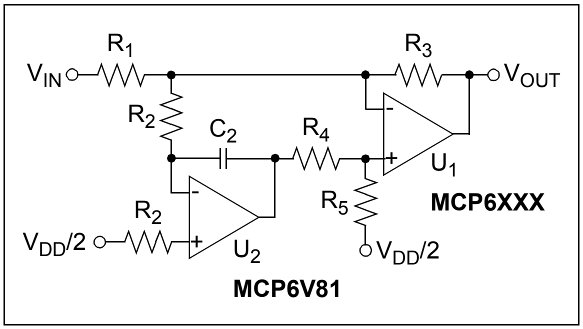


**FIGURE 4-13:** *Offset Correction.*

### 4.4.4 PRECISION COMPARATOR

Use high gain before a comparator to improve the latter's performance. Do not use MCP6V81/1U as a comparator by itself; the $V_{OS}$ correction circuitry does not operate properly without a feedback loop.

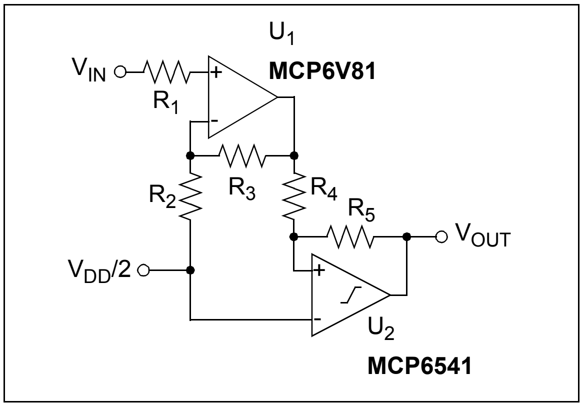


**FIGURE 4-14:** *Precision Comparator.*

NOTES:

## 5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6V81/1U family of op amps.

### 5.1 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

### 5.2 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

### 5.3 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analog tools.

Some boards that are especially useful are:

- MCP6V01 Thermocouple Auto-Zeroed Reference Design (P/N MCP6V01RD-TCPL)
- MCP6XXX Amplifier Evaluation Board 1 (P/N DS51667)
- MCP6XXX Amplifier Evaluation Board 2 (P/N DS51668)
- MCP6XXX Amplifier Evaluation Board 3 (P/N DS51673)
- MCP6XXX Amplifier Evaluation Board 4 (P/N DS51681)
- Active Filter Demo Board Kit (P/N DS51614)
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board (P/N SOIC8EV)
- 14-Pin SOIC/TSSOP/DIP Evaluation Board (P/N SOIC14EV)

### 5.4 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

**ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits"* (DS21821)

**AN722:** *"Operational Amplifier Topologies and DC Specifications"* (DS00722)

**AN723:** *"Operational Amplifier AC Specifications and Applications"* (DS00723)

**AN884:** *"Driving Capacitive Loads With Op Amps"* (DS00884)

**AN990:** *"Analog Sensor Conditioning Circuits – An Overview"* (DS00990)

**AN1177:** *"Op Amp Precision Design: DC Errors"* (DS01177)

**AN1228:** *"Op Amp Precision Design: Random Noise*" (DS01228)

**AN1258:** *"Op Amp Precision Design: PCB Layout Techniques"* (DS01258)

**AN1767:** *"Solutions for Radio Frequency Electromagnetic Interference in Amplifier Circuits"* (DS01767A)

These Application Notes and others are listed in the design guide:

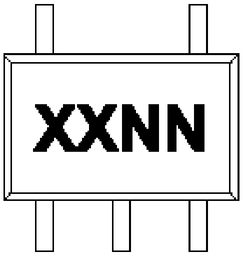
*"Signal Chain Design Guide"* (DS21825)

NOTES:

## 6.0 PACKAGING INFORMATION

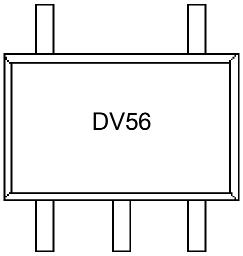
### 6.1 Package Marking Information

5-Lead SC70 (**MCP6V81U**)

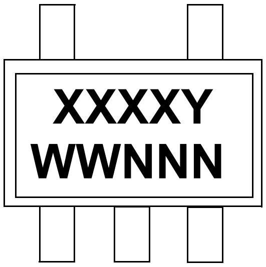


| Device | Code |
|---|---|
| MCP6V81UT-E/LTY | DVNN |

Example

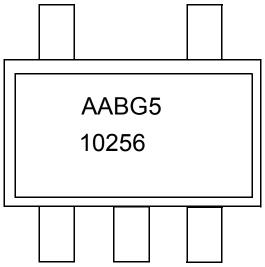


5-Lead SOT-23 **(MCP6V81, MCP6V81U)**



| Device | Code |
|---|---|
| MCP6V81T-E/OT | AABGY |
| MCP6V81UT-E/OT | AABHY |

Example

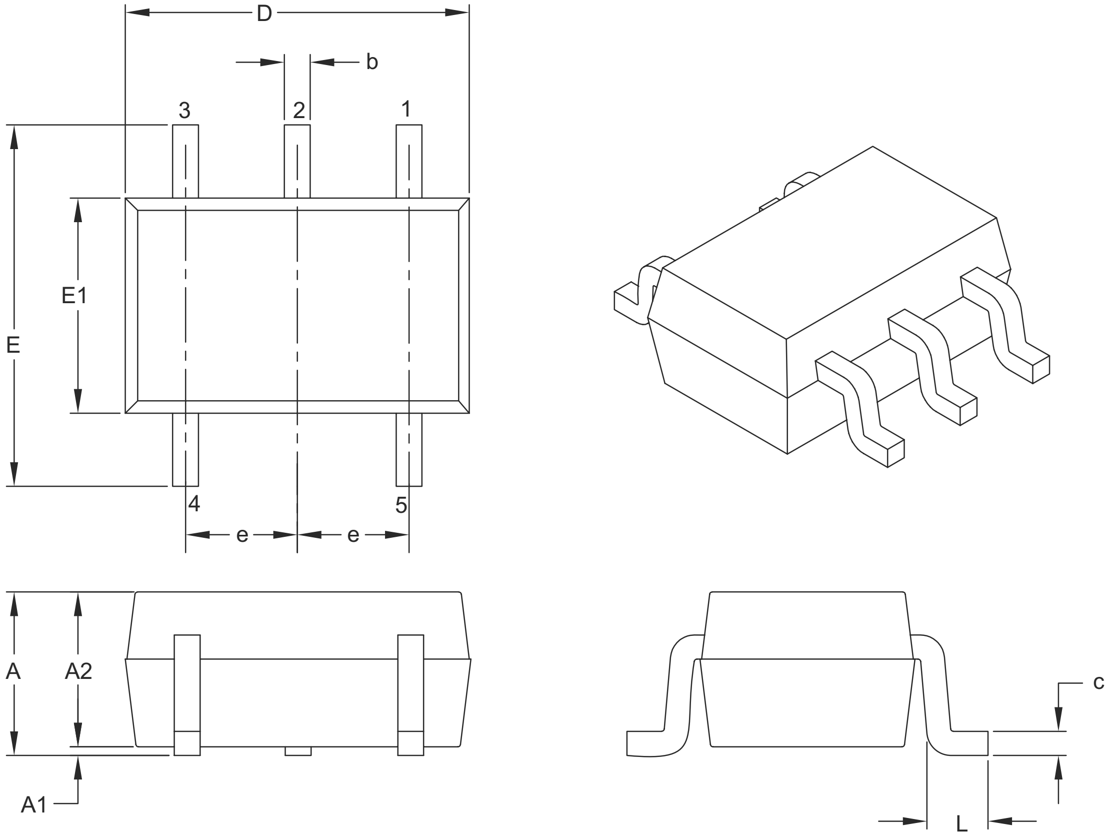


| **Legend:** | | |
|---|---|---|
| | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | ⓔ3 | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 5-Lead Plastic Small Outine Transistor (LTY) [SC70]

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 5 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | – | 1.10 |
| Molded Package Thickness | A2 | 0.80 | – | 1.00 |
| Standoff | A1 | 0.00 | – | 0.10 |
| Overall Width | E | 1.80 | 2.10 | 2.40 |
| Molded Package Width | E1 | 1.15 | 1.25 | 1.35 |
| Overall Length | D | 1.80 | 2.00 | 2.25 |
| Foot Length | L | 0.10 | 0.20 | 0.46 |
| Lead Thickness | c | 0.08 | – | 0.26 |
| Lead Width | b | 0.15 | – | 0.40 |

**Notes:**

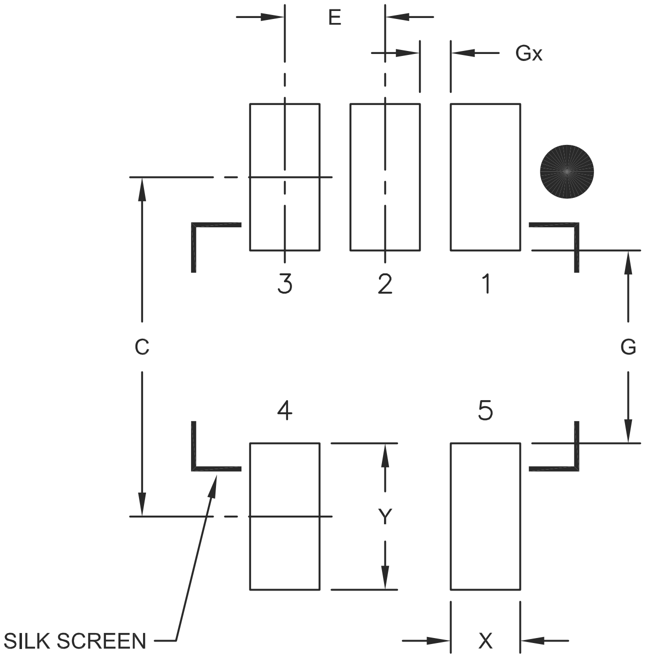
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

### 5-Lead Plastic Small Outine Transistor (LTY) [SC70]

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|



RECOMMENDED LAND PATTERN

| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| | Dimension Limits | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 2.20 | |
| Contact Pad Width | X | | | 0.45 |
| Contact Pad Length | Y | | | 0.95 |
| Distance Between Pads | G | 1.25 | | |
| Distance Between Pads | Gx | 0.20 | | |

Notes:

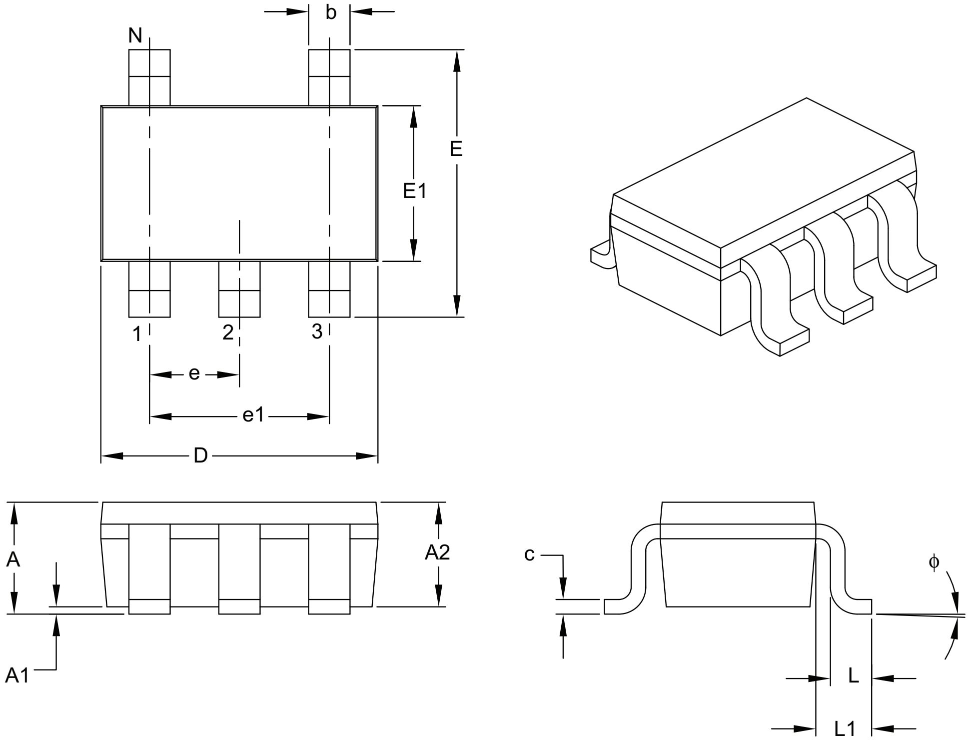
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

## 5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 5 | | |
| Lead Pitch | e | 0.95 BSC | | |
| Outside Lead Pitch | e1 | 1.90 BSC | | |
| Overall Height | A | 0.90 | – | 1.45 |
| Molded Package Thickness | A2 | 0.89 | – | 1.30 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | 2.20 | – | 3.20 |
| Molded Package Width | E1 | 1.30 | – | 1.80 |
| Overall Length | D | 2.70 | – | 3.10 |
| Foot Length | L | 0.10 | – | 0.60 |
| Footprint | L1 | 0.35 | – | 0.80 |
| Foot Angle | ϕ | 0° | – | 30° |
| Lead Thickness | c | 0.08 | – | 0.26 |
| Lead Width | b | 0.20 | – | 0.51 |

**Notes:**

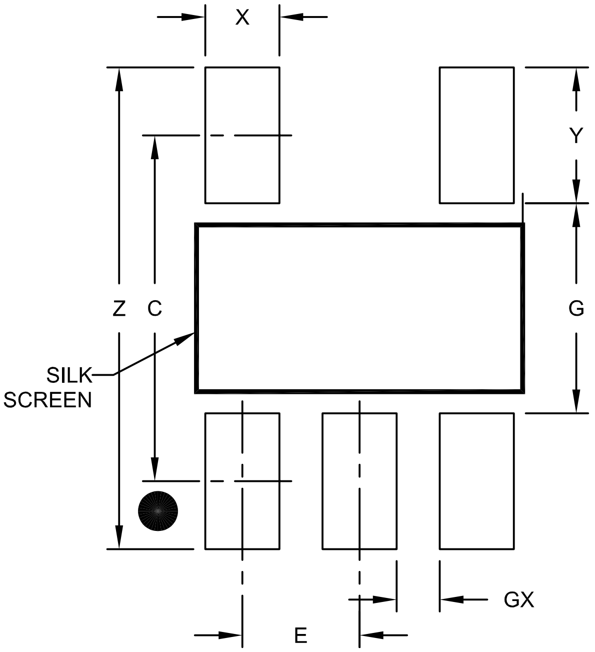
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

## 5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.95 BSC | | |
| Contact Pad Spacing | C | | 2.80 | |
| Contact Pad Width (X5) | X | | | 0.60 |
| Contact Pad Length (X5) | Y | | | 1.10 |
| Distance Between Pads | G | 1.70 | | |
| Distance Between Pads | GX | 0.35 | | |
| Overall Width | Z | | | 3.90 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

**NOTES:**

## APPENDIX A: REVISION HISTORY

### Revision A (June 2015)

- Original Release of this Document.

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | [X][1] | –X | /XX |
|---|---|---|---|
| **Device** | **Tape and Reel** | **Temperature Range** | **Package** |

| | | |
|---|---|---|
| **Device:** | MCP6V81T: | Single Op Amp (Tape and Reel) (SOT-23 only) |
| | MCP6V81UT: | Single Op Amp (Tape and Reel) (SC-70, SOT-23) |
| **Temperature Range:** | E | = -40°C to +125°C (Extended) |
| **Package:** | LTY* | = Plastic Small Outline Transistor, SC-70, 5-lead |
| | OT | = Plastic Small Outline Transistor, SOT-23, 5-lead |
| | *Y | = Nickel palladium gold manufacturing designator. Only available on the SC70 package. |

**Examples:**

| | | |
|---|---|---|
| a) | MCP6V81T-E/OT: | Tape and Reel,<br>Extended temperature,<br>5LD SOT-23 package |
| a) | MCP6V81UT-E/LTY: | Tape and Reel<br>Extended temperature,<br>5LD SC70 package |
| b) | MCP6V81UT-E/OT: | Tape and Reel,<br>Extended temperature,<br>5LD SOT-23 package |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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