

PIC18(L)F26/46K22 Rev. A2/A4 Silicon Errata and Data Sheet Clarification

The PIC18(L)F26/46K22 family devices that you have received conform functionally to the current Device Data Sheet (DS41412E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC18(L)F26/46K22 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICKit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICKit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F26/46K22 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾	
		A2	A4
PIC18F46K22	0101 0100 000x xxxx	0 0010	0 0100
PIC18LF46K22	0101 0100 001x xxxx	0 0010	0 0100
PIC18F26K22	0101 0100 010x xxxx	0 0010	0 0100
PIC18LF26K22	0101 0100 011x xxxx	0 0010	0 0100

- Note 1:** The Device ID is located in the last configuration memory space.
- Note 2:** Refer to the "PIC18(L)F2XK22/4XK22 Flash Memory Programming Specification" (DS41398) for detailed information on Device and Revision IDs for your specific device.

PIC18(L)F26/46K22

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A2	A4
Comparators	CxSYNC Control	1.	The comparator output to the device pin (Cx) always bypasses the Timer1 synchronization latch.	X	X
Clock Switching	Fail-Safe Clock Monitor	2.	When the FCMEN Configuration bit is set and the IESO Configuration bit is not set, then a clock failure during Sleep will not be detected.	X	X
Power-on Reset (POR)	Power-on Reset	3.	Transient current spikes on some parts during power-up may cause the part to become stuck in Reset.	X	
Timer1/3/5 Gate	Timer1/3/5 Gate	4.	The Timer1/3/5 gate times cannot be resolved to the two Least Significant bits, when using Fosc as the Timer1/3/5 source.	X	X
EUSART	EUSART Asynchronous Operation	5.	The EUSART asynchronous operation may miss the Start bit edge.	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Comparators

The CxSYNC controls are inoperative. The comparator output (Cx) always bypasses the Timer1 synchronization latch.

Work around

None.

Affected Silicon Revisions

A2	A4						
X	X						

2. Module: Clock Switching

When the FCMEN Configuration bit is set and the IESO Configuration bit is not set, then a clock failure during Sleep will not be detected.

Work around

The IESO Configuration bit must also be set when the FCMEN Configuration bit is set.

Affected Silicon Revisions

A2	A4						
X	X						

3. Module: Power-on Reset (POR)

There may be transient current spikes on some parts during power-up. If the application cannot supply enough current to get past these transients, then the part may become stuck in Reset.

Work around

Ensure that the application is capable of supplying at least 30 mA of transient current during power-up.

Affected Silicon Revisions

A2	A4						
X							

4. Module: Timer1/3/5 Gate

The Timer gate times cannot be resolved to the two Least Significant timer bits when the source frequency is FOSC (TMRxCS[1:0]=01). This is because the gate edges are synchronized with the FOSC/4 clock.

Work around

None.

Affected Silicon Revisions

A2	A4						
X	X						

5. Module: EUSART

The EUSART asynchronous operation has a probability of 1 in 256 of missing the Start bit edge for all combinations of BRGH and BRG16 values, other than BRGH = 1, BRG16 = 1.

Work around

Set BRGH = 1, and BRG16 = 1 and use this baud rate formula:

$$Baud_Rate = Fosc / [4([SPBRGH:SPBRGL]+1)]$$

Affected Silicon Revisions

A2	A4						
X							

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41412E):

<p>Note: Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.</p>

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (8/2010)

Initial release of this document.

Rev B Document (7/2011)

Updated for Revision A4 silicon release; Module 3.1 errata fixed; Other minor corrections.

Data Sheet Clarifications: No changes.

Rev C Document (8/2011)

Added Module 5, EUSART; Module 5 errata fixed on Silicon revision A4.

Data Sheet Clarifications: No changes.

Rev D Document (2/2012)

Removed Module 3.2; Other minor corrections.

Data Sheet Clarifications: Removed Module 1.

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NOTES:

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