KSZ8051MNL/RNL

10Base-T/100Base-TX Physical Layer Transceiver

General Description

The KSZ8051 is a single supply 10Base-T/100Base-TX Ethernet physical layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8051 is a highly integrated, compact solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low noise regulator to supply the 1.2V core.

The KSZ8051MNL offers the Media Independent Interface (MII) and the KSZ8051RNL offers the Reduced Media Independent Interface (RMII) for direct connection with MII/ RMII compliant Ethernet MAC processors and switches.

A 25MHz crystal is used to generate all required clocks, including the 50MHz RMII reference clock output for the KSZ8051RNL.

The KSZ8051 provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ8051 I/Os and board. Micrel LinkMD® TDR-based cable diagnostics permit identification of faulty copper cabling.

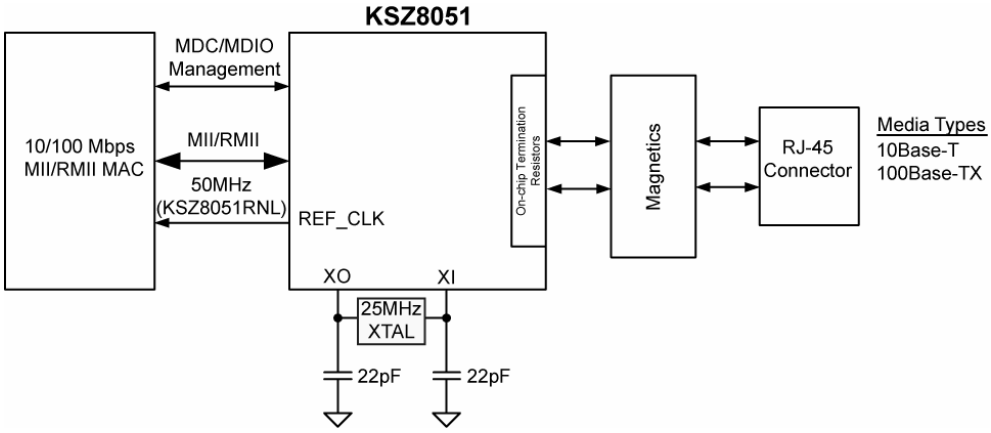
The KSZ8051MNL and KSZ8051RNL are available in 32-pin, lead-free QFN packages (See Ordering Information).

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Single-chip 10Base-T/100Base-TX IEEE 802.3 compliant Ethernet Transceiver
- MII Interface support (KSZ8051MNL)
- RMII v1.2 Interface support with 50MHz reference clock output to MAC, and option to input 50MHz reference clock (KSZ8051RNL)
- Back-to-Back mode support for 100Mbps copper repeater or media converter
- MDC/MDIO Management Interface for PHY register configuration
- Programmable interrupt output
- LED outputs for link, activity and speed status indication
- On-chip termination resistors for the differential pairs
- Baseline Wander Correction
- HP Auto MDI/MDI-X for reliable detection and correction for straight-through and crossover cables with disable and enable option
- Auto-negotiation to automatically select the highest link up speed (10/100 Mbps) and duplex (half/full)
- Power down and power saving modes
- LinkMD® TDR-based cable diagnostics for identification of faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and board.

Functional Diagram



More Features

- Loopback modes for diagnostics
- Single 3.3V power supply with VDD I/O options for 1.8V, 2.5V, or 3.3V
- Built-in 1.2V regulator for core
- Available in 32-pin (5mm x 5mm) QFN package

Applications

- Game Console
- IP Phone
- IP Set-top Box
- IP TV
- LOM
- Printer

Ordering Information

Part Number	Temp. Range	Package	Lead Finish	Description
KSZ8051MNL	0°C to 70°C	32-Pin QFN	Pb-Free	MII, Commercial Temperature
KSZ8051MNLI (1)	-40°C to 85°C	32-Pin QFN	Pb-Free	MII, Industrial Temperature
KSZ8051RNL	0°C to 70°C	32-Pin QFN	Pb-Free	RMII, Commercial Temperature
KSZ8051RNLI (1)	-40°C to 85°C	32-Pin QFN	Pb-Free	RMII, Industrial Temperature

Note:

1. Contact factory for lead time.

Revision History

Revision	Date	Summary of Changes
1.0	6/22/10	Data sheet created.

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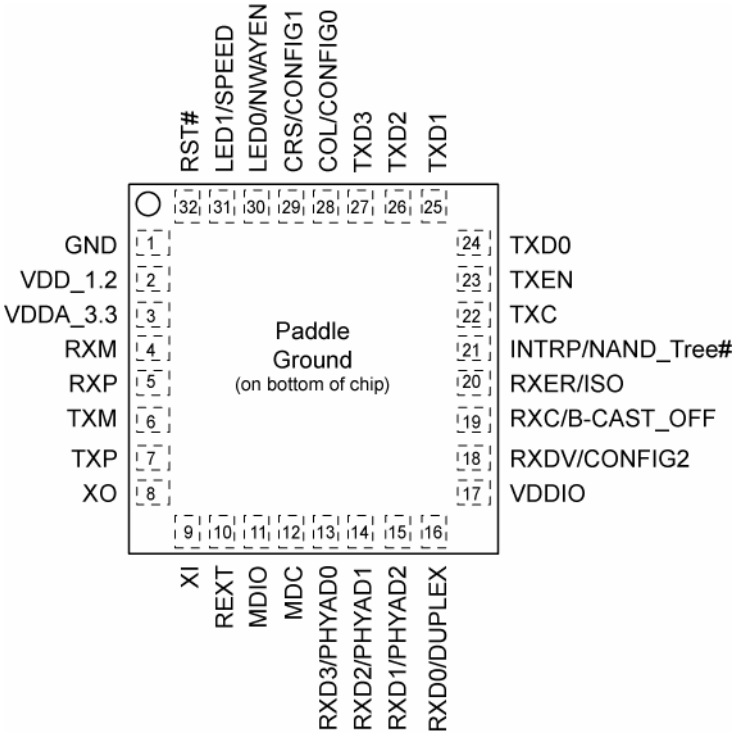
Pin Configuration – KSZ8051MNL



32-Pin (5mm x 5mm) QFN

Pin Description – KSZ8051MNL

Pin Number	Pin Name	Type[1]	Pin Function
1	GND	Gnd	Ground
2	VDD_1.2	P	1.2V core V_{DD} (power supplied by KSZ8051MNL) Decouple with 2.2uF and 0.1uF capacitors to ground.
3	VDDA_3.3	P	3.3V analog V_{DD}
4	RXM	I/O	Physical receive or transmit signal (- differential)
5	RXP	I/O	Physical receive or transmit signal (+ differential)
6	TXM	I/O	Physical transmit or receive signal (- differential)
7	TXP	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal feedback – for 25 MHz crystal This pin is a no connect if oscillator or external clock source is used.
9	XI	I	Crystal / Oscillator / External Clock Input 25MHz +/-50ppm
10	REXT	I	Set physical transmit output current Connect a 6.49KΩ resistor to ground on this pin.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This clock pin is synchronous to the MDIO data pin.
13	RXD3 / PHYAD0	Ipu/O	MII Mode: MII Receive Data Output[3][2] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See “Strapping Options” section for details.
14	RXD2 / PHYAD1	Ipd/O	MII Mode: MII Receive Data Output[2][2] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See “Strapping Options” section for details.
15	RXD1 / PHYAD2	Ipd/O	MII Mode: MII Receive Data Output[1][2] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See “Strapping Options” section for details.
16	RXD0 / DUPLEX	Ipu/O	MII Mode: MII Receive Data Output[0][2] / Config Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See “Strapping Options” section for details.
17	VDDIO	P	3.3V, 2.5V or 1.8V digital V_{DD}
18	RXDV / CONFIG2	Ipd/O	MII Mode: MII Receive Data Valid Output / Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See “Strapping Options” section for details.
19	RXC / B-CAST_OFF	Ipd/O	MII Mode: MII Receive Clock Output Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See “Strapping Options” section for details.
20	RXER / ISO	Ipd/O	MII Mode: MII Receive Error Output / Config Mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset. See “Strapping Options” section for details.
21	INTRP /	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td></td><td>NAND_Tree#</td><td></td><td>Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>22</td><td>TXC</td><td>I/O</td><td>MII Mode: MII Transmit Clock Output
MII Back-to-Back Mode: MII Transmit Clock Input</td></tr>
<tr><td>23</td><td>TXEN</td><td>I</td><td>MII Mode: MII Transmit Enable Input</td></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>MII Mode: MII Transmit Data Input[0](3)</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>MII Mode: MII Transmit Data Input[1](3)</td></tr>
<tr><td>26</td><td>TXD2</td><td>I</td><td>MII Mode: MII Transmit Data Input[2](3)</td></tr>
<tr><td>27</td><td>TXD3</td><td>I</td><td>MII Mode: MII Transmit Data Input[3](3)</td></tr>
<tr><td>28</td><td>COL /
CONFIG0</td><td>Ipd/O</td><td>MII Mode: MII Collision Detect Output /
Config Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>CRS /
CONFIG1</td><td>Ipd/O</td><td>MII Mode: MII Carrier Sense Output /
Config Mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>30</td><td>LED0 /
NWAYEN</td><td>Ipu/O</td><td>LED Output: Programmable LED0 Output /
Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) at the de-assertion of reset. See “Strapping Options” section for details.
The LED0 pin is programmable via register 1Fh bits [5:4], and is defined as follows.

<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

<table>
<tr><th colspan="3">LED mode = [01]</th></tr>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
</table>

LED mode = [10], [11] Reserved</td></tr>
<tr><td>31</td><td>LED1 /
SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output /
Config Mode: Latched as SPEED (register 0h, bit 13) at the de-assertion of reset. See “Strapping Options” section for details.
The LED1 pin is programmable via register 1Fh bits [5:4], and is defined as follows.
<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>10Base-T</td><td>High</td><td>OFF</td></tr>
<tr><td>100Base-TX</td><td>Low</td><td>ON</td></tr>
</table>

<table>
<tr><th colspan="3">LED mode = [01]</th></tr>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>High</td><td>OFF</td></tr>
</table>
</td></tr>
</table>

Pin Number	Pin Name	Type(1)	Pin Function
			Activity | Toggle | Blinking **LED mode = [10], [11]** Reserved
32	RST#	I	Chip Reset (active low)
PADDLE	GND	Gnd	Ground

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin with internal pull-up (see Electrical Characteristics for value) otherwise.
2. MII Rx Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC. RXD[3:0] is invalid data from the PHY when RXDV is de-asserted.
3. MII Tx Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] presents valid data from the MAC. TXD[3:0] has no effect on the PHY when TXEN is de-asserted.

Strapping Options – KSZ8051MNL

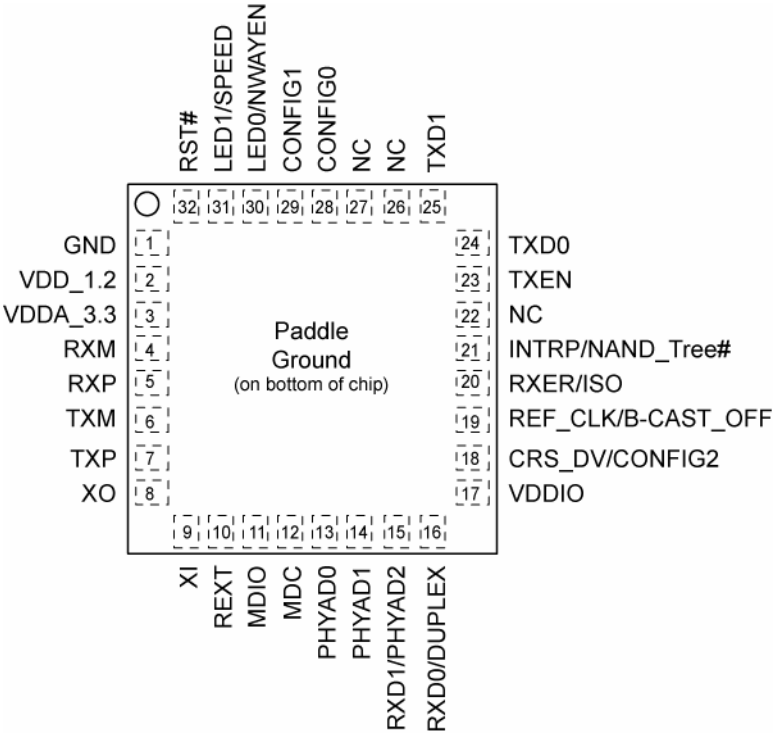
Pin Number	Pin Name	Type[1]	Pin Function
15 14 13	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at de-assertion of reset and is configurable to any value from 0 to 7. The default PHY Address is 00001. PHY Address 00000 is enabled only if the B-CAST_OFF strapping pin is pulled high. PHY Address bits [4:3] are set to '00' by default.
18 29 28	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset. **CONFIG[2:0]** / **Mode** 000 / MII (default) 110 / MII Back-to-Back 001 – 101, 111 / Reserved – not used
20	ISO	Ipd/O	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable At the de-assertion of reset, this pin value is latched into register 0h bit 10.
31	SPEED	Ipu/O	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps At the de-assertion of reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
16	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex At the de-assertion of reset, this pin value is latched into register 0h bit 8.
30	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation At the de-assertion of reset, this pin value is latched into register 0h bit 12.
19	B-CAST_OFF	Ipd/O	Broadcast Off – for PHY Address 0 Pull-up = PHY Address 0 is set as an unique PHY address Pull-down (default) = PHY Address 0 is set as a broadcast PHY address At the de-assertion of reset, this pin value is latched by the chip.
21	NAND_Tree#	Ipu/Opu	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable At the de-assertion of reset, this pin value is latched by the chip.

Note:

1. Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin with internal pull-up (see Electrical Characteristics for value) otherwise.

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the MII signals to be latched to the unintended high/low states. In this case, external pull-ups (4.7K) or pull-downs (1.0K) should be added on these PHY strap-in pins to ensure the intended values are strapped-in correctly.

Pin Configuration – KSZ8051RNL



32-Pin (5mm x 5mm) QFN

Pin Description – KSZ8051RNL

Pin Number	Pin Name	Type[1]	Pin Function
1	GND	Gnd	Ground
2	VDD_1.2	P	1.2V core V_{DD} (power supplied by KSZ8051RNL) Decouple with 2.2uF and 0.1uF capacitors to ground.
3	VDDA_3.3	P	3.3V analog V_{DD}
4	RXM	I/O	Physical receive or transmit signal (- differential)
5	RXP	I/O	Physical receive or transmit signal (+ differential)
6	TXM	I/O	Physical transmit or receive signal (- differential)
7	TXP	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal feedback – for 25 MHz crystal This pin is a no connect if oscillator or external clock source is used.
9	XI	I	25MHz Mode: 25MHz +/-50ppm Crystal / Oscillator / External Clock Input 50MHz Mode: 50MHz +/-50ppm Oscillator / External Clock Input
10	REXT	I	Set physical transmit output current Connect a 6.49KΩ resistor-to-ground on this pin.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This clock pin is synchronous to the MDIO data pin.
13	PHYAD0	Ipu/O	The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See “Strapping Options” section for details.
14	PHYAD1	Ipd/O	The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See “Strapping Options” section for details.
15	RXD1 / PHYAD2	Ipd/O	RMII Mode: RMII Receive Data Output[1][2] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See “Strapping Options” section for details.
16	RXD0 / DUPLEX	Ipu/O	RMII Mode: RMII Receive Data Output[0][2] / Config Mode: The pull-up/pull-down value is latched as DUPLEX at the de-assertion of reset. See “Strapping Options” section for details.
17	VDDIO	P	3.3V, 2.5V or 1.8V digital V_{DD}
18	CRS_DV / CONFIG2	Ipd/O	RMII Mode: RMII Carrier Sense/Receive Data Valid Output / Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See “Strapping Options” section for details.
19	REF_CLK / B-CAST_OFF	Ipd/O	RMII Mode: 25MHz Mode: This pin provides the 50MHz RMII reference clock output to the MAC. See also XI (pin 9). 50MHz Mode: This pin is a no connect. See also XI (pin 9). Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. See “Strapping Options” section for details.
20	RXER / ISO	Ipd/O	RMII Mode: RMII Receive Error Output / Config Mode: The pull-up/pull-down value is latched as ISOLATE at the de-assertion of reset. See “Strapping Options” section for details.
21	INTRP /	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td></td><td>NAND_Tree#</td><td></td><td>Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>22</td><td>NC</td><td>O</td><td>No connect- It is recommended to tie this unused pin directly to ground.</td></tr>
<tr><td>23</td><td>TXEN</td><td>I</td><td>RMII Transmit Enable Input</td></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>RMII Transmit Data Input[0](3)</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>RMII Transmit Data Input[1](3)</td></tr>
<tr><td>26</td><td>NC</td><td>I</td><td>No connect- It is recommended to tie this unused pin directly to ground.</td></tr>
<tr><td>27</td><td>NC</td><td>I</td><td>No connect- It is recommended to tie this unused pin directly to ground.</td></tr>
<tr><td>28</td><td>CONFIG0</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>CONFIG1</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See “Strapping Options” section for details.</td></tr>
<tr><td>30</td><td>LED0 / NWAYEN</td><td>Ipu/O</td><td>LED Output: Programmable LED0 Output /
Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) at the de-assertion of reset. See “Strapping Options” section for details.
The LED0 pin is programmable via register 1Fh bits [5:4], and is defined as follows.

<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>High</td><td>OFF</td></tr>
<tr><td>Link</td><td>Low</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
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<table>
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</table>

LED mode = [10], [11] Reserved</td></tr>
<tr><td>31</td><td>LED1 / SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output /
Config Mode: Latched as SPEED (register 0h, bit 13) at the de-assertion of reset. See “Strapping Options” section for details.
The LED1 pin is programmable via register 1Fh bits [5:4], and is defined as follows.

<table>
<tr><th colspan="3">LED mode = [00]</th></tr>
<tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>10Base-T</td><td>High</td><td>OFF</td></tr>
<tr><td>100Base-TX</td><td>Low</td><td>ON</td></tr>
</table>

<table>
<tr><th colspan="3">LED mode = [01]</th></tr>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>High</td><td>OFF</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

LED mode = [10], [11] Reserved</td></tr>
</table>

Pin Number	Pin Name	Type(1)	Pin Function
32	RST#	I	Chip Reset (active low)
PADDLE	GND	Gnd	Ground

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin with internal pull-up (see Electrical Characteristics for value) otherwise.
2. RMII Rx Mode: The RXD[1:0] bits are synchronous with the 50MHz RMII Reference Clock. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent by the PHY to the MAC.
3. RMII Tx Mode: The TXD[1:0] bits are synchronous with the 50MHz RMII Reference Clock . For each clock period in which TXEN is asserted, two bits of data are received by the PHY from the MAC.

Strapping Options – KSZ8051RNL

Pin Number	Pin Name	Type[1]	Pin Function
15 14 13	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at de-assertion of reset and is configurable to any value from 0 to 7. The default PHY Address is 00001. PHY Address 00000 is enabled only if the B-CAST_OFF strapping pin is pulled high. PHY Address bits [4:3] are set to '00' by default.
18 29 28	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset. **CONFIG[2:0]** / **Mode** 001 / RMII 101 / RMII Back-to-Back 000, 010 – 100, 110, 111 / Reserved – not used
20	ISO	Ipd/O	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable At the de-assertion of reset, this pin value is latched into register 0h bit 10.
31	SPEED	Ipu/O	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps At the de-assertion of reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
16	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex At the de-assertion of reset, this pin value is latched into register 0h bit 8.
30	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation At the de-assertion of reset, this pin value is latched into register 0h bit 12.
19	B-CAST_OFF	Ipd/O	Broadcast Off – for PHY Address 0 Pull-up = PHY Address 0 is set as an unique PHY address Pull-down (default) = PHY Address 0 is set as a broadcast PHY address At the de-assertion of reset, this pin value is latched by the chip.
21	NAND_Tree#	Ipu/Opu	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable At the de-assertion of reset, this pin value is latched by the chip.

Note:

1. Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
   Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin with internal pull-up (see Electrical Characteristics for value) otherwise.

The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC MII receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the RMII signals to be latched to the unintended high/low states. In this case, external pull-ups (4.7K) or pull-downs (1.0K) should be added on these PHY strap-in pins to ensure the intended values are strapped-in correctly.

Functional Description: 10Base-T/100Base-TX Transceiver

The KSZ8051MNL/RNL is an integrated single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8051MNL/RNL supports 10Base-T and 100Base-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8051MNL offers the Media Independent Interface (MII) and the KSZ8051RNL offers the Reduced Media Independent Interface (RMII) for direct connection with MII/RMII compliant Ethernet MAC processors and switches.

The MII management bus option gives the MAC processor complete access to the KSZ8051MNL/RNL control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP and RXM inputs from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8051MNL/RNL decodes a data frame. The receive clock is kept active during idle periods in between data reception.

Scrambler/De-scrambler (100Base-TX only)

The scrambler is used to spread the power spectrum of the transmitted signal to reduce EMI and baseline wander, and the de-scrambler is needed to recover the scrambled signal.

SQE and Jabber Function (10Base-T only)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

PLL Clock Synthesizer

The KSZ8051MNL/RNL generates all internal clocks and all external clocks for system timing from an external 25MHz crystal, oscillator, or reference clock. For the KSZ8051RNL in RMII 50MHz clock mode, these clocks are generated from an external 50MHz oscillator or system clock.

Auto-Negotiation

The KSZ8051MNL/RNL conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (Unshielded Twisted Pair) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ8051MNL/RNL link partner is forced to bypass auto-negotiation, then the KSZ8051MNL/RNL sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8051MNL/RNL to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

Auto-negotiation is enabled by either hardware pin strapping (NWAYEN, pin 30) or software (register 0h, bit 12).

By default, auto-negotiation is enabled after power-up or hardware reset. Afterwards, auto-negotiation can be enabled or disabled by register 0h, bit 12. If auto-negotiation is disabled, the speed is set by register 0h, bit 13, and the duplex is set by register 0h, bit 8.

The auto-negotiation link up process is shown in the following flow chart.

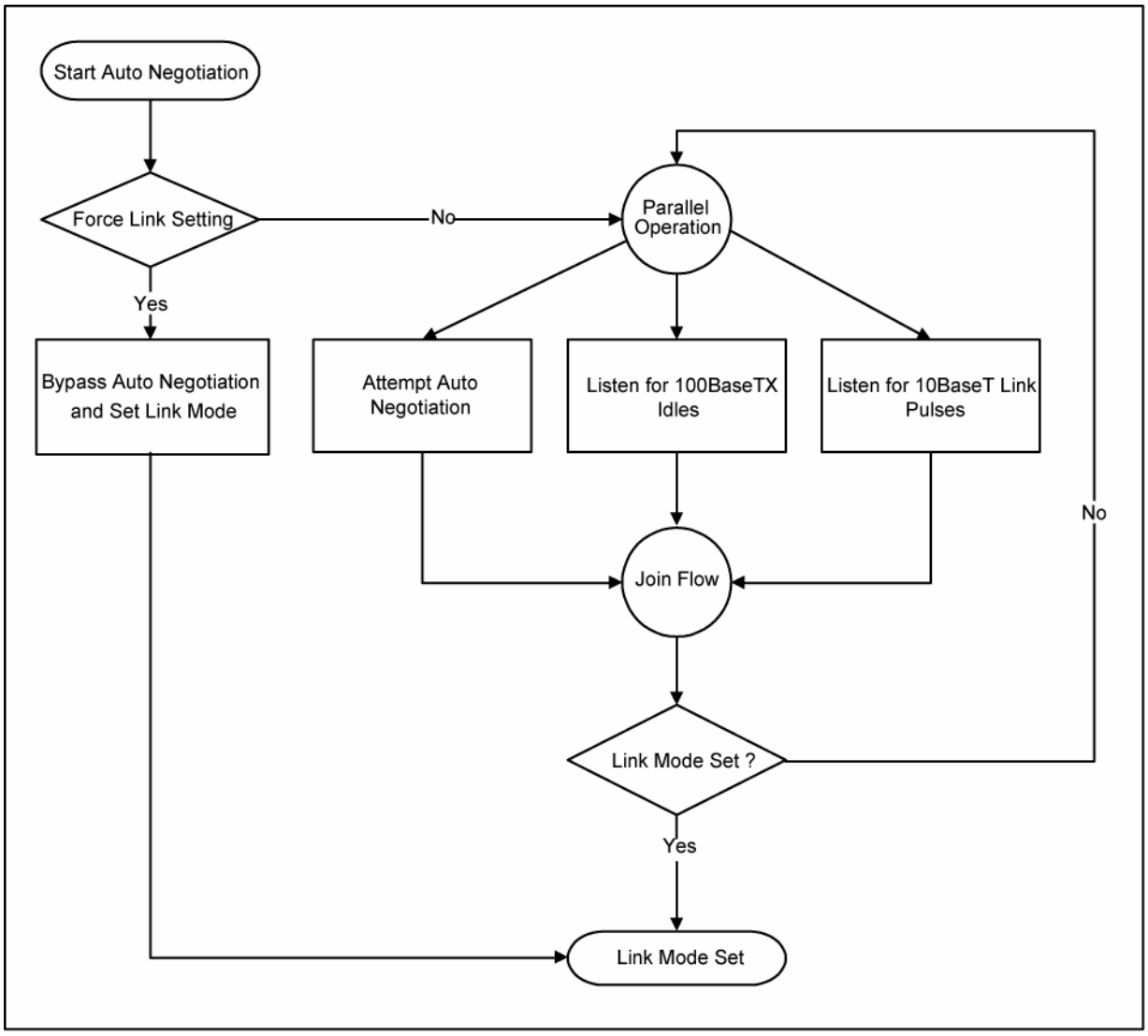


Figure 1. Auto-Negotiation Flow Chart

MII Data Interface (KSZ8051MNL only)

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 15 pins (6 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10Mbps and 100Mbps data rates are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4-bit wide, a nibble.

By default, the KSZ8051MNL is configured to MII mode after it is powered up or hardware reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to ‘000’ (default setting).

MII Signal Definition

The following table describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

MII Signal Name	Direction (with respect to PHY, KSZ8051MNL signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	Output	Input	Receive Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input, or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

Table 1. MII Signal Definition

Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0].

TXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Transmit Enable (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

Transmit Data [3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. TXD[3:0] is ”00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10Mbps mode, RXC is recovered from the line while carrier is active. RXC is derived from the PHY’s reference clock when the line is idle, or link is down.
- In 100Mbps mode, RXC is continuously recovered from the line. If link is down, RXC is derived from the PHY’s reference clock.

RXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), “5D”, and remains asserted until the end of the frame.
- In 100Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

Receive Data[3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (e.g., a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based upon the reception of an end-of-frame (EOF) marker.
- In 100Mbps mode, CRS is asserted when a start-of-stream delimiter or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

Collision (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This is used to inform the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

MII Signal Diagram

The KSZ8051MNL MII pin connections to the MAC are shown in the following figure.

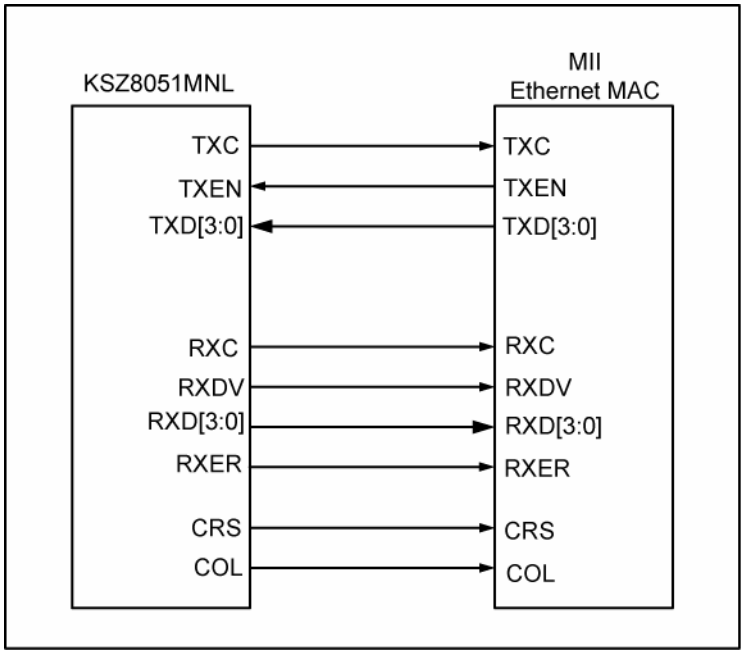


Figure 2. KSZ8051MNL MII Interface

RMII Data Interface (KSZ8051RNL only)

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Pin count is 8 pins (3 pins for data transmission, 4 pins for data reception, 1 pin for the 50MHz reference clock).
- 10Mbps and 100Mbps data rates are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 2-bit wide, a dibit.

RMII – 25MHz Clock Mode

The KSZ8051RNL is configured to RMII – 25MHz Clock Mode after it is powered up or hardware reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to '001'.
- Register 1Fh, bit 7 is set to '0' (default value) to select 25MHz Clock Mode.

RMII – 50MHz Clock Mode

The KSZ8051RNL is configured to RMII – 50MHz Clock Mode after it is powered up or hardware reset with the following:

- An external 50MHz clock source (oscillator) connected to XI (pin 9).
- The CONFIG[2:0] strapping pins (pins 18, 29, 28) set to '001'.
- Register 1Fh, bit 7 is set to '1' to select 50MHz Clock Mode.

RMII Signal Definition

The following table describes the RMII signals. Refer to RMII Specification v1.2 for detailed information.

RMII Signal Name	Direction (with respect to PHY, KSZ8051RNL signal)	Direction (with respect to MAC)	Description
REF_CLK	Output (25MHz clock mode) / <no connect> (50MHz clock mode)	Input / Input or <no connect>	Synchronous 50 MHz reference clock for receive, transmit and control interface
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RXER	Output	Input, or (not required)	Receive Error

Table 2. RMII Signal Description

Reference Clock (REF_CLK)

REF_CLK is a continuous 50MHz clock that provides the timing reference for TX_EN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

For 25MHz Clock Mode, the KSZ8051RNL generates and outputs the 50MHz RMII REF_CLK to the MAC at REF_CLK (pin 19).

For 50MHz Clock Mode, the KSZ8051RNL takes in the 50MHz RMII REF_CLK from the MAC or system board at XI (pin 9) and has the REF_CLK (pin 19) left as a no connect.

Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting dibits on TXD[1:0] for transmission. It is asserted synchronously with the first dibit of the preamble and remains asserted while all dibits to be transmitted are presented on the RMII, and is negated prior to the first REF_CLK following the final dibit of a frame.

TXEN transitions synchronously with respect to REF_CLK.

Transmit Data [1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TXEN is asserted, TXD[1:0] are accepted for transmission by the PHY.

TXD[1:0] is ”00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[1:0] while TXEN is de-asserted are ignored by the PHY.

Carrier Sense/Receive Data Valid (CRS_DV)

CRS_DV is asserted by the PHY when the receive medium is non-idle. It is asserted asynchronously on detection of carrier. This is when squelch is passed in 10Mbps mode, and when 2 non-contiguous zeroes in 10 bits are detected in 100Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

So long as carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered dibit of the frame through the final recovered dibit, and it is negated prior to the first REF_CLK that follows the final dibit. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is "00" until proper receive signal decoding takes place.

Receive Data [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously with respect to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY.

RXD[1:0] is "00" to indicate idle when CRS_DV is de-asserted. Values other than “00” on RXD[1:0] while CRS_DV is de-asserted are ignored by the MAC.

Receive Error (RXER)

RXER is asserted for one or more REF_CLK periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RX_ER has no effect on the MAC.

Collision Detection

The MAC regenerates the COL signal of the MII from TXEN and CRS_DV.

RMII Signal Diagram

The KSZ8051RNL RMII pin connections to the MAC are shown in the following figures for 25MHz Clock Mode and 50MHz Clock Mode.

RMII – 25MHz Clock Mode

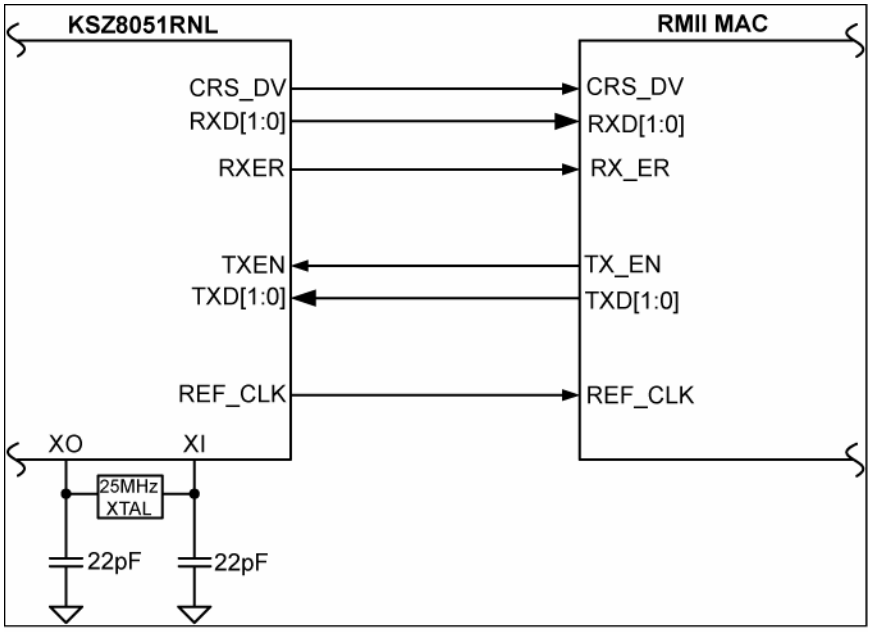


Figure 3. KSZ8051RNL RMII Interface (25MHz Clock Mode)

RMII – 50MHz Clock Mode

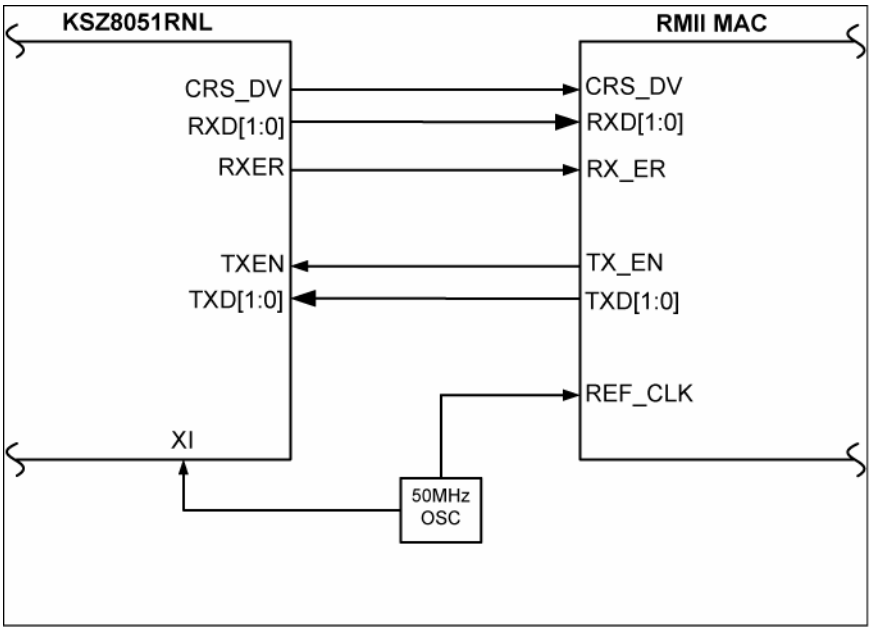


Figure 4. KSZ8051RNL RMII Interface (50MHz Clock Mode)

Back-to-Back Mode – 100Mbps Copper Repeater / Media Converter

Two KSZ8051MNL/RNL devices can be connected back-to-back to form a 100Base-TX to 100Base-TX copper repeater.

A KSZ8051MNL/RNL and a KSZ8041FTL can be connected back-to-back to provide a low cost media converter solution. Media conversion is between 100Base-TX copper and 100Base-FX fiber. On the copper side, link up at 10Base-T is not allowed, and is blocked during auto-negotiation.

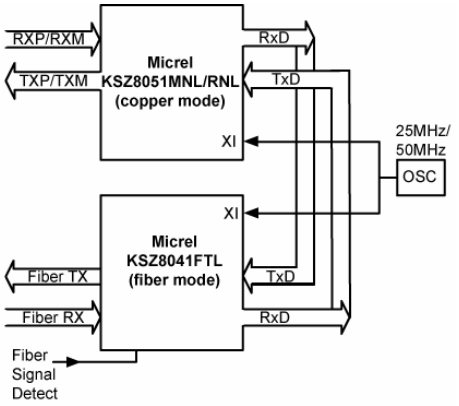


Figure 5. KSZ8051MNL/RNL and KSZ8041FTL Back-to-Back Media Converter

MII Back-to-Back Mode (KSZ8051MNL only)

In MII Back-to-Back mode, a KSZ8051MNL interfaces with another KSZ8051MNL, or a KSZ8041FTL to provide a complete 100Mbps copper repeater, or media converter solution, respectively.

The KSZ8051MNL devices are configured to MII Back-to-Back mode after power-up or reset with the following:

- Strapping pin CONFIG[2:0] (pins 18, 29, 28) set to '110'
- A common 25MHz reference clock connected to XI (pin 9)
- MII signals connected as shown in the following table.

KSZ8051MNL (100Base-TX copper) [Device 1]			KSZ8051MNL (100Base-TX copper) [Device 2]		
Pin Name	**Pin Number**	**Pin Type**	**Pin Name**	**Pin Number**	**Pin Type**
RXC	19	Output	TXC	22	Input
RXDV	18	Output	TXEN	23	Input
RXD3	13	Output	TXD3	27	Input
RXD2	14	Output	TXD2	26	Input
RXD1	15	Output	TXD1	25	Input
RXD0	16	Output	TXD0	24	Input
TXC	22	Input	RXC	19	Output
TXEN	23	Input	RXDV	18	Output
TXD3	27	Input	RXD3	13	Output
TXD2	26	Input	RXD2	14	Output
TXD1	25	Input	RXD1	15	Output
TXD0	24	Input	RXD0	16	Output

Table 3. MII Signal Connection for MII Back-to-Back Mode (100Base-TX Copper Repeater)

RMII Back-to-Back Mode (KSZ8051RNL only)

In RMII Back-to-Back mode, a KSZ8051RNL interfaces with another KSZ8051RNL, or a KSZ8041FTL to provide a complete 100Mbps copper repeater, or media converter solution, respectively.

The KSZ8051RNL devices are configured to RMII Back-to-Back mode after power-up or reset with the following:

- Strapping pin CONFIG[2:0] (pins 18, 29, 28) set to '101'
- A common 50MHz reference clock connected to XI (pin 9)
- RMII signals connected as shown in the following table.

KSZ8051RNL (100Base-TX copper) [Device 1]			KSZ8051RNL (100Base-TX copper) [Device 2]		
Pin Name	**Pin Number**	**Pin Type**	**Pin Name**	**Pin Number**	**Pin Type**
CRSDV	18	Output	TXEN	23	Input
RXD1	15	Output	TXD1	25	Input
RXD0	16	Output	TXD0	24	Input
TXEN	23	Input	CRSDV	18	Output
TXD1	25	Input	RXD1	15	Output
TXD0	24	Input	RXD0	16	Output

Table 4. RMII Signal Connection for RMII Back-to-Back Mode (100Base-TX Copper Repeater)

MII Management (MIIM) Interface

The KSZ8051MNL/RNL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface enables upper-layer device, like a MAC processor, to monitor and control the state of the KSZ8051MNL/RNL. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows the external controller to communicate with one or more PHY devices.
- A set of 16-bit MDIO registers. Registers [0:8] are standard registers, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See "Register Map" section for details.

As the default, the KSZ8051MNL/RNL supports unique PHY addresses 1 to 7, and broadcast PHY address 0. The latter is defined per the IEEE 802.3 Specification, and can be used to read/write to a single KSZ8051MNL/RNL device, or write to multiple KSZ8051MNL/RNL devices simultaneously.

Optionally, PHY address 0 can be disabled as the broadcast address by either hardware pin strapping (B-CAST_OFF, pin 19) or software (register 16h, bit 9), and assigned as a unique PHY address.

The PHYAD[2:0] strapping pins are used to assigned a unique PHY address between 0 and 7 to each KSZ8051MNL/RNL device.

The following table shows the MII Management frame format for the KSZ8051MNL/RNL.

	Preamble	**Start of Frame**	**Read/Write OP Code**	**PHY Address Bits [4:0]**	**REG Address Bits [4:0]**	**TA**	**Data Bits [15:0]**	**Idle**
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Table 5. MII Management Frame Format – for KSZ8051MNL/RNL

Interrupt (INTRP)

INTRP (pin 21) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8051MNL/RNL PHY register. Register 1Bh, bits [15:8] are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Register 1Bh, bits [7:0] are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Register 1Fh, bit 9 sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ8051MNL/RNL control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the confusion of whether to use a straight cable or a crossover cable between the KSZ8051MNL/RNL and its link partner. This feature allows the KSZ8051MNL/RNL to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner, and then assigns transmit and receive pairs of the KSZ8051MNL/RNL accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to register 1Fh, bit 13. MDI and MDI-X mode is selected by register 1Fh, bit 14 if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X.

The IEEE 802.3 Standard defines MDI and MDI-X as follows:

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TX+	1	RX+
2	TX-	2	RX-
3	RX+	3	TX+
6	RX-	6	TX-

Table 6. MDI/MDI-X Pin Definition

Straight Cable

A straight cable connects a MDI device to a MDI-X device, or a MDI-X device to a MDI device. The following figure depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

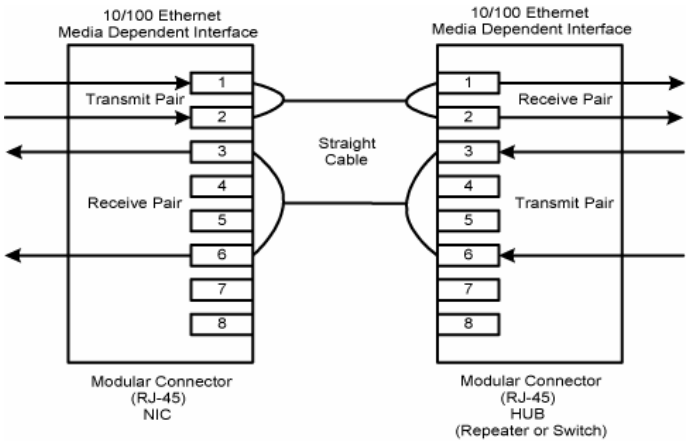


Figure 6. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects a MDI device to another MDI device, or a MDI-X device to another MDI-X device. The following figure depicts a typical crossover cable connection between two switches or hubs (two MDI-X devices).

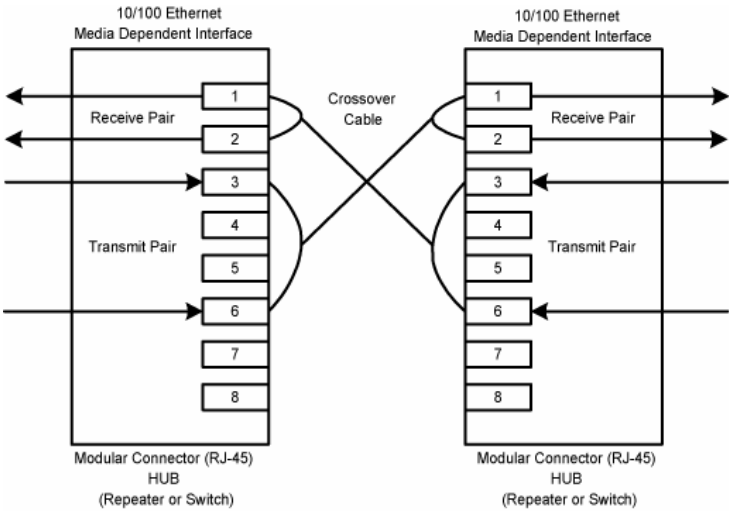


Figure 7. Typical Crossover Cable Connection

LinkMD® Cable Diagnostics

The LinkMD® function utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits and impedance mismatches.

LinkMD® works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, and then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD® function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD® is initiated by accessing register 1Dh, the LinkMD® Control/Status Register, in conjunction with register 1Fh, the PHY Control 2 Register. The latter register is used to disable auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

NAND Tree Support

The KSZ8051MNL/RNL provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8051MNL/RNL digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the CRS/CONFIG1 pin provides the output for the nested NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving low each NAND tree input pin sequentially per the NAND tree pin order
- Checking the NAND tree output to ensure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

The following tables list the NAND tree pin order.

Pin Number	Pin Name	NAND Tree Description
11	MDIO	Input
12	MDC	Input
13	RXD3	Input
14	RXD2	Input
15	RXD1	Input
16	RXD0	Input
18	RXDV	Input
19	RXC	Input
20	RXER	Input
21	INTRP	Input
22	TXC	Input
23	TXEN	Input
24	TXD0	Input
25	TXD1	Input
26	TXD2	Input
27	TXD3	Input
30	LED0	Input
31	LED1	Input
28	COL	Input
29	CRS	Output

Table 7. NAND Tree Test Pin Order – for KSZ8051MNL

Pin Number	Pin Name	NAND Tree Description
11	MDIO	Input
12	MDC	Input
13	PHYAD0	Input
14	PHYAD1	Input
15	RXD1	Input
16	RXD0	Input
18	CRS_DV	Input
19	REF_CLK	Input
20	RXER	Input
21	INTRP	Input
23	TXEN	Input
24	TXD0	Input
25	TXD1	Input
30	LED0	Input
31	LED1	Input
28	CONFIG0	Input
29	CONFIG1	Output

Table 8. NAND Tree Test Pin Order – for KSZ8051RNL

NAND Tree I/O Testing

The following procedure can be used to check for faults on the KSZ8051MNL/RNL digital I/O pin connections to the board:

1. Enable NAND tree mode by either hardware pin strapping (NAND_Tree#, pin 21) or software (register 16h, bit 5).
2. Use board logic to drive all KSZ8051MNL/RNL NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, per KSZ8051MNL/RNL NAND Tree pin order, as follow:
    a. Toggle the first pin (MDIO) from high to low, and verify the CRS/CONFIG1 pin switch from low to high to indicate that the first pin is connected properly.
    b. Leave the first pin (MDIO) low.
    c. Toggle the second pin (MDC) from high to low, and verify the CRS/CONFIG1 pin switch from high to low to indicate that the second pin is connected properly.
    d. Leave the first pin (MDIO) and the second pin (MDC) low.
    e. Toggle the third pin from high to low, and verify the CRS/CONFIG1 pin switch from low to high to indicate that the third pin is connected properly.
    f. Continue with this sequence until all KSZ8051MNL/RNL NAND tree input pins have been toggled.

Each KSZ8051MNL/RNL NAND tree input pin must cause the CRS/CONFIG1 output pin to toggle high-to-low or low-to-high to indicate a good connection. If the CRS/CONFIG1 pin fails to toggle when the KSZ8051MNL/RNL input pin toggles from high to low, the input pin has a fault.

Power Management

The KSZ8051MNL/RNL offers the following power management modes:

Power Saving Mode

Power Saving Mode is used to reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a one to register 1Fh, bit 10, and is in effect when auto-negotiation mode is enabled and cable is disconnected (no link).

In this mode, the KSZ8051MNL/RNL shuts down all transceiver blocks, except for transmitter, energy detect and PLL circuits.

By default, Power Saving Mode is disabled after power-up.

Energy Detect Power Down Mode

Energy Detect Power Down Mode is used to further reduce the transceiver power consumption when the cable is un-plugged. It is enabled by writing a zero to register 18h, bit 11, and is in effect when auto-negotiation mode is enabled and cable is disconnected (no link).

In this mode, the KSZ8051MNL/RNL shuts down all transceiver blocks, except for transmitter and energy detect circuits.

Further power consumption is achieved by extending the time interval in between transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure two link partners in the same low power state and with auto MDI/MDI-X disabled can wake up when the cable is connected between them.

By default, Energy Detect Power Down Mode is disabled after power-up.

Power Down Mode

Power Down Mode is used to power down the KSZ8051MNL/RNL device when it is not in use after power-up. It is enabled by writing a one to register 0h, bit 11.

In this mode, the KSZ8051MNL/RNL disables all internal functions, except for the MII management interface. The KSZ8051MNL/RNL exits (disables) Power Down Mode after register 0h, bit 11 is set back to zero.

Slow Oscillator Mode

Slow Oscillator Mode is used to disconnect the input reference crystal/clock on XI (pin 9) and select the on-chip slow oscillator when the KSZ8051MNL/RNL device is not in use after power-up. It is enabled by writing a one to register 11h, bit 5.

Slow Oscillator Mode works in conjunction with Power Down Mode to put the KSZ8051MNL/RNL device in the lowest

power state with all internal functions disabled, except for the MII management interface. To properly exit this mode and return to normal PHY operation, use the following programming sequence:

1. Disable Slow Oscillator Mode by writing a zero to register 11h, bit 5.
2. Disable Power Down Mode by writing a zero to register 0h, bit 11.
3. Initiate software reset by writing a one to register 0h, bit 15.

Reference Circuit for Power and Ground Connections

The KSZ8051MNL/RNL is a single 3.3V supply device with a built-in regulator to supply the 1.2V core. The power and ground connections are shown in the following figure and table for 3.3V VDDIO.

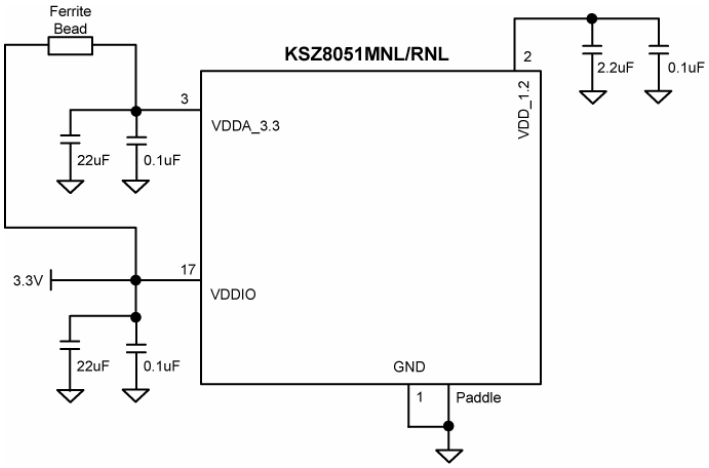


Figure 8. KSZ8051MNL/RNL Power and Ground Connections

Power Pin	Pin Number	Description
VDD_1.2	2	Decouple with 2.2uF and 0.1uF capacitors-to-ground.
VDDA_3.3	3	Connect to board's 3.3V supply through ferrite bead. Decouple with 22uF and 0.1uF capacitors-to-ground.
VDDIO	17	Connect to board's 3.3V supply for 3.3V VDDIO. Decouple with 22uF and 0.1uF capacitors-to-ground.

Table 9. KSZ8051MNL/RNL Power Pin Description

Register Map

Register Number (Hex)	Description
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Link Partner Next Page Ability
9h – 10h	Reserved
11h	AFE Control 1
12h – 14h	Reserved
15h	RXER Counter
16h	Operation Mode Strap Override
17h	Operation Mode Strap Status
18h	Expanded Control
19h – 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch	Reserved
1Dh	LinkMD® Control/Status
1Eh	PHY Control 1
1Fh	PHY Control 2

Register Description

Address	Name	Description	Mode(1)	Default
Register 0h – Basic Control				
0.15	Reset	1 = Software reset 0 = Normal operation This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.14	Loop-back	1 = Loop-back mode 0 = Normal operation	RW	0
0.13	Speed Select	1 = 100Mbps 0 = 10Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1).	RW	Set by SPEED strapping pin. See "Strapping Options" section for details.
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, auto-negotiation result overrides settings in register 0.13 and 0.8.	RW	Set by NWAYEN strapping pin. See "Strapping Options" section for details.

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
Register 0h – Basic Control				
0.11	Power Down	1 = Power down mode 0 = Normal operation If software reset (register 0.15) is used to exit Power Down mode (register 0.11 = 1), two software reset writes (register 0.15 = 1) are required. First write clears Power Down mode; second write resets chip and re-latches the pin strapping pin values.	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from MII 0 = Normal operation	RW	Set by ISO strapping pin. See “Strapping Options” section for details.
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a ‘1’ is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	Inverse of DUPLEX strapping pin value. See “Strapping Options” section for details.
0.7	Collision Test	1 = Enable COL test 0 = Disable COL test	RW	0
0.6:0	Reserved		RO	000_0000
Register 1h – Basic Status				
1.15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100Base-TX Full Duplex	1 = Capable of 100Mbps full-duplex 0 = Not capable of 100Mbps full-duplex	RO	1
1.13	100Base-TX Half Duplex	1 = Capable of 100Mbps half-duplex 0 = Not capable of 100Mbps half-duplex	RO	1
1.12	10Base-T Full Duplex	1 = Capable of 10Mbps full-duplex 0 = Not capable of 10Mbps full-duplex	RO	1
1.11	10Base-T Half Duplex	1 = Capable of 10Mbps half-duplex 0 = Not capable of 10Mbps half-duplex	RO	1
1.10:7	Reserved		RO	0000
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Capable to perform auto-negotiation 0 = Not capable to perform auto-negotiation	RO	1

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capabilities registers	RO	1
Register 2h – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0022h
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0001_01
3.9:4	Model Number	Six bit manufacturer's model number	RO	01_0101
3.3:0	Revision Number	Four bit manufacturer's revision number	RO	Indicates silicon revision
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability.	RW	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved		RO	0
4.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RW	00
4.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	Set by SPEED strapping pin. See "Strapping Options" section for details.
4.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RW	Set by SPEED strapping pin. See "Strapping Options" section for details.
4.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RW	1
4.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved		RO	0
5.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RO	00
5.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RO	0
5.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RO	0
5.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RO	0
5.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0001
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved		RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next page(s) will follow 0 = Last page	RW	0
7.14	Reserved		RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001
Register 8h – Link Partner Next Page Ability				
8.15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0
8.12	Acknowledge2	1 = Able to act on the information 0 = Not able to act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one	RO	0
8.10:0	Message Field		RO	000_0000_0000
Register 11h – AFE Control 1				
11.15:6	Reserved		RW	0000_0000_00
11.5	Slow Oscillator Mode Enable	Slow Oscillator Mode is used to disconnect the input reference crystal/clock on the XI pin and select the on-chip slow oscillator when the KSZ8051 device is not in use after power-up. 1 = Enable 0 = Disable This bit automatically sets software power down to the analog side when enabled.	RW	0
11.4:0	Reserved		RW	0_0000
Register 15h – RXER Counter				
15.15:0	RXER Counter	Receive error counter for Symbol Error frames	RO/SC	0000h

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
Register 16h – Operation Mode Strap Override				
16.15:11	Reserved		RW	0000_0
16.10	Reserved		RO	0
16.9	B-CAST_OFF override	1 = Override strap-in for B-CAST_OFF If bit is '1', PHY Address 0 is non-broadcast.	RW	0
16.8	Reserved		RW	0
16.7	MII B-to-B override	1 = Override strap-in for MII Back-to-Back mode (set also bit 0 of this register to 1) This bit is applicable for KSZ8051MNL only.	RW	0
16.6	RMII B-to-B override	1 = Override strap-in for RMII Back-to-Back mode (set also bit 1 of this register to 1) This bit is applicable for KSZ8051RNL only.	RW	0
16.5	NAND Tree override	1 = Override strap-in for NAND Tree mode	RW	0
16.4:2	Reserved		RW	000
16.1	RMII override	1 = Override strap-in for RMII mode This bit is applicable for KSZ8051RNL only.	RW	0
16.0	MII override	1 = Override strap-in for MII mode This bit is applicable for KSZ8051MNL only.	RW	1
Register 17h – Operation Mode Strap Status				
17.15:13	PHYAD[2:0] strap-in status	[000] = Strap to PHY Address 0 [001] = Strap to PHY Address 1 [010] = Strap to PHY Address 2 [011] = Strap to PHY Address 3 [100] = Strap to PHY Address 4 [101] = Strap to PHY Address 5 [110] = Strap to PHY Address 6 [111] = Strap to PHY Address 7	RO	
17.12:10	Reserved		RO	
17.9	B-CAST_OFF strap-in status	1 = Strap to B-CAST_OFF If bit is '1', PHY Address 0 is non-broadcast.	RO	
17.8	Reserved		RO	
17.7	MII B-to-B strap-in status	1 = Strap to MII Back-to-Back mode This bit is applicable for KSZ8051MNL only.	RO	
17.6	RMII B-to-B strap-in status	1 = Strap to RMII Back-to-Back mode This bit is applicable for KSZ8051RNL only.	RO	
17.5	NAND Tree strap-in status	1 = Strap to NAND Tree mode	RO	
17.4:2	Reserved		RO	
17.1	RMII strap-in status	1 = Strap to RMII mode This bit is applicable for KSZ8051RNL only.	RO	
17.0	MII strap-in status	1 = Strap to MII mode This bit is applicable for KSZ8051MNL only.	RO	

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
Register 18h – Expanded Control				
18.15:12	Reserved		RW	0000
18.11	EDPD Disabled	Energy Detect Power Down mode 1 = Disable 0 = Enable	RW	1
18.10	100Base-TX Preamble Restore	1 = Restore received preamble to MII output (random latency) 0 = Consume 1-byte preamble before sending frame to MII output for fixed latency This bit is applicable for KSZ8051MNL only.	RW	0
18.9:7	Reserved		RW	000
18.6	10Base-T Preamble Restore	1 = Restore received preamble to MII output 0 = Remove all 7-bytes of preamble before sending frame (starting with SFD) to MII output This bit is applicable for KSZ8051MNL only.	RW	0
18.5:0	Reserved		RW	00_0000
Register 1Bh – Interrupt Control/Status				
1b.15	Jabber Interrupt Enable	1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt	RW	0
1b.14	Receive Error Interrupt Enable	1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt	RW	0
1b.13	Page Received Interrupt Enable	1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt	RW	0
1b.12	Parallel Detect Fault Interrupt Enable	1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt	RW	0
1b.11	Link Partner Acknowledge Interrupt Enable	1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt	RW	0
1b.10	Link Down Interrupt Enable	1= Enable Link Down Interrupt 0 = Disable Link Down Interrupt	RW	0
1b.9	Remote Fault Interrupt Enable	1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt	RW	0
1b.8	Link Up Interrupt Enable	1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt	RW	0
1b.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occurred	RO/SC	0
1b.6	Receive Error Interrupt	1 = Receive Error occurred 0 = Receive Error did not occurred	RO/SC	0

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
1b.5	Page Receive Interrupt	1 = Page Receive occurred 0 = Page Receive did not occur	RO/SC	0
1b.4	Parallel Detect Fault Interrupt	1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occur	RO/SC	0
1b.3	Link Partner Acknowledge Interrupt	1 = Link Partner Acknowledge occurred 0 = Link Partner Acknowledge did not occur	RO/SC	0
1b.2	Link Down Interrupt	1 = Link Down occurred 0 = Link Down did not occur	RO/SC	0
1b.1	Remote Fault Interrupt	1 = Remote Fault occurred 0 = Remote Fault did not occur	RO/SC	0
1b.0	Link Up Interrupt	1 = Link Up occurred 0 = Link Up did not occur	RO/SC	0
Register 1Dh – LinkMD® Control/Status				
1d.15	Cable Diagnostic Test Enable	1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared. 0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read.	RW/SC	0
1d.14:13	Cable Diagnostic Test Result	[00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test has failed	RO	00
1d.12	Short Cable Indicator	1 = Short cable (<10 meter) has been detected by LinkMD®.	RO	0
1d.11:9	Reserved		RW	000
1d.8:0	Cable Fault Counter	Distance to fault	RO	0_0000_0000
Register 1Eh – PHY Control 1				
1e.15:10	Reserved		RO	0000_00
1e.9	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0
1e.8	Link Status	1 = Link is up 0 = Link is down	RO	0
1e.7	Polarity Status	1 = Polarity is reversed 0 = Polarity is not reversed	RO	
1e.6	Reserved		RO	0
1e.5	MDI/MDI-X State	1 = MDI-X 0 = MDI	RO	
1e.4	Energy Detect	1 = Presence of signal on receive differential pair 0 = No signal detected on receive differential pair	RO	0

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
1e.3	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation	RW	0
1e.2:0	Operation Mode Indication	[000] = still in auto-negotiation [001] = 10Base-T half-duplex [010] = 100Base-TX half-duplex [011] = reserved [100] = reserved [101] = 10Base-T full-duplex [110] = 100Base-TX full-duplex [111] = reserved	RO	000
Register 1Fh – PHY Control 2				
1f:15	HP_MDIX	1 = HP Auto MDI/MDI-X mode 0 = Micrel Auto MDI/MDI-X mode	RW	1
1f:14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 1 = MDI-X Mode Transmit on RXP,RXM (pins 5,4) and Receive on TXP,TXM (pins 7,6) 0 = MDI Mode Transmit on TXP,TXM (pins 7,6) and Receive on RXP,RXM (pins 5,4)	RW	0
1f:13	Pair Swap Disable	1 = Disable auto MDI/MDI-X 0 = Enable auto MDI/MDI-X	RW	0
1f.12	Reserved		RW	0
1f.11	Force Link	1 = Force link pass 0 = Normal link operation This bit bypasses the control logic and allow transmitter to send pattern even if there is no link.	RW	0
1f.10	Power Saving	1 = Enable power saving 0 = Disable power saving	RW	0
1f.9	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
1f.8	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
1f.7	RMII Reference Clock Select	1 = RMII 50MHz Clock Mode; clock input to XI (pin 9) is 50MHz 0 = RMII 25MHz Clock Mode; clock input to XI (pin 9) is 25MHz This bit is applicable for KSZ8051RNL only.	RW	0
1f.6	Reserved		RW	0

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
1f.5:4	LED mode	[00] = LED1 : Speed LED0 : Link/Activity [01] = LED1 : Activity LED0 : Link [10], [11] = Reserved	RW	00
1f.3	Disable Transmitter	1 = Disable transmitter 0 = Enable transmitter	RW	0
1f.2	Remote Loop-back	1 = Remote (analog) loop back is enable 0 = Normal mode	RW	0
1f.1	Enable SQE Test	1 = Enable SQE test 0 = Disable SQE test	RW	0
1f.0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

Note:

1. RW = Read/Write.
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.
   LL = Latch low.

Absolute Maximum Ratings[1]

Supply Voltage
($V_{DD\_1.2}$) ..... -0.5V to +1.8V
($V_{DDIO,}$ $V_{DDA\_3.3}$) ..... -0.5V to +4.0V
Input Voltage (all inputs) ..... -0.5V to +4.0V
Output Voltage (all outputs) ..... -0.5V to +4.0V
Lead Temperature (soldering, 10sec.) ..... 260°C
Storage Temperature (T_s) ..... -55°C to +150°C

Operating Ratings[2]

Supply Voltage
($V_{DDIO\_3.3,}$ $V_{DDA\_3.3}$) ..... +3.135V to +3.465V
($V_{DDIO\_2.5}$) ..... +2.375V to +2.625V
($V_{DDIO\_1.8}$) ..... +1.710V to +1.890V
Ambient Temperature
(T_A, Commercial) ..... 0°C to +70°C
(T_A, Industrial) ..... -40°C to +85°C
Maximum Junction Temperature (T_J Max) ..... 125°C
Thermal Resistance (θ_{JA}) ..... 34°C/W
Thermal Resistance (θ_{JC}) ..... 6°C/W

Electrical Characteristics[3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Supply Current (V_{DDIO},$V_{DDA\_3.3}$ = 3.3V)[4]						
I_{DD1}	10Base-T	Full-duplex traffic @ 100% utilization		39.5		mA
I_{DD2}	100Base-TX	Full-duplex traffic @ 100% utilization		48.9		mA
I_{DD3}	Power Saving Mode	Ethernet cable disconnected (reg. 1F.10 = 1)		30.0		mA
I_{DD4}	Power Down Mode	Software power down (reg. 0.11 = 1)		2.0		mA
CMOS Level Inputs						
V_{IH}	Input High Voltage	V_{DDIO} = 3.3V	2.0			V
		V_{DDIO} = 2.5V	1.8			V
		V_{DDIO} = 1.8V	1.3			V
V_{IL}	Input Low Voltage	V_{DDIO} = 3.3V			0.8	V
		V_{DDIO} = 2.5V			0.7	V
		V_{DDIO} = 1.8V			0.5	V
I_{IN}	Input Current	V_{IN} = GND ~ VDDIO		-10	10	µA
CMOS Level Outputs						
V_{OH}	Output High Voltage	V_{DDIO} = 3.3V	2.4			V
		V_{DDIO} = 2.5V	2.0			V
		V_{DDIO} = 1.8V	1.5			V
V_{OL}	Output Low Voltage	V_{DDIO} = 3.3V			0.4	V
		V_{DDIO} = 2.5V			0.4	V
		V_{DDIO} = 1.8V			0.3	V
$\|I_{oz}\|$	Output Tri-State Leakage				10	µA
LED Outputs						
I_{LED}	Output Drive Current	Each LED pin (LED0, LED1)		8		mA
Strapping Pins						
pu	Internal Pull-up Resistance	V_{DDIO} = 3.3V	29	43	76	KΩ
		V_{DDIO} = 2.5V	37	59	102	KΩ
		V_{DDIO} = 1.8V	57	100	187	KΩ
pd	Internal Pull-down Resistance	V_{DDIO} = 3.3V	27	43	76	KΩ
		V_{DDIO} = 2.5V	35	60	110	KΩ
		V_{DDIO} = 1.8V	55	100	190	KΩ

Electrical Characteristics[3] (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
100Base-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination across differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination across differential output			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				± 0.25	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of ISET			0.65		V
	Output Jitter	Peak-to-peak		0.7	1.4	ns
10Base-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	100Ω termination across differential output	2.2		2.8	V
	Jitter Added	Peak-to-peak			3.5	ns
t_r, t_f	Rise/Fall Time			25		ns
10Base-T Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV
REF_CLK Output						
	50MHz RMII Clock Output Jitter	Peak-to-peak (Applies to KSZ8051RNL in RMII – 25MHz Clock Mode only)		600		ps

Notes:

1. Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
2. The device is not guaranteed to function outside its operating rating.
3. T_A = 25°C. Specification is for packaged product only.
4. Current consumption is for the single 3.3V supply KSZ8051MNL/RNL device only, and includes the transmit driver current and the 1.2V supply voltage ($V_{DD\_1.2}$) that are supplied by the KSZ8051MNL/RNL.

Timing Diagrams

MII SQE Timing (10Base-T)

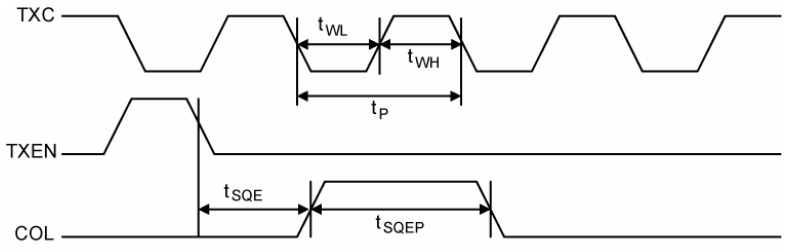


Figure 9. MII SQE Timing (10Base-T)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	TXC period		400		ns
t_{WL}	TXC pulse width low		200		ns
t_{WH}	TXC pulse width high		200		ns
t_{SQE}	COL (SQE) delay after TXEN de-asserted		1.8		µs
t_{SQEP}	COL (SQE) pulse duration		1.0		µs

Table 10. MII SQE Timing (10Base-T) Parameters

MII Transmit Timing (10Base-T)

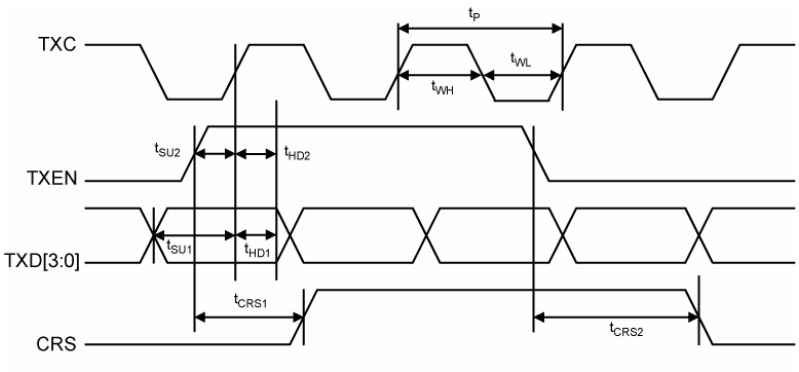


Figure 10. MII Transmit Timing (10Base-T)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	TXC period		400		ns
t_{WL}	TXC pulse width low		200		ns
t_{WH}	TXC pulse width high		200		ns
t_{SU1}	TXD[3:0] setup to rising edge of TXC	120			ns
t_{SU2}	TXEN setup to rising edge of TXC	120			ns
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0			ns
t_{HD2}	TXEN hold from rising edge of TXC	0			ns
t_{CRS1}	TXEN high to CRS asserted latency		200		ns
t_{CRS2}	TXEN low to CRS de-asserted latency		550		ns

Table 11. MII Transmit Timing (10Base-T) Parameters

MII Receive Timing (10Base-T)

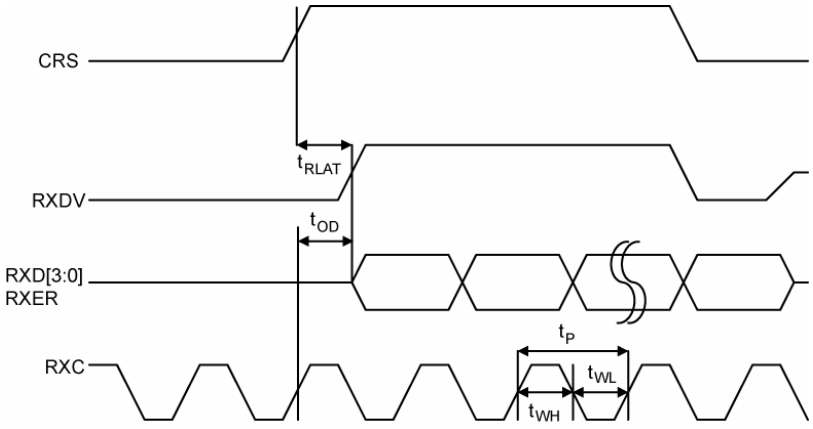


Figure 11. MII Receive Timing (10Base-T)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	RXC period		400		ns
t_{WL}	RXC pulse width low		200		ns
t_{WH}	RXC pulse width high		200		ns
t_{OD}	(RXDV, RXD[3:0], RXER) output delay from rising edge of RXC		185		ns
t_{RLAT}	CRS to (RXDV, RXD[3:0]) latency		6.5		µs

Table 12. MII Receive Timing (10Base-T) Parameters

MII Transmit Timing (100Base-TX)

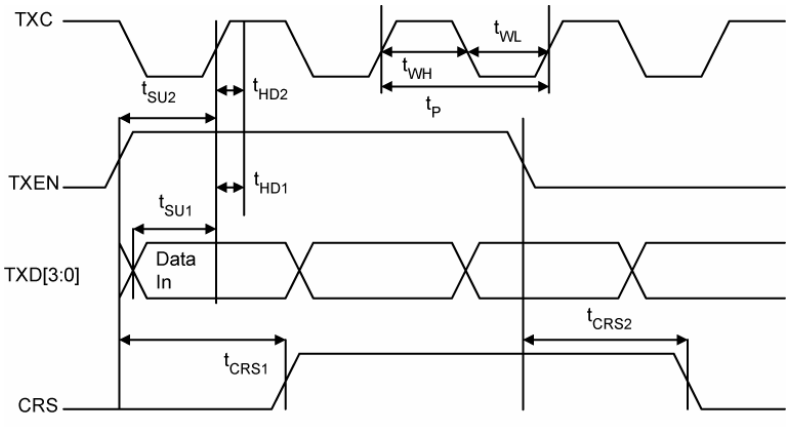


Figure 12. MII Transmit Timing (100Base-TX)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	TXC period		40		ns
t_{WL}	TXC pulse width low		20		ns
t_{WH}	TXC pulse width high		20		ns
t_{SU1}	TXD[3:0] setup to rising edge of TXC	10			ns
t_{SU2}	TXEN setup to rising edge of TXC	10			ns
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0			ns
t_{HD2}	TXEN hold from rising edge of TXC	0			ns
t_{CRS1}	TXEN high to CRS asserted latency		35		ns
t_{CRS2}	TXEN low to CRS de-asserted latency		36		ns

Table 13. MII Transmit Timing (100Base-TX) Parameters

MII Receive Timing (100Base-TX)

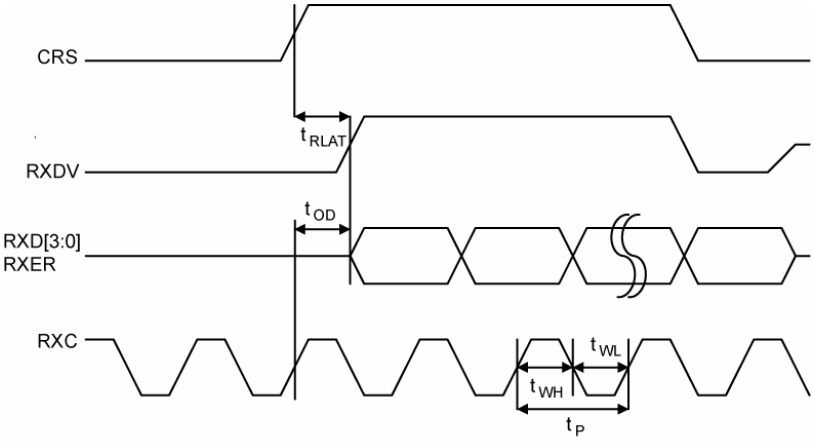


Figure 13. MII Receive Timing (100Base-TX)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	RXC period		40		ns
t_{WL}	RXC pulse width low		20		ns
t_{WH}	RXC pulse width high		20		ns
t_{OD}	(RXDV, RXD[3:0], RXER) output delay from rising edge of RXC		23		ns
t_{RLAT}	CRS to (RXDV, RXD[3:0]) latency		130		ns

Table 14. MII Receive Timing (100Base-TX) Parameters

RMII Timing

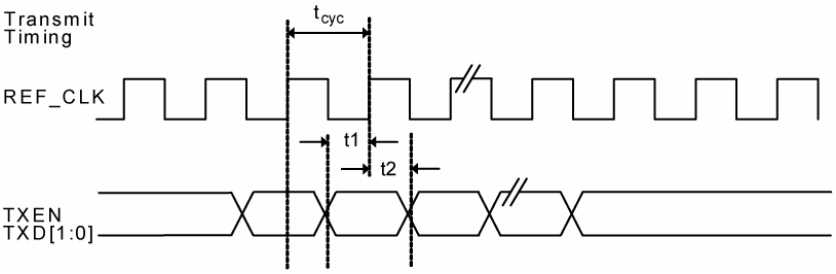


Figure 14. RMII Timing – Data Received from RMII

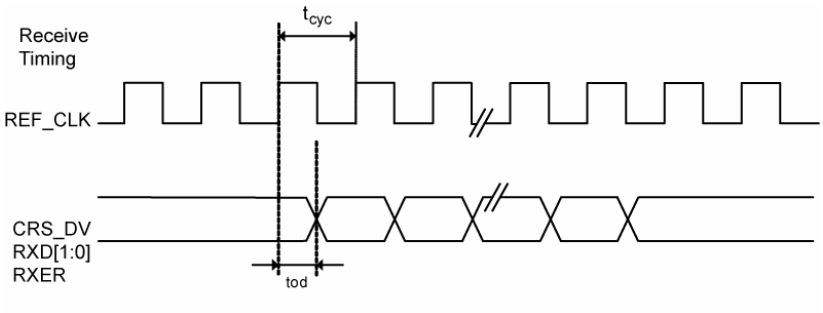


Figure 15. RMII Timing – Data Input to RMII

Timing Parameter	Description	Min	Typ	Max	Unit
t_{cyc}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	2			ns
t_{od}	Output delay	7	9	13	ns

Table 15. RMII Timing Parameters – KSZ8051RNL (25MHz input to XI pin, 50MHz output from REF_CLK pin)

Timing Parameter	Description	Min	Typ	Max	Unit
t_{cyc}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	8			ns
t_{od}	Output delay	9	13	15	ns

Table 16. RMII Timing Parameters – KSZ8051RNL (50MHz input to XI pin)

Auto-Negotiation Timing

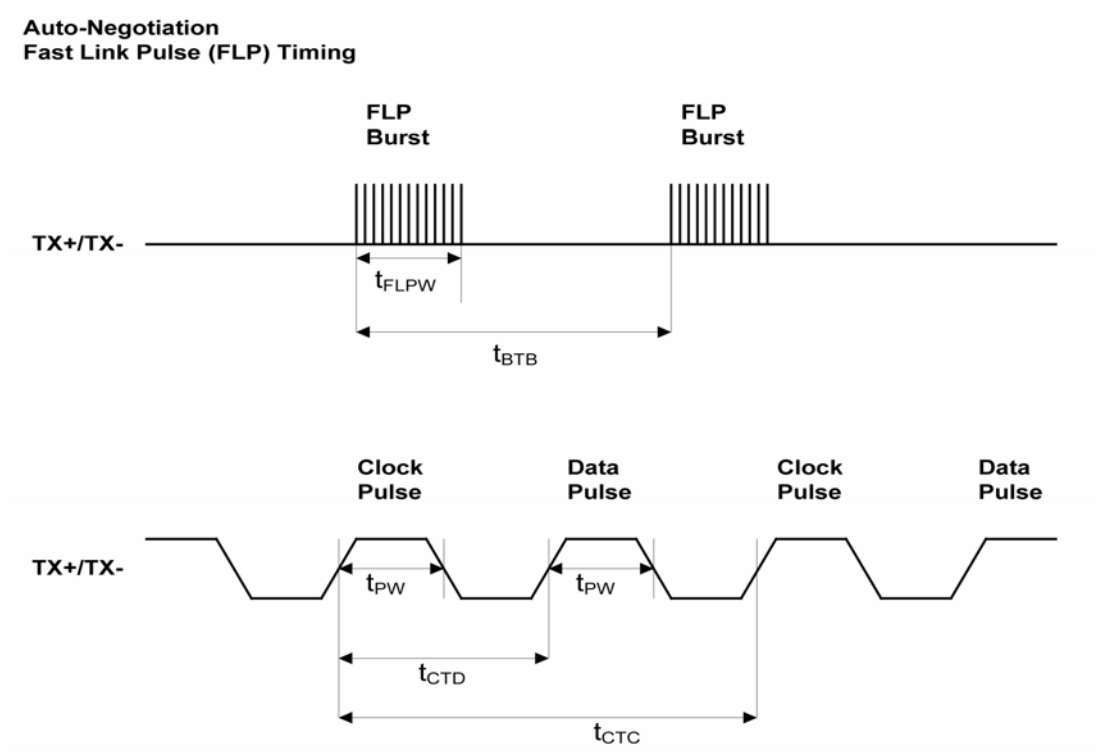


Figure 16. Auto-Negotiation Fast Link Pulse (FLP) Timing

Timing Parameter	Description	Min	Typ	Max	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst width		2		ms
t_{PW}	Clock/Data Pulse width		100		ns
t_{CTD}	Clock Pulse to Data Pulse	55.5	64	69.5	µs
t_{CTC}	Clock Pulse to Clock Pulse	111	128	139	µs
	Number of Clock/Data Pulse per FLP Burst	17		33	

Table 17. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

MDC/MDIO Timing

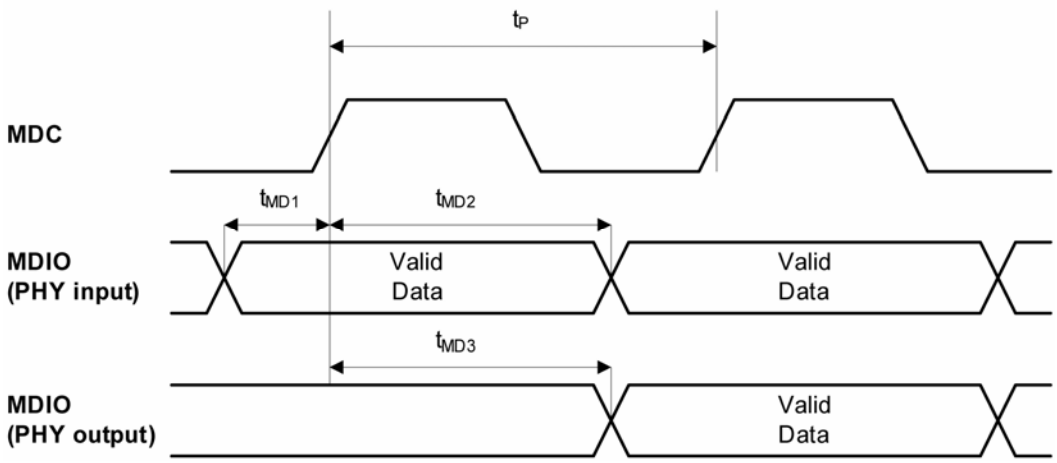


Figure 17. MDC/MDIO Timing

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	MDC period		400		ns
t_{1MD1}	MDIO (PHY input) setup to rising edge of MDC	10			ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	4			ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC * [can vary with MDC clock frequency]		*		ns

Table 18. MDC/MDIO Timing Parameters

Reset Timing

The KSZ8051MNL/RNL reset timing requirement is summarized in the following figure and table.

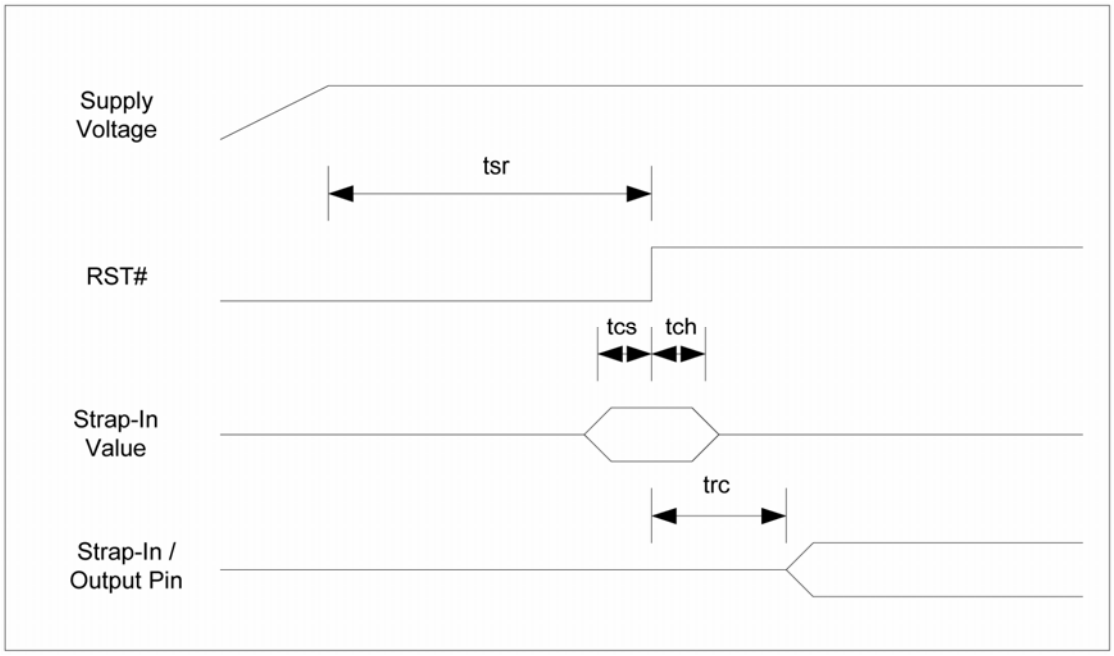


Figure 18. Reset Timing

Parameter	Description	Min	Max	Units
t_{sr}	Stable supply voltage ($V_{DDIO,}$ $V_{DDA\_3.3}$) to reset high	10		ms
t_{cs}	Configuration setup time	5		ns
t_{ch}	Configuration hold time	5		ns
t_{rc}	Reset to strap-in pin output	6		ns

Table 19. Reset Timing Parameters

After the de-assertion of reset, it is recommended to wait a minimum of 100µs before starting programming on the MIIM (MDC/MDIO) Interface.

Reset Circuit

The following reset circuit is recommended for powering up the KSZ8051MNL/RNL if reset is triggered by the power supply.

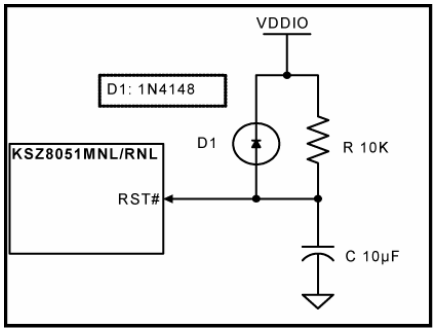


Figure 19. Recommended Reset Circuit

The following reset circuit is recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8051MNL/RNL device. The RST_OUT_n from CPU/FPGA provides the warm reset after power up.

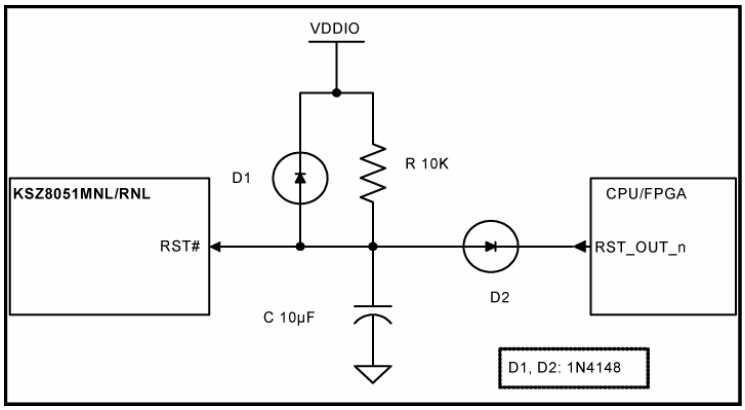


Figure 20. Recommended Reset Circuit for interfacing with CPU/FPGA Reset Output.

Reference Circuits for LED Strapping Pins

The pull-up, float and pull-down reference circuits for the LED1/SPEED and LED0/NWAYEN strapping pins are shown in the following figure.

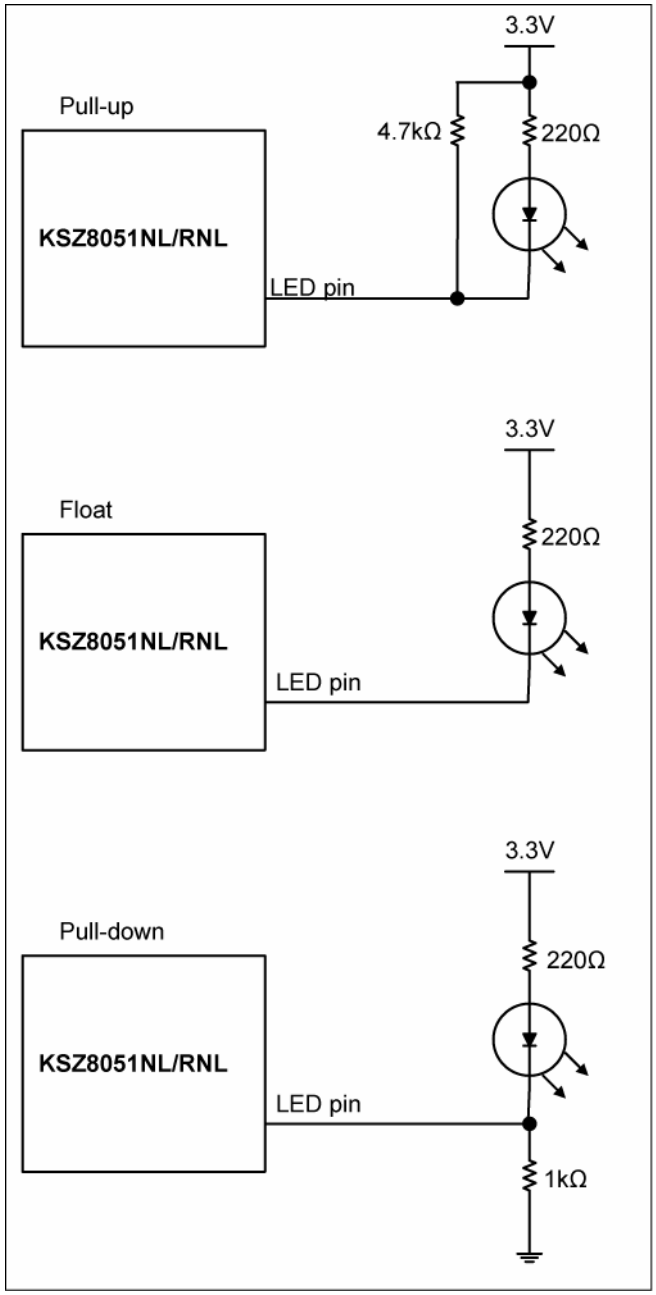


Figure 21. Reference Circuits for LED Strapping Pins

Magnetics Specification

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode chokes is recommended for exceeding FCC requirements.

The following tables list recommended magnetic characteristics and qualified magnetics for the KSZ8051MNL/RNL.

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min.)	350μH	100mV, 100kHz, 8mA
Insertion loss (max.)	-1.0dB	100kHz – 100MHz
HIPOT (min.)	1500Vrms	

Table 20. Magnetics Selection Criteria

Magnetic Manufacturer	Part Number	Auto MDI-X	Number of Port
Bel Fuse	S558-5999-U7	Yes	1
Bel Fuse (Mag Jack)	SI-46001-F	Yes	1
Bel Fuse (Mag Jack)	SI-50170-F	Yes	1
Delta	LF8505	Yes	1
LANKom	LF-H41S-1	Yes	1
Pulse	H1102	Yes	1
Pulse (low cost)	H1260	Yes	1
Transpower	HB726	Yes	1
TDK (Mag Jack)	TLA-6T718A	Yes	1

Table 21. Qualified Single Port 10/100 Magnetics

Reference Clock – Connection and Selection

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ8051MNL/RNL.

For the KSZ8051MNL in all operating modes and for the KSZ8051RNL in RMII – 25MHz Clock Mode, the reference clock is 25 MHz. The reference clock connections to XI (pin 9) and XO (pin 8), and the reference clock selection criteria are provided in the following figure and table.

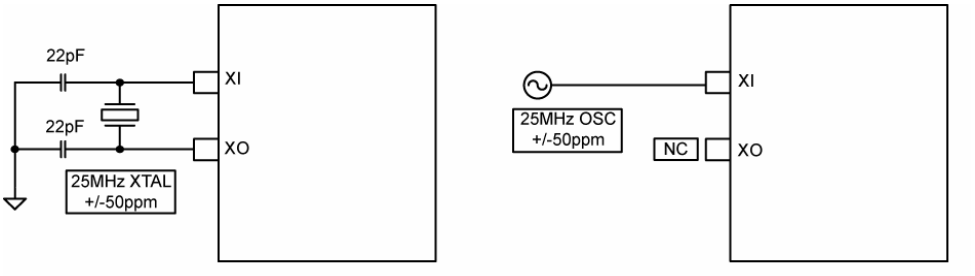


Figure 22. 25MHz Crystal / Oscillator Reference Clock Connection

Characteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max)	±50	ppm

Table 22. 25MHz Crystal / Reference Clock Selection Criteria

For the KSZ8051RNL in RMII – 50MHz Clock Mode, the reference clock is 50 MHz. The reference clock connections to XI (pin 9), and the reference clock selection criteria are provided in the following figure and table.

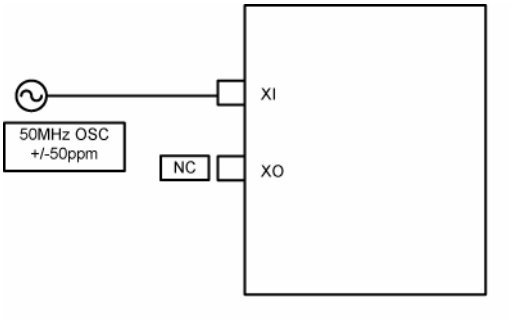
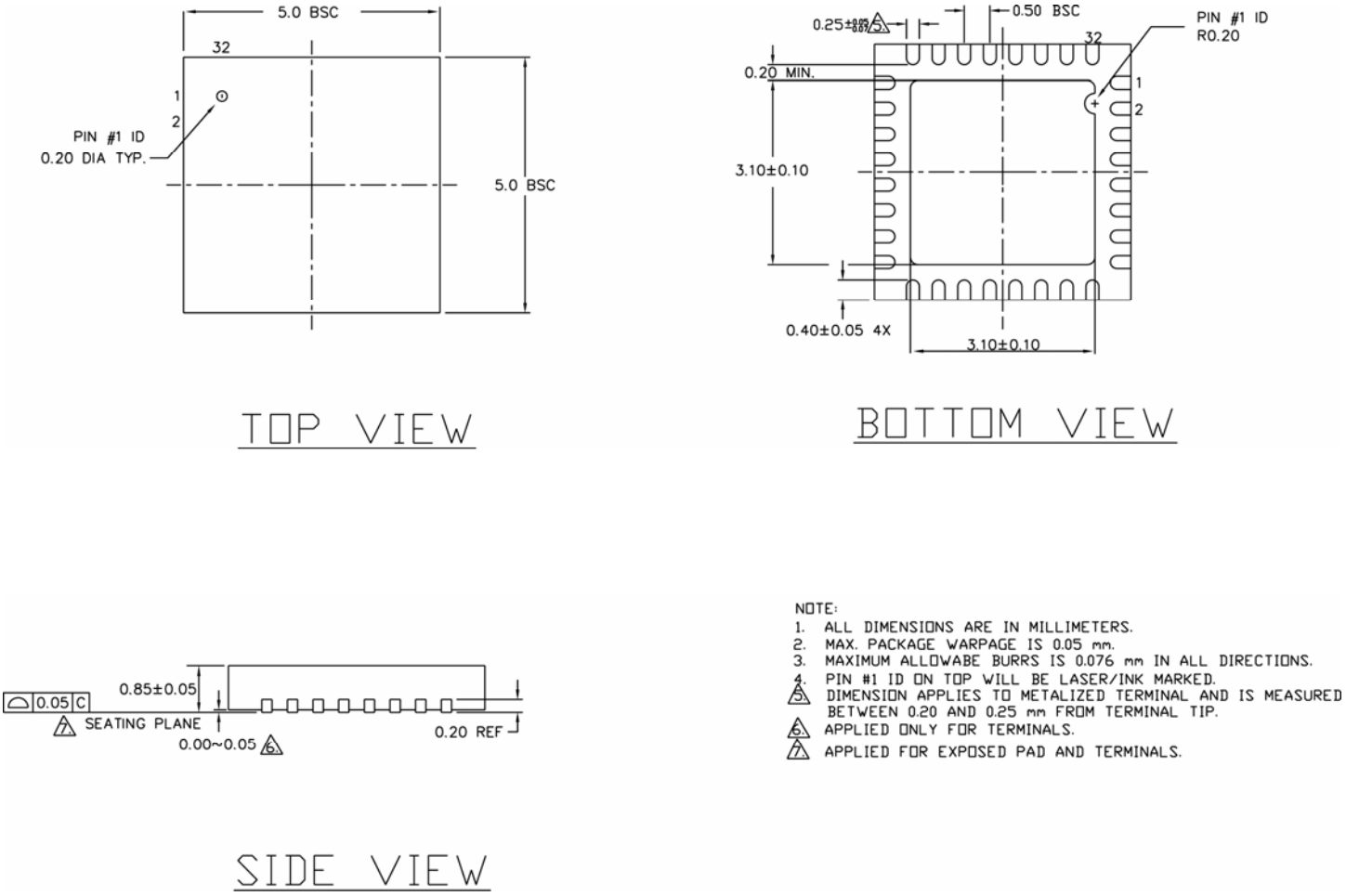


Figure 23. 50MHz Oscillator Reference Clock Connection

Characteristics	Value	Units
Frequency	50	MHz
Frequency tolerance (max)	±50	ppm

Table 23. 50MHz Oscillator / Reference Clock Selection Criteria

Package Information



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