BUK7Y53-100B

N-channel TrenchMOS standard level FET

Rev. 3 — 13 October 2010 | Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Q101 compliant
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive systems
- DC-to-DC converters
- Engine management
- General purpose power switching
- Solenoid drivers
- Transmission control

1.4 Quick reference data

Table 1. Quick reference data

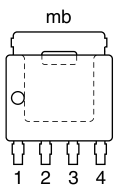
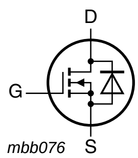
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	100	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1; see Figure 4	-	-	24.8	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	85	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A; $T_j = 25$ °C; see Figure 12; see Figure 13	-	40	53	mΩ

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 24.8 A; $V_{sup} \leq$ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	81	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	I_D = 10 A; V_{DS} = 80 V; V_{GS} = 10 V; see Figure 14	-	8.5	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	c	source	 SOT669 (LFPAK)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y53-100B	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 4	-	24.8	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V; see Figure 1	-	17.6	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 4	-	99	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	85	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	24.8	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C	-	99	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 24.8$ A; $V_{sup} \leq 100$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped	-	81	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3 [1][2][3]	-	-	J

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[2] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[3] Refer to application note AN10273 for further information.

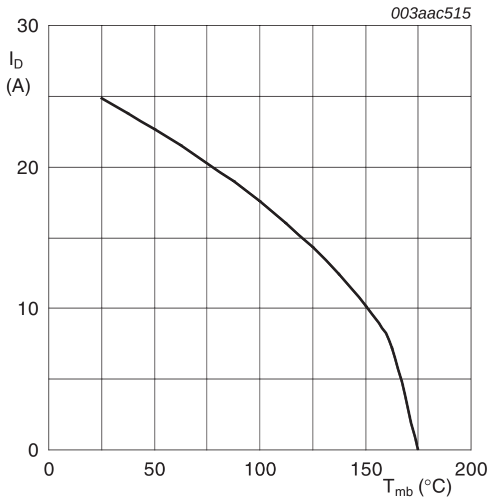
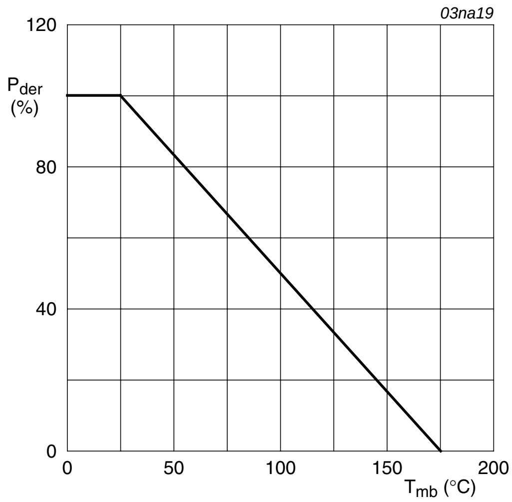


Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

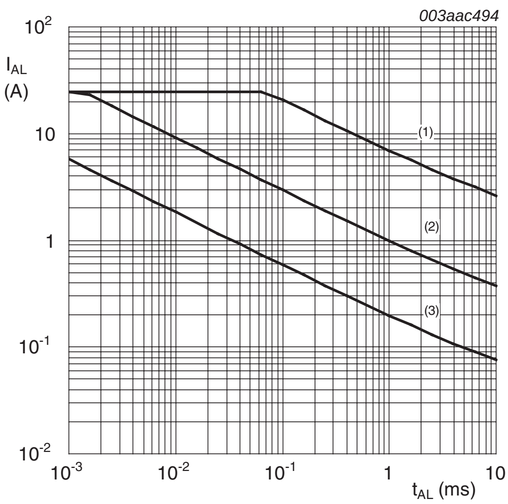
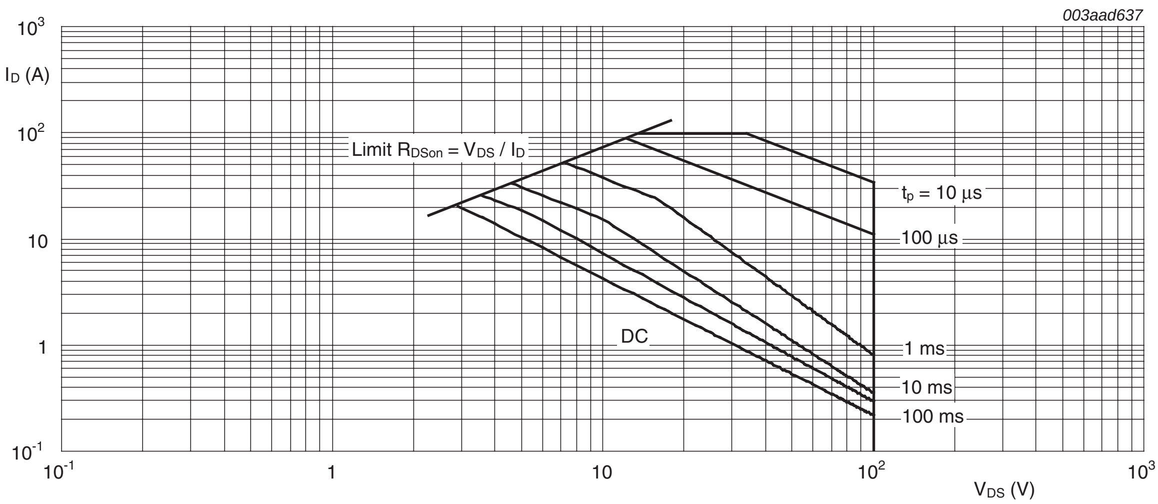


Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



$T_{mb} = 25\,°C; I_{DM}$ is single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	1.76	K/W

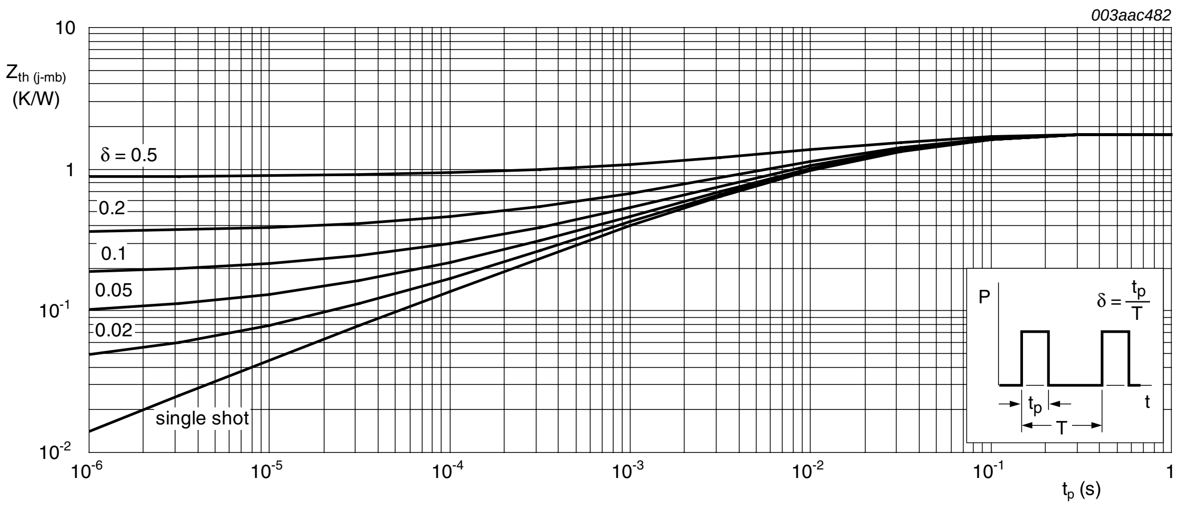
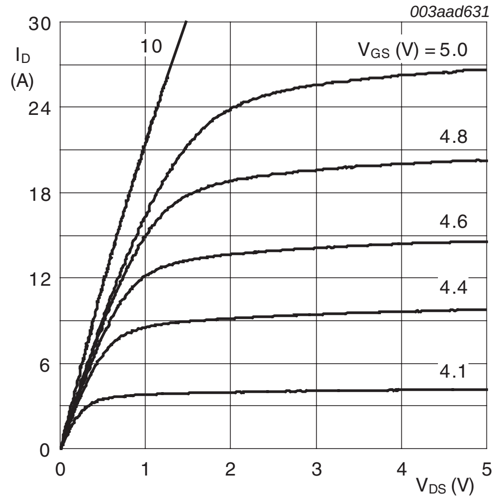


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

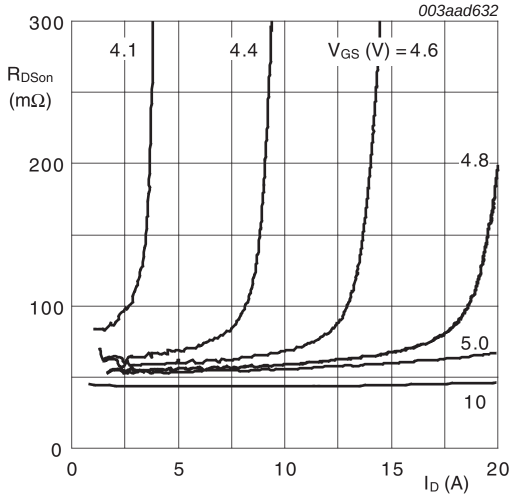
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10; see Figure 11	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 10	-	-	4.4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 10	1	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -20 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 175 °C; see Figure 12; see Figure 13	-	-	138	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; see Figure 12; see Figure 13	-	40	53	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 80 V; V_{GS} = 10 V; see Figure 14	-	22	-	nC
Q_{GS}	gate-source charge		-	4.3	-	nC
Q_{GD}	gate-drain charge		-	8.5	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	1100	1467	pF
C_{oss}	output capacitance		-	142	170	pF
C_{rss}	reverse transfer capacitance		-	63	86	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 3 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω	-	15.3	-	ns
t_r	rise time		-	7.8	-	ns
$t_{d(off)}$	turn-off delay time		-	34	-	ns
t_f	fall time		-	7.7	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 25 V; T_j = 25 °C; see Figure 16	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V	-	56	-	ns
Q_r	recovered charge		-	155	-	nC



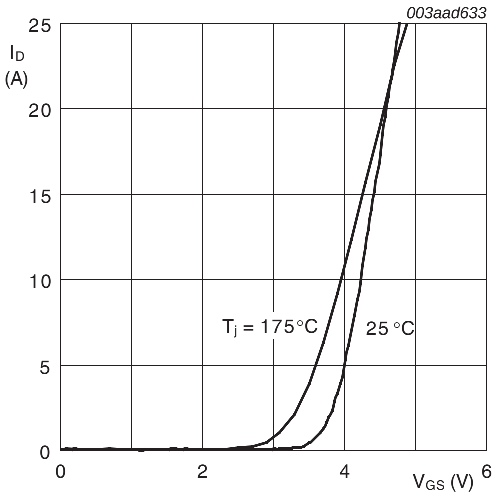
$T_j = 25°C$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



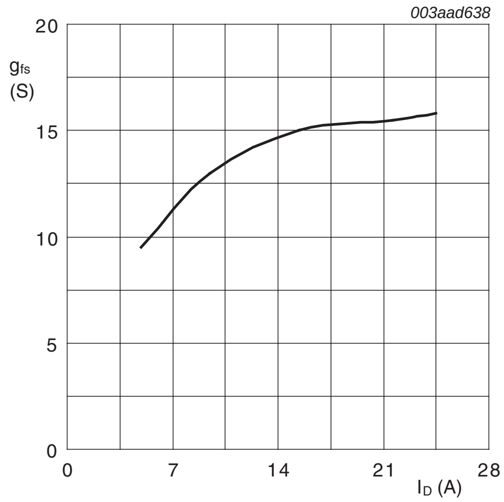
$T_j = 25°C$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



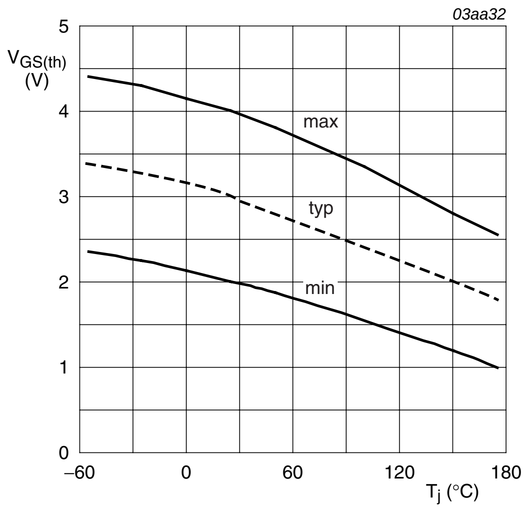
$V_{DS} = 25V$

Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



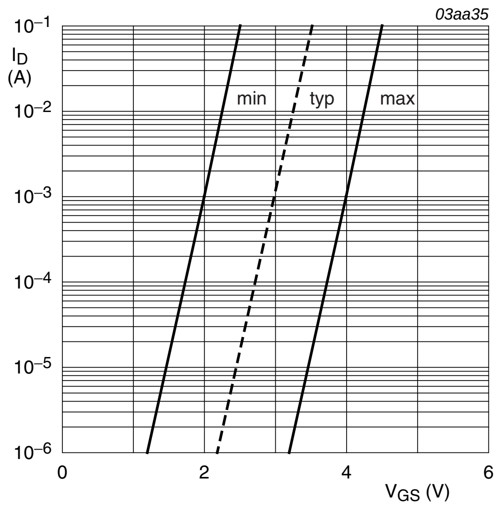
$T_j = 25°C; V_{DS} = 25V$

Fig 9. Forward transconductance as a function of drain current; typical values.



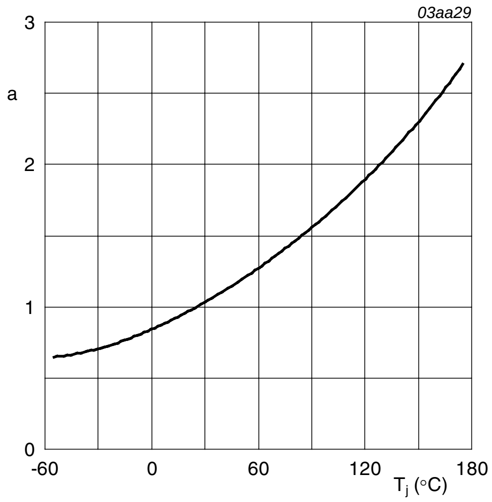
$$I_D = 1mA; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



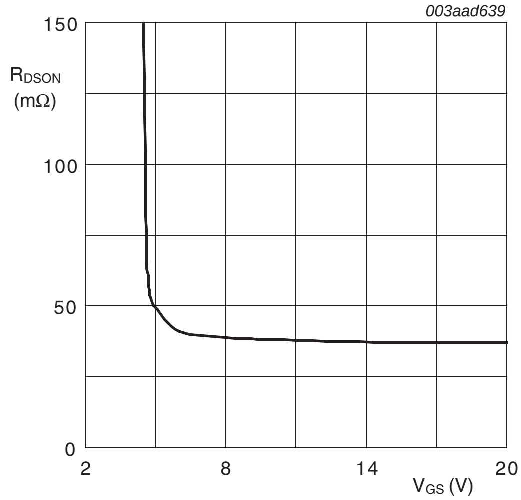
$$T_j = 25\,°C; V_{DS} = 5V$$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



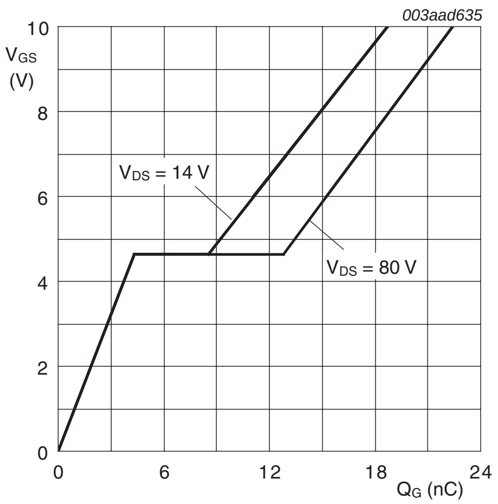
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



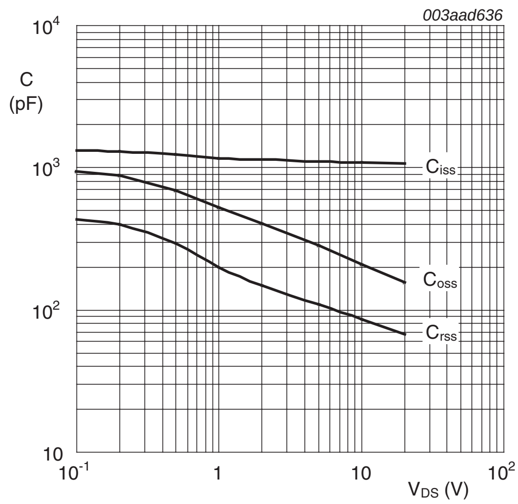
$$T_j = 25\,°C; I_D = 10A$$

Fig 13. Drain-source on-state resistance as a function of gate-source voltage; typical values.



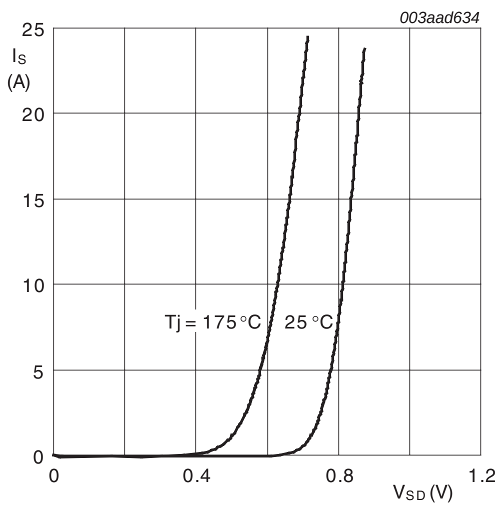
$$T_j = 25\,°C; I_D = 10\,A$$

Fig 14. Gate-source voltage as a function of gate charge; typical values.



$$V_{GS} = 0\,V; f = 1\,MHz$$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

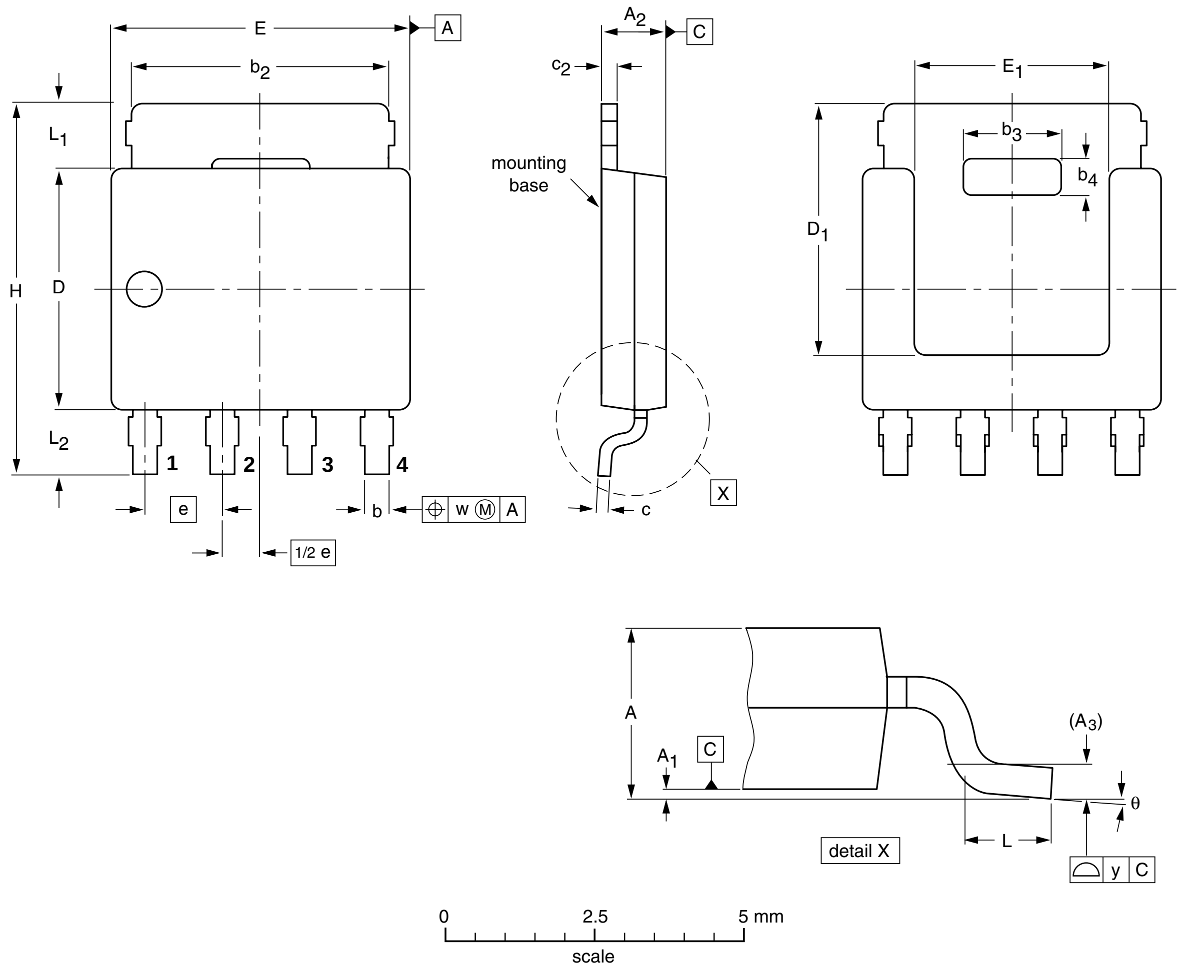


$$V_{GS} = 0\,V$$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	$D^{(1)}$	$D_1^{(1)}$ max	$E^{(1)}$	$E_1^{(1)}$	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~04-10-13~~ 06-03-16

Fig 17. Package outline SOT669 (LFPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7Y53-100B v.3	20101013	Product data sheet	-	BUK7Y53-100B_2
Modifications:	• Status changed from objective to product.			
BUK7Y53-100B_2	20100211	Objective data sheet	-	BUK7Y53-100B_1

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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