



PMCXB900UE

20 V, complementary N/P-channel Trench MOSFET

30 June 2015

Product data sheet

1. General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Very low threshold voltage for portable applications: $V_{GS(th)} = 0.7\text{ V}$
- Leadless ultra small and ultra thin SMD plastic package: $1.1 \times 1.0 \times 0.37\text{ mm}$
- ElectroStatic Discharge (ESD) protection $> 1\text{ kV HBM}$

3. Applications

- Relay driver
- High-speed line driver
- Level shifter
- Power management in battery-driven portables

4. Quick reference data

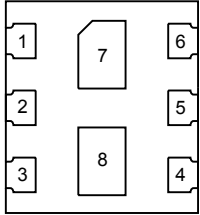
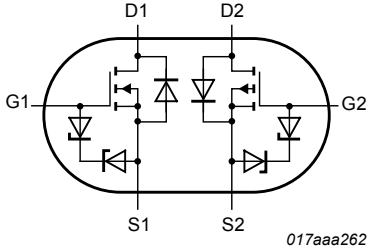
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 600\text{ mA}; T_j = 25\text{ }^\circ\text{C}$	-	470	620	m Ω
TR2 (P-channel), Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -500\text{ mA}; T_j = 25\text{ }^\circ\text{C}$	-	1.02	1.4	Ω
TR1 (N-channel)						
V_{DS}	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	20	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$	[1]	-	600	mA
TR2 (P-channel)						
V_{DS}	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	-20	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$	[1]	-	-500	mA



[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view DFN1010B-6 (SOT1216)</p>	 <p>017aaa262</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

5. Ordering information

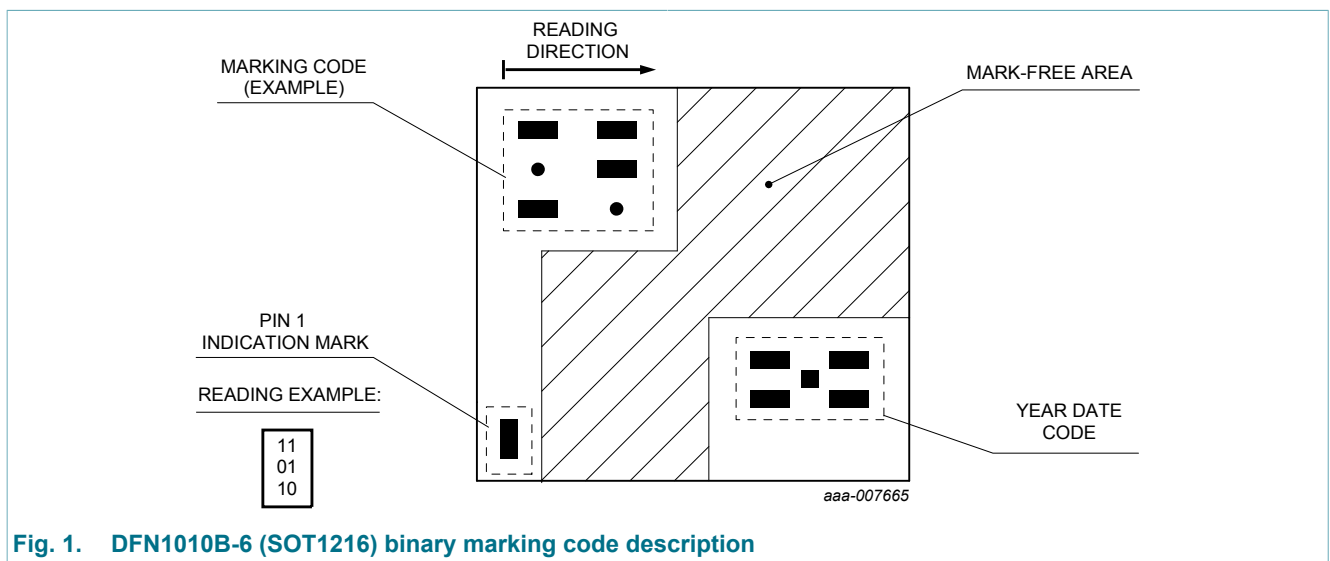
Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMCXB900UE	DFN1010B-6	DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

6. Marking

Table 4. Marking codes

Type number	Marking code
PMCXB900UE	10 00 00



7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1 (N-channel)						
V _{DS}	drain-source voltage	T _j = 25 °C		-	20	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	600	mA
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	400	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	2.5	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	265	mW
			[1]	-	380	mW
		T _{sp} = 25 °C		-	4025	mW
TR1 (N-channel), Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	400	mA
TR2 (P-channel)						
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-500	mA
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-300	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-2	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	265	mW
			[1]	-	380	mW
		T _{sp} = 25 °C		-	4025	mW
TR2 (P-channel), Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-350	mA
Per device						
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

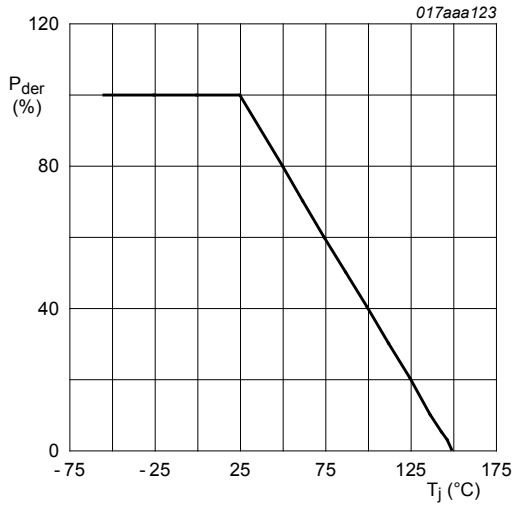


Fig. 2. MOSFET transistor: Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

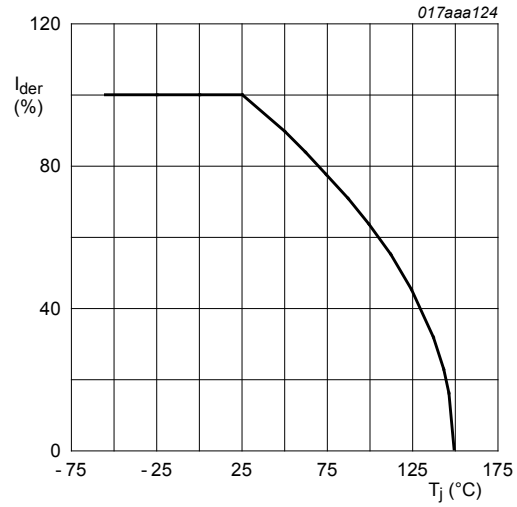
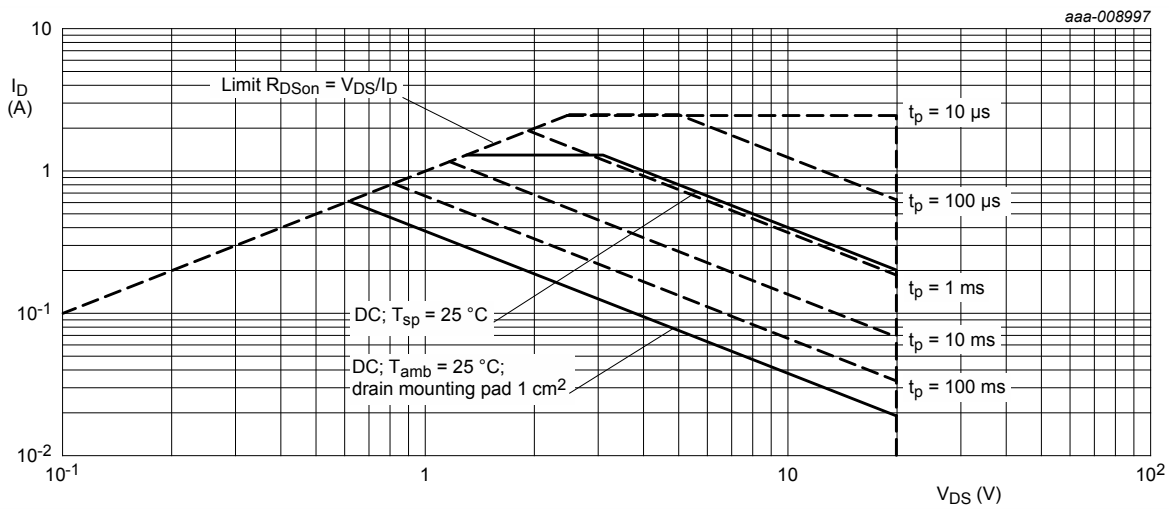


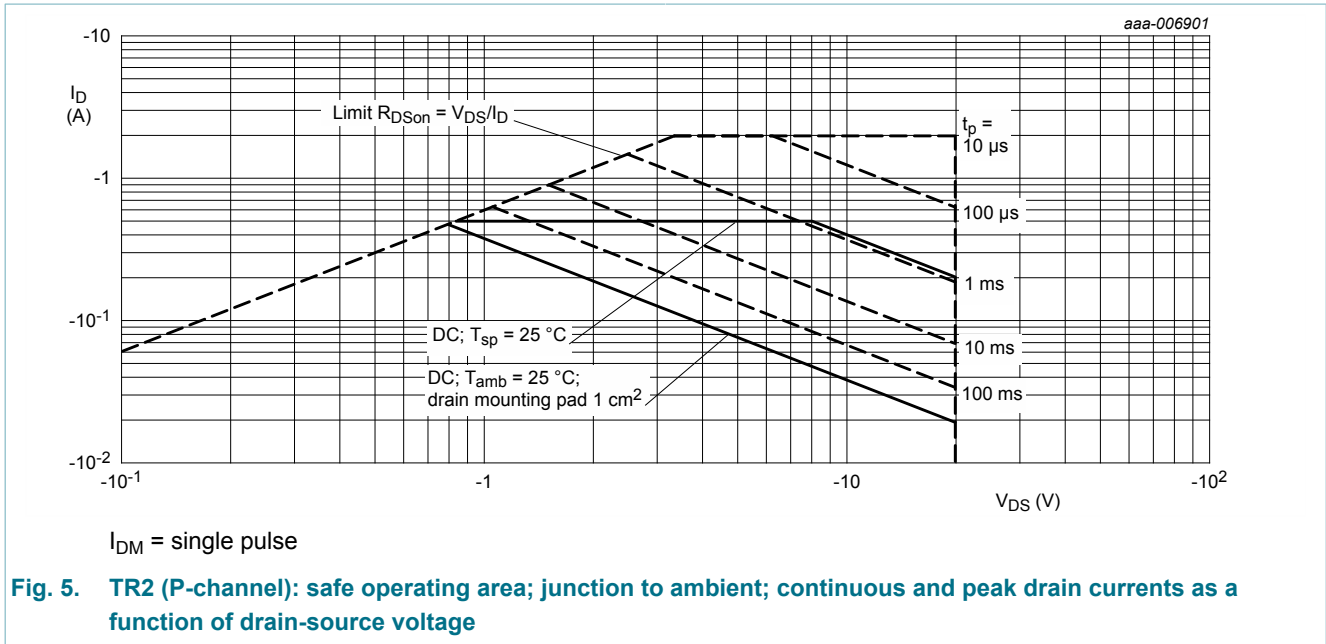
Fig. 3. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$



I_{DM} = single pulse

Fig. 4. TR1 (N-channel): safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage



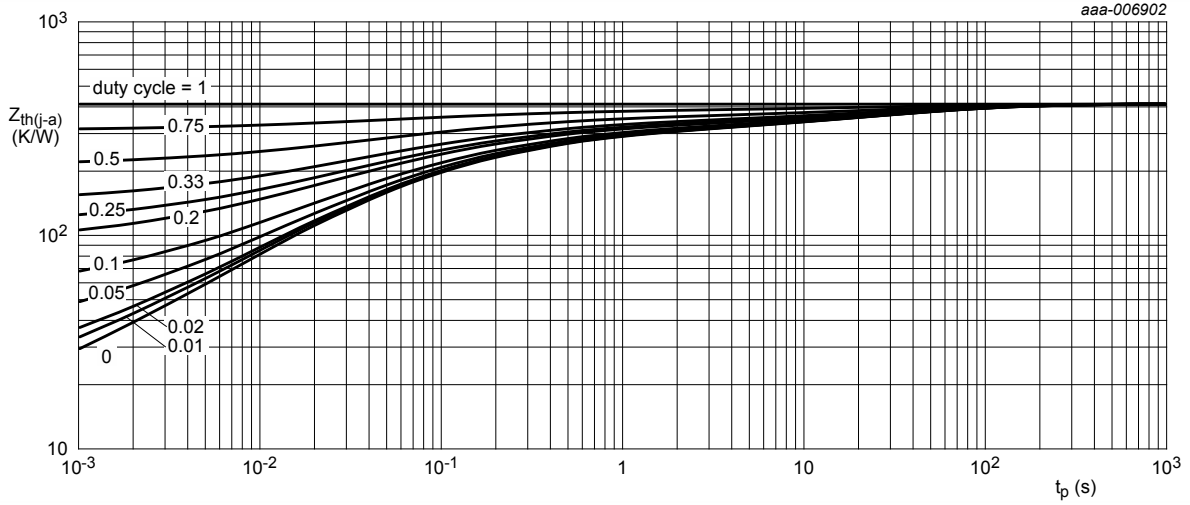
8. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (N-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	410	475	K/W
			[2]	-	285	330	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	27	31	K/W
TR2 (P-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	410	475	K/W
			[2]	-	285	330	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	27	31	K/W

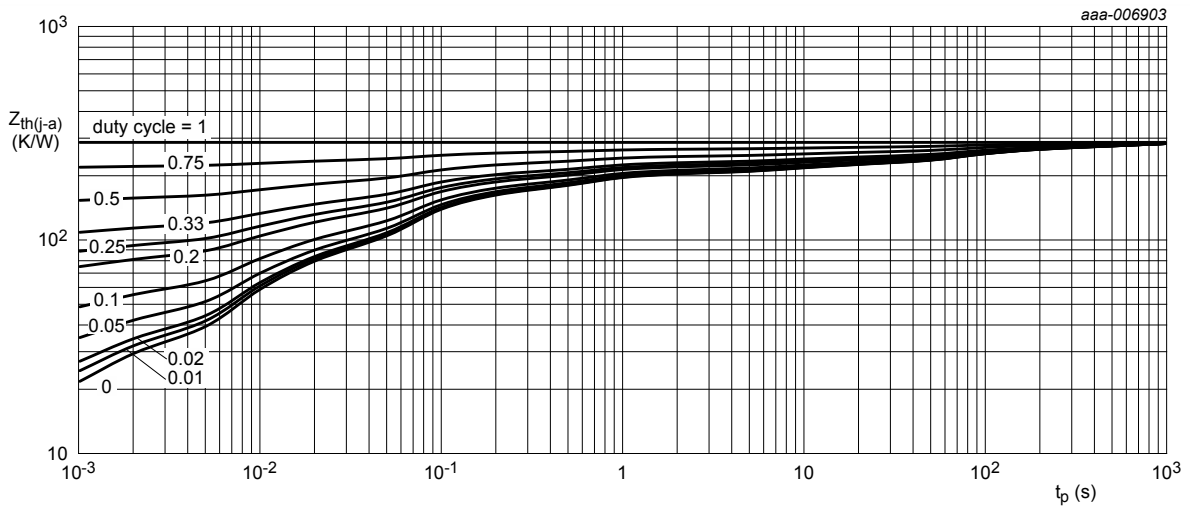
[1] Device mounted on an FR4 PCB, single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .



FR4 PCB, standard footprint

Fig. 6. TR1 and TR2: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig. 7. TR1 and TR2: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

9. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	0.45	0.7	0.95	V
I_{DSS}	drain leakage current	$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 600 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	470	620	m Ω
		$V_{GS} = 4.5 V; I_D = 600 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	760	1000	m Ω
		$V_{GS} = 2.5 V; I_D = 500 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	620	850	m Ω
		$V_{GS} = 1.8 V; I_D = 100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	845	1300	m Ω
		$V_{GS} = 1.5 V; I_D = 10 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1125	3000	m Ω
		$V_{GS} = 1.2 V; I_D = 1 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2210	-	m Ω
g_{fs}	transfer conductance	$V_{DS} = 5 V; I_D = 600 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1	-	S
TR1 (N-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 V; I_D = 600 \text{ mA}; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$	-	0.4	0.7	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.1	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	21.3	-	pF
C_{oss}	output capacitance		-	5.4	-	pF
C_{rss}	reverse transfer capacitance		-	4.2	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 V; I_D = 600 \text{ mA}; V_{GS} = 4.5 V; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	5.6	-	ns
t_r	rise time		-	9.2	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
t_f	fall time		-	51	-	ns
TR1 (N-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = 360 \text{ mA}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.8	1.2	V

20 V, complementary N/P-channel Trench MOSFET

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR2 (P-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.45	-0.7	-0.95	V
I_{DSS}	drain leakage current	$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -500 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.02	1.4	Ω
		$V_{GS} = -4.5 V; I_D = -500 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	1.54	2.1	Ω
		$V_{GS} = -2.5 V; I_D = -200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.27	2.2	Ω
		$V_{GS} = -1.8 V; I_D = -40 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.7	3.3	Ω
		$V_{GS} = -1.5 V; I_D = -10 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2.3	5	Ω
		$V_{GS} = -1.2 V; I_D = -1 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	3.5	-	Ω
g_{fs}	transfer conductance	$V_{DS} = -10 V; I_D = -500 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	480	-	mS
TR2 (P-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V; I_D = -450 \text{ mA}; V_{GS} = -4.5 V; T_j = 25 \text{ }^\circ C$	-	1.19	2.1	nC
Q_{GS}	gate-source charge		-	0.17	-	nC
Q_{GD}	gate-drain charge		-	0.1	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	43	-	pF
C_{oss}	output capacitance		-	14	-	pF
C_{rss}	reverse transfer capacitance		-	8	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = -10 V; I_D = -450 \text{ mA}; V_{GS} = -4.5 V; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	2.3	-
t_r	rise time	$V_{GS} = -4.5 V; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	5	-	ns
$t_{d(off)}$	turn-off delay time		-	13.5	-	ns
t_f	fall time		-	6	-	ns
TR2 (P-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = -115 \text{ mA}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-0.7	-1.2	V

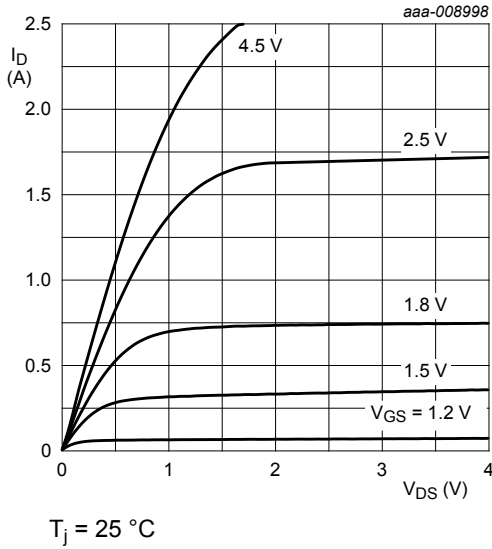


Fig. 8. TR1: output characteristics; drain current as a function of drain-source voltage; typical values

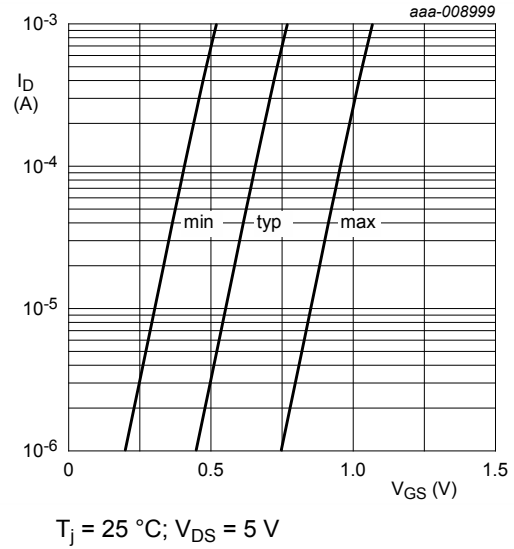


Fig. 9. TR1: sub-threshold drain current as a function of gate-source voltage

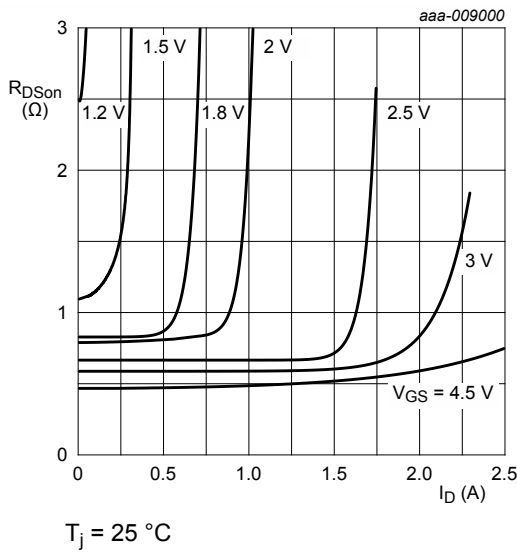


Fig. 10. TR1: drain-source on-state resistance as a function of drain current; typical values

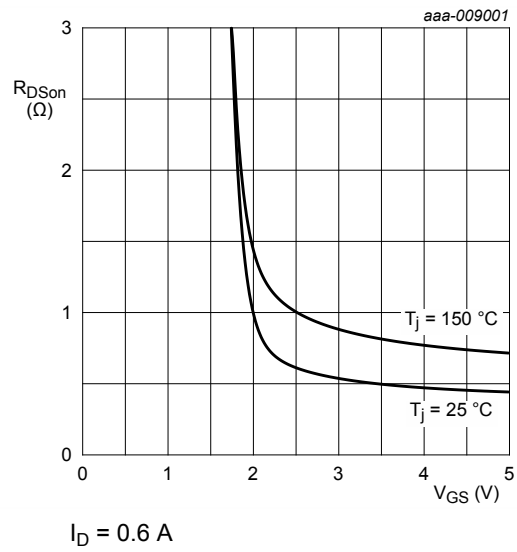
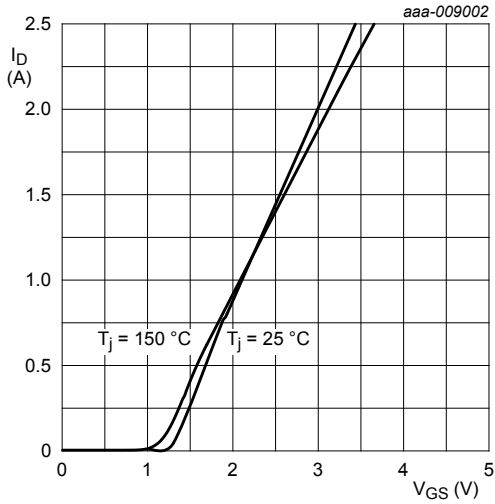


Fig. 11. TR1: drain-source on-state resistance as a function of gate-source voltage; typical values



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 12. TR1: transfer characteristics; drain current as a function of gate-source voltage; typical values

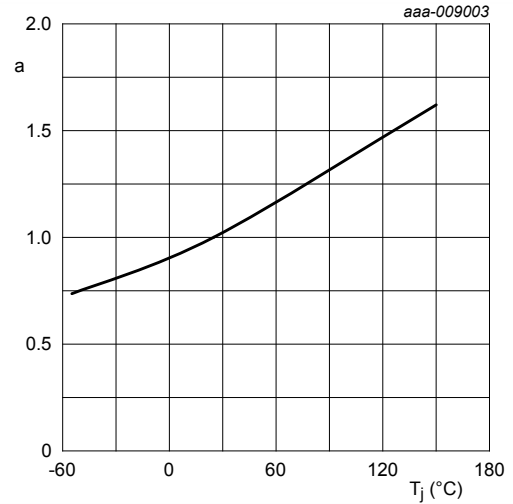
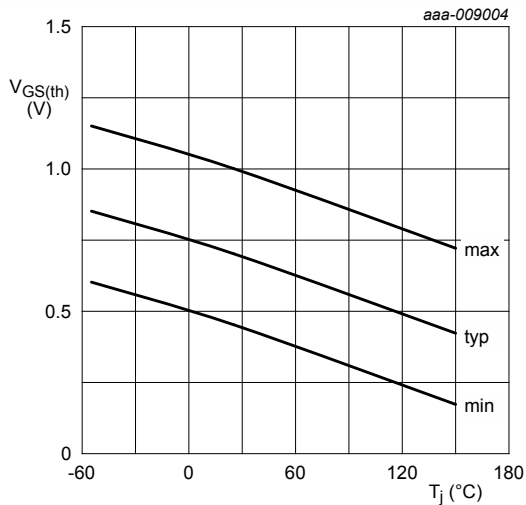


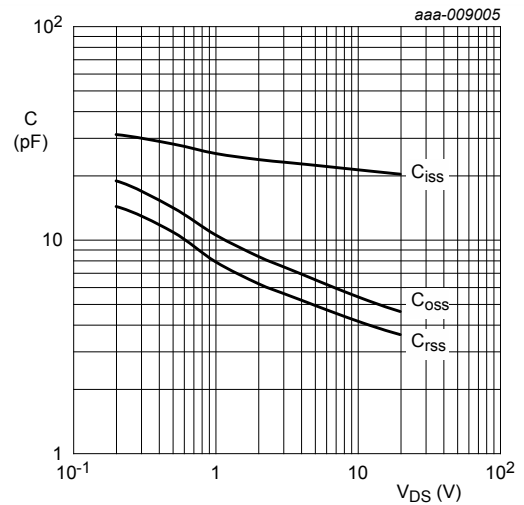
Fig. 13. TR1: normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



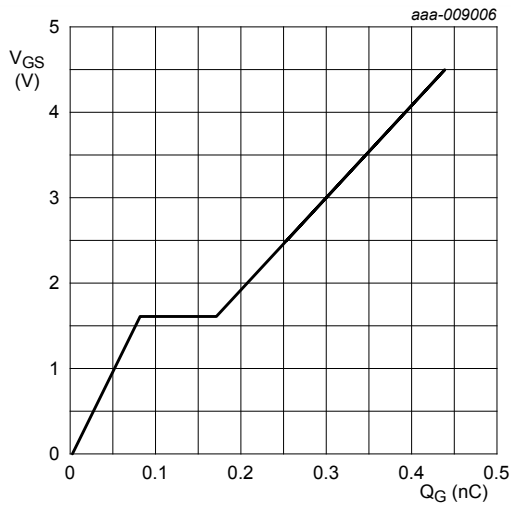
$$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$$

Fig. 14. TR1: gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 15. TR1: input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 0.6 \text{ A}; V_{DS} = 10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 16. TR1: gate-source voltage as a function of gate charge; typical values

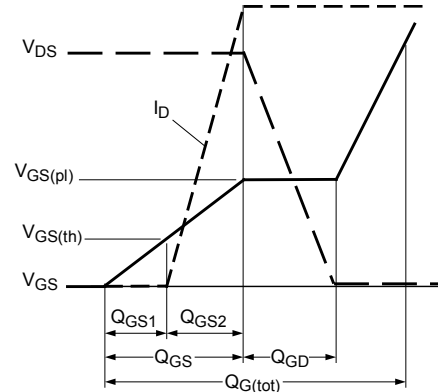
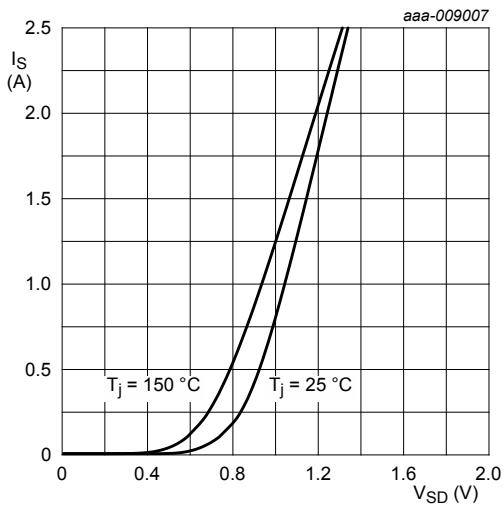
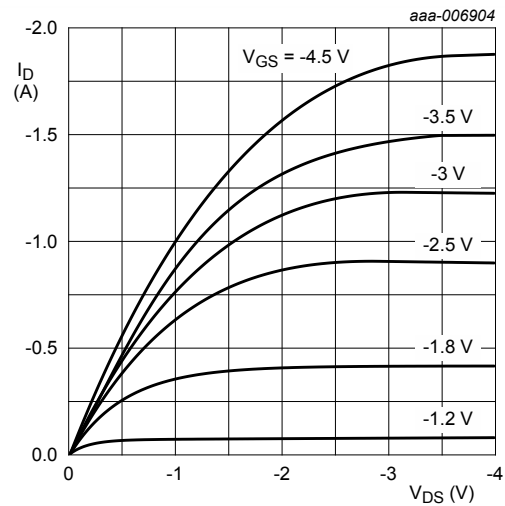


Fig. 17. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 18. TR1: source current as a function of source-drain voltage; typical values



$T_j = 25 \text{ }^\circ\text{C}$

Fig. 19. TR2: output characteristics; drain current as a function of drain-source voltage; typical values

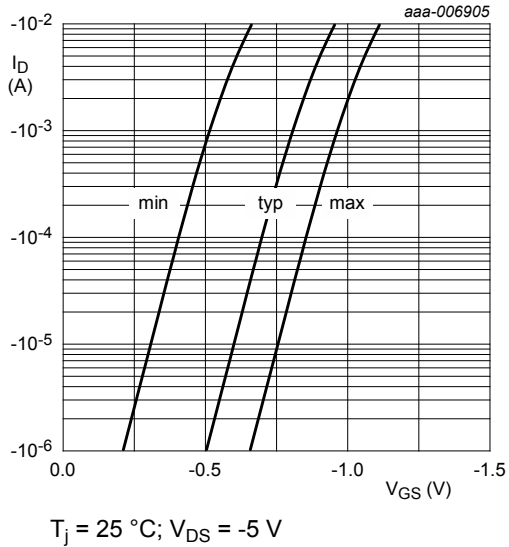


Fig. 20. TR2: sub-threshold drain current as a function of gate-source voltage

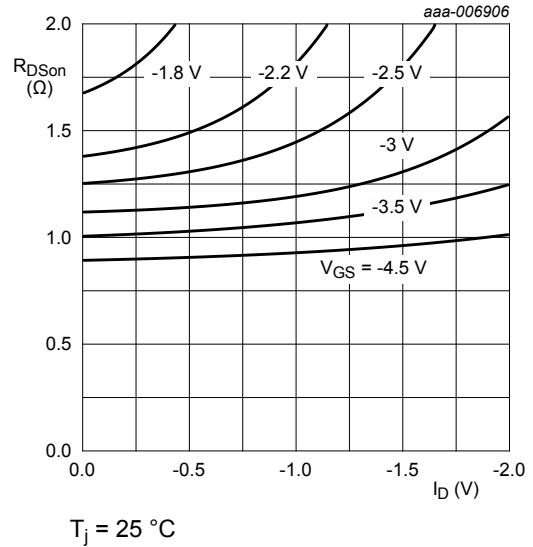


Fig. 21. TR2: drain-source on-state resistance as a function of drain current; typical values

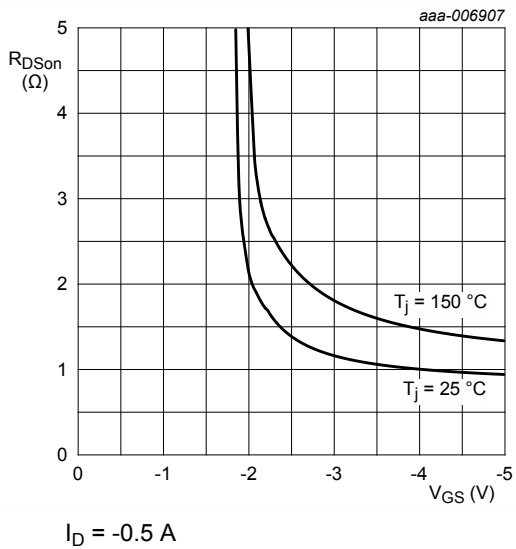


Fig. 22. TR2: drain-source on-state resistance as a function of gate-source voltage; typical values

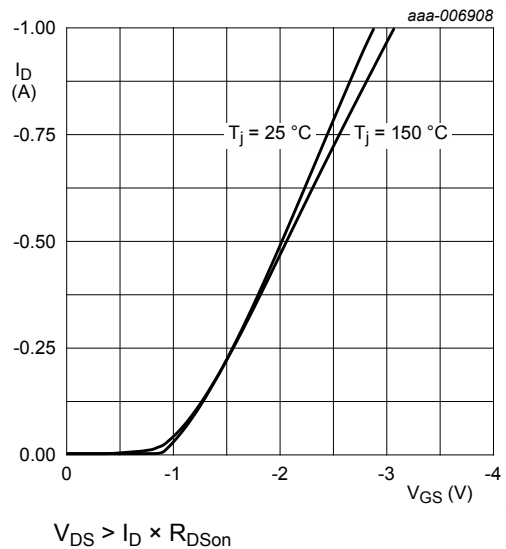


Fig. 23. TR2: transfer characteristics; drain current as a function of gate-source voltage; typical values

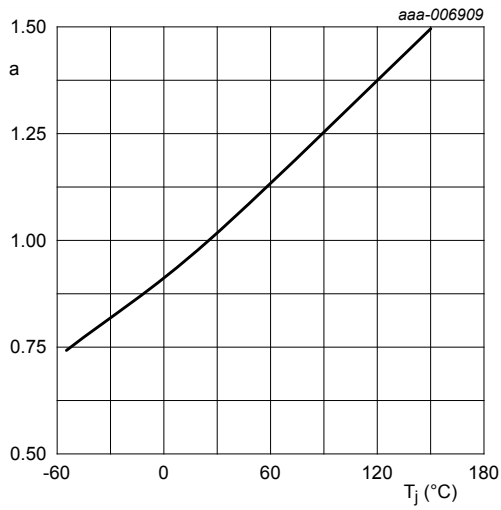
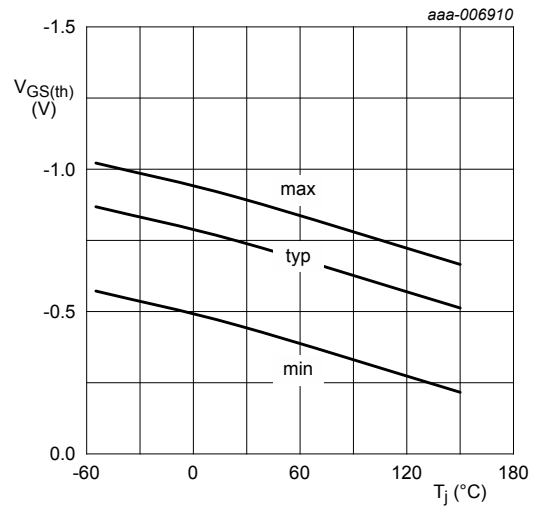


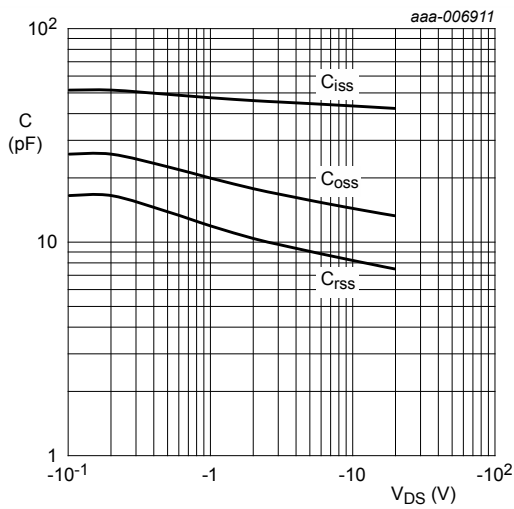
Fig. 24. TR2: normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ C)}}$$



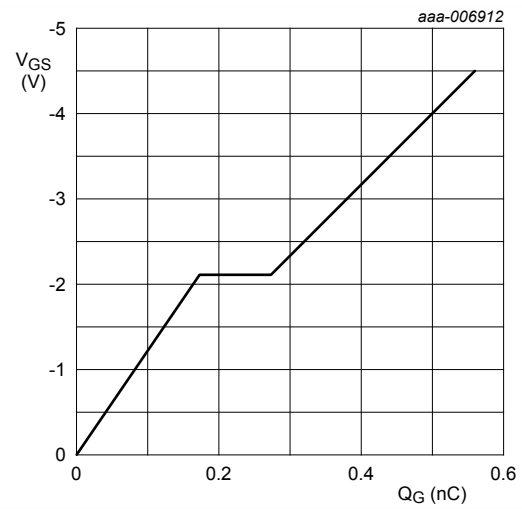
I_D = -0.25 mA; V_{DS} = V_{GS}

Fig. 25. TR2: gate-source threshold voltage as a function of junction temperature



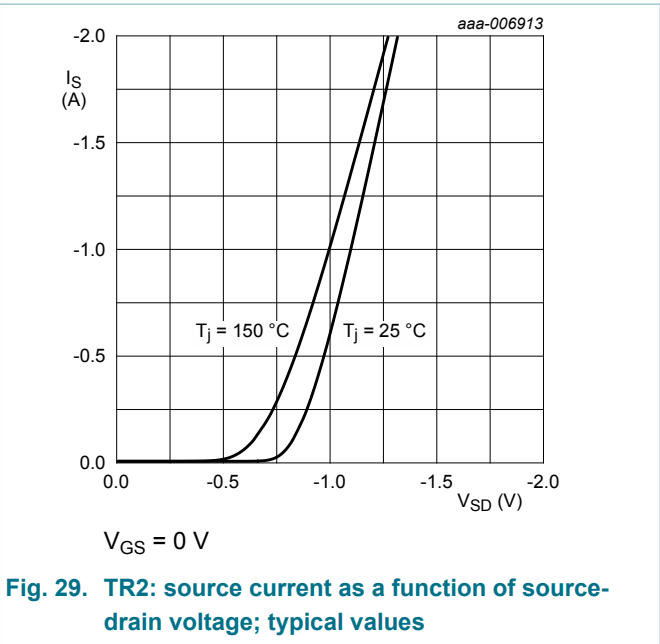
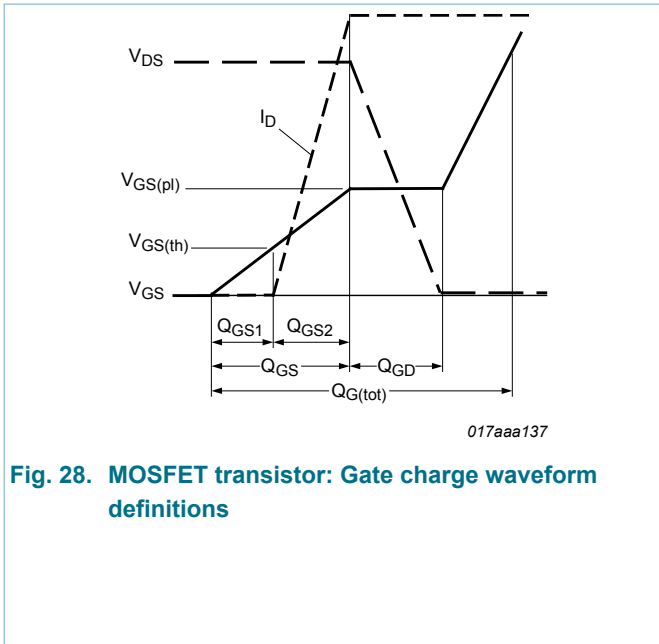
f = 1 MHz; V_{GS} = 0 V

Fig. 26. TR2: input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

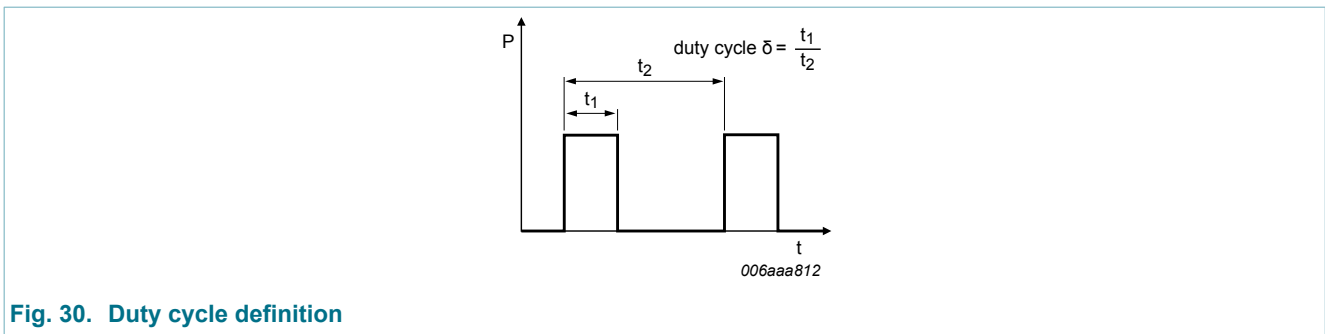


I_D = -0.45 A; V_{DS} = -10 V; T_{amb} = 25 °C

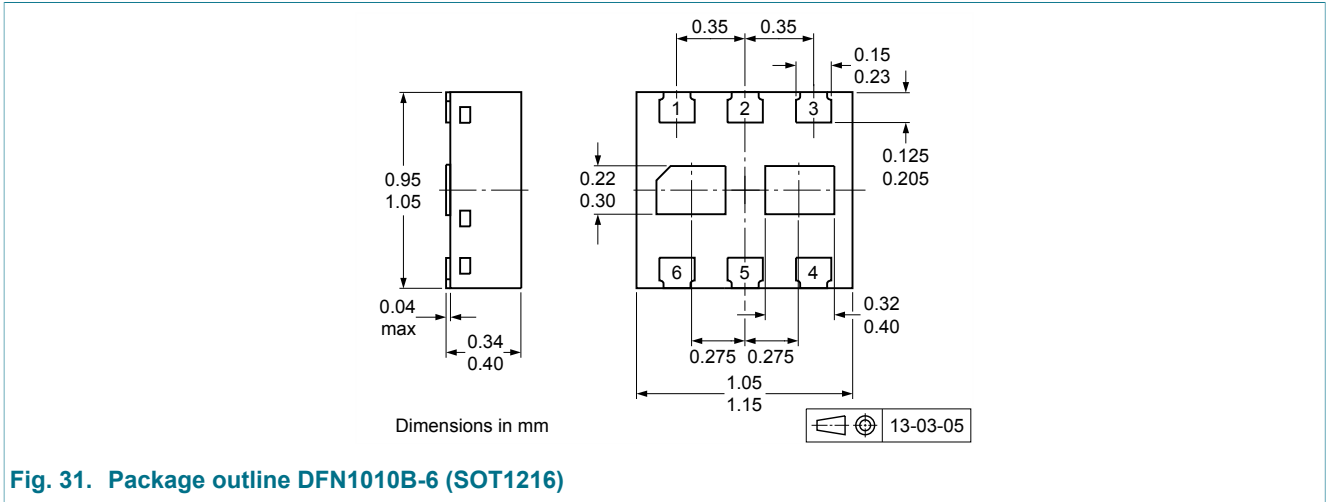
Fig. 27. TR2: gate-source voltage as a function of gate charge; typical values



10. Test information



11. Package outline



12. Soldering

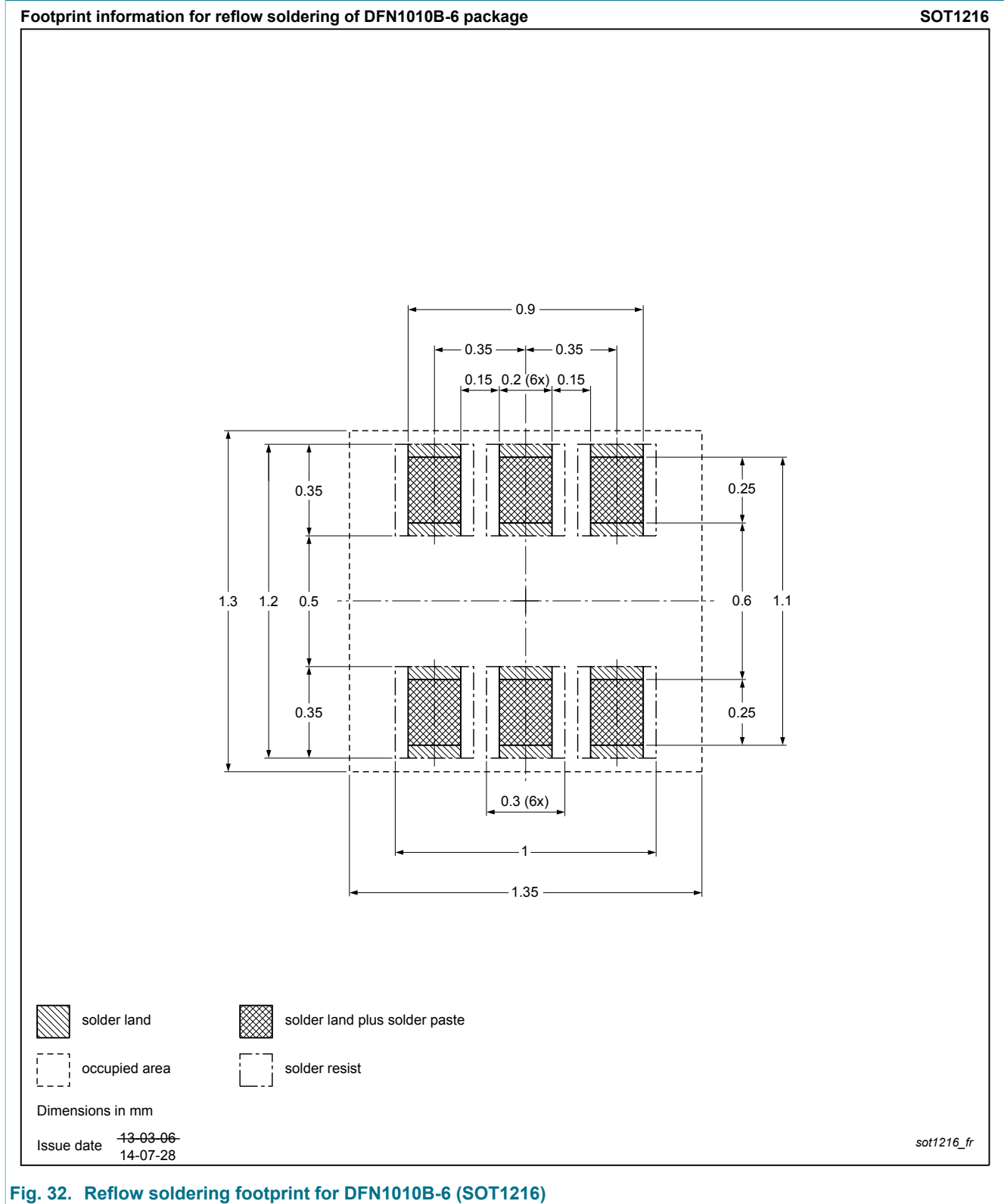


Fig. 32. Reflow soldering footprint for DFN1010B-6 (SOT1216)

13. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCXB900UE v.2	20150630	Product data sheet	-	PMCXB900UE v.1
Modification:	<ul style="list-style-type: none">Change of binary marking code position.			
PMCXB900UE v.1	20131007	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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