



PSMN022-30BL

N-channel 30 V 22.6 mΩ logic level MOSFET in D2PAK

Rev. 1 — 21 March 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

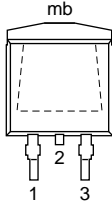
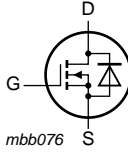
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	-	-	30	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	41	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 100\text{ °C};$ see Figure 13	-	26.84	31.6	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C};$ see Figure 12	-	19.17	22.6	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 5\text{ A}; V_{DS} = 15\text{ V};$ see Figure 14 ; see Figure 15	-	1.4	-	nC
$Q_{G(tot)}$	total gate charge		-	4.4	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 30\text{ A};$ $V_{sup} \leq 30\text{ V}; R_{GS} = 50\text{ Ω};$ unclamped	-	-	7	mJ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN022-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

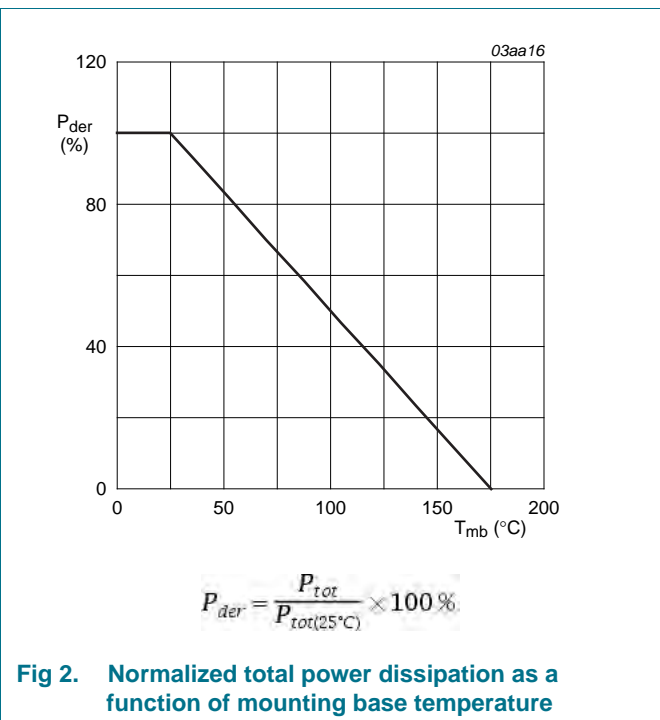
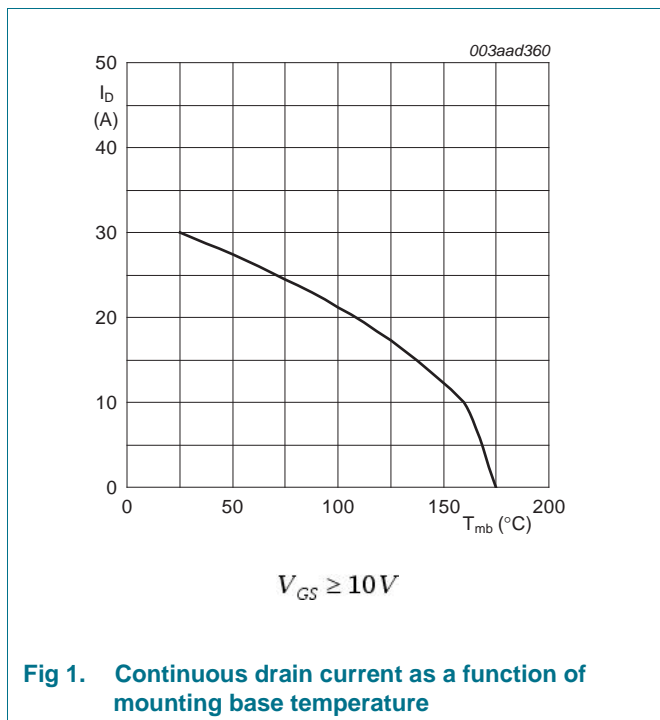
Type number	Marking code
PSMN022-30BL	PSMN022-30BL

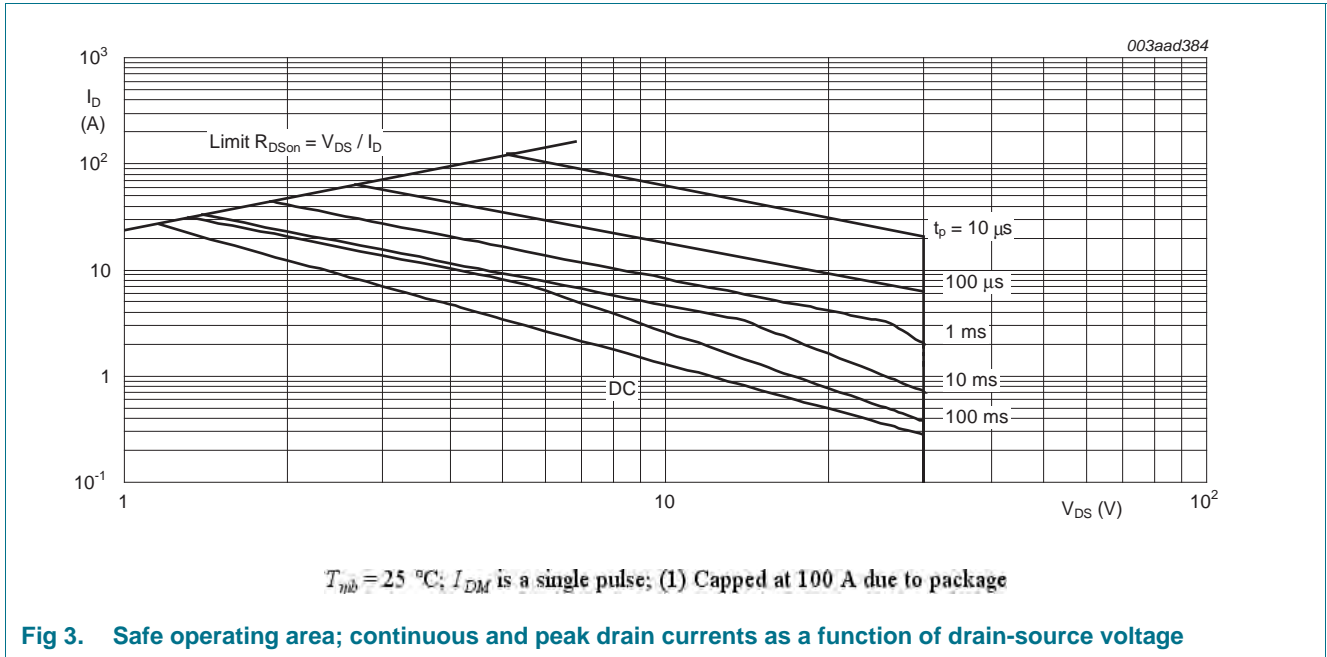
5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$; see Figure 1	-	22	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$; see Figure 1	-	30	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	125	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	41	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	30	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	125	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 30\text{ A}; V_{sup} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega$; unclamped	-	7	mJ

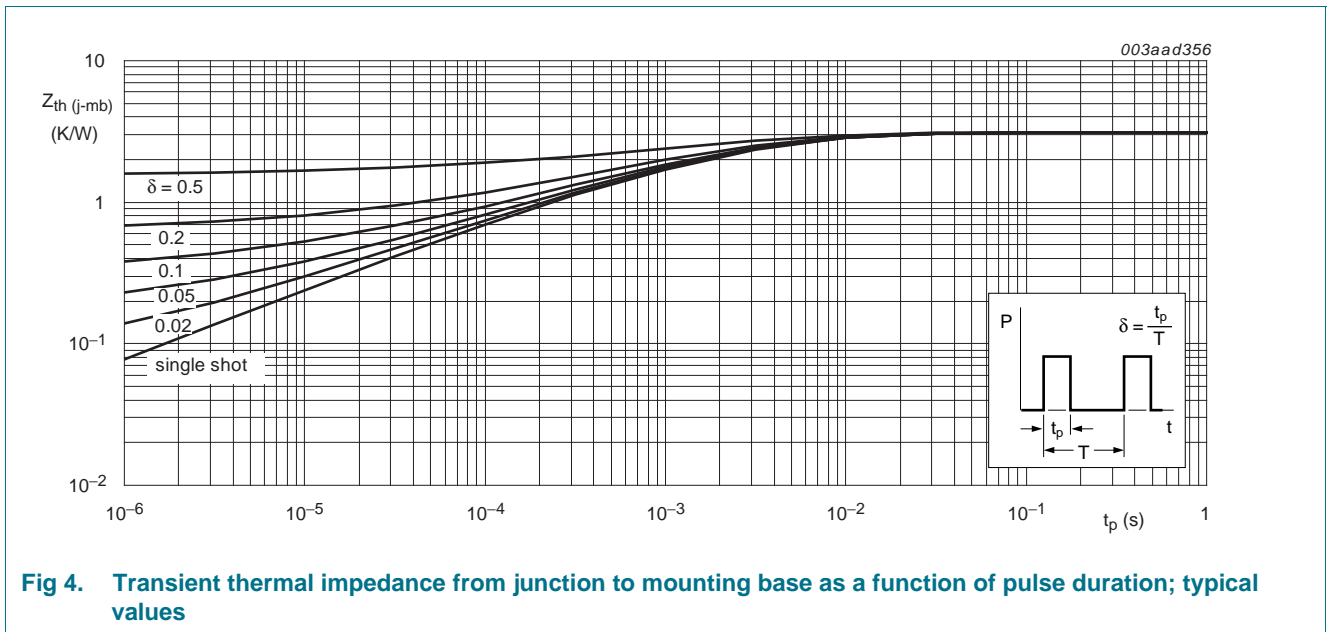




6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	3.1	3.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed circuit board	-	50	-	K/W



7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 10 ; see Figure 11	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 11	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 11	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.3	1	μA
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	-	50	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 \text{ }^\circ C$; see Figure 12	-	25.17	29.6	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 175 \text{ }^\circ C$; see Figure 13 ; see Figure 12	-	50.99	60	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 100 \text{ }^\circ C$; see Figure 13	-	26.84	31.6	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 25 \text{ }^\circ C$; see Figure 12	-	19.17	22.6	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	2	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 5 A; V_{DS} = 15 V; V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	9	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	8	-	nC
		$I_D = 5 A; V_{DS} = 15 V; V_{GS} = 4.5 V$; see Figure 14 ; see Figure 15	-	4.4	-	nC
Q_{GS}	gate-source charge		-	1.6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	0.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.8	-	nC
Q_{GD}	gate-drain charge		-	1.4	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 5 A; V_{DS} = 15 V$; see Figure 14 ; see Figure 15	-	3	-	V
C_{iss}	input capacitance	$V_{DS} = 15 V; V_{GS} = 0 V; f = 1 \text{ MHz}$;	-	447	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ C$; see Figure 16	-	96	-	pF
C_{rss}	reverse transfer capacitance		-	61	-	pF

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 1.5\ \Omega; V_{GS} = 4.5\text{ V};$	-	12	-	ns
t_r	rise time	$R_{G(ext)} = 4.7\ \Omega$	-	29	-	ns
$t_{d(off)}$	turn-off delay time		-	17	-	ns
t_f	fall time		-	7	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 17	-	0.7	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	22	-	ns
Q_r	recovered charge	$V_{DS} = 15\text{ V}$	-	10	-	nC

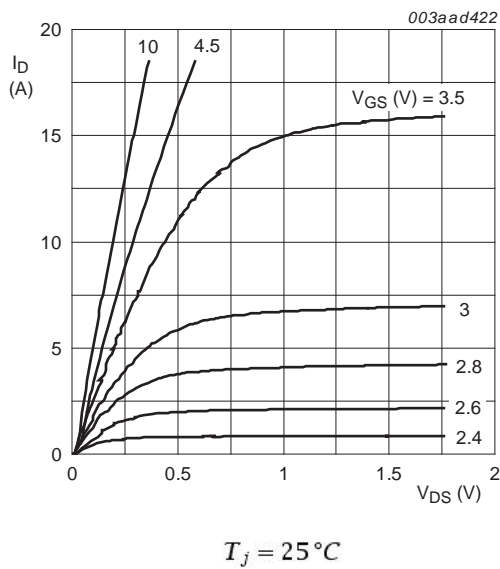


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

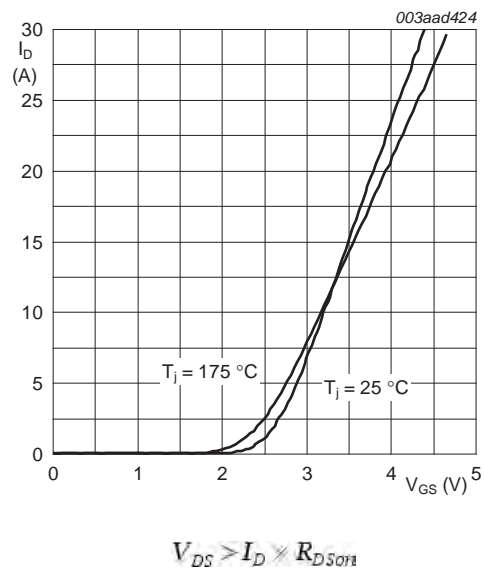
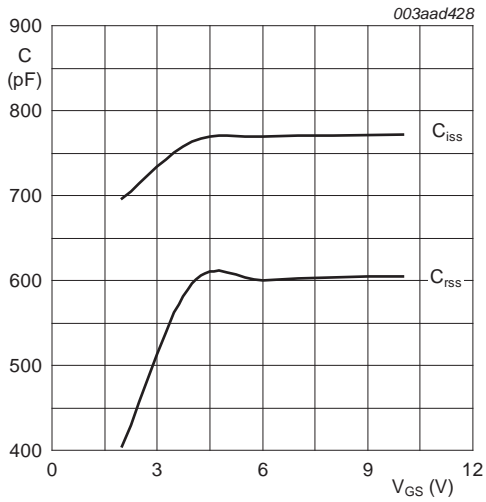
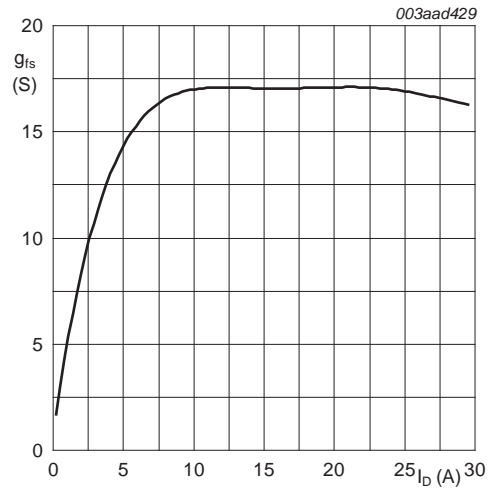


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



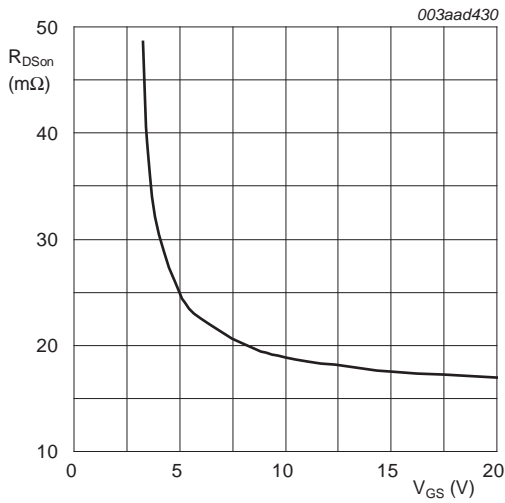
$V_{DS} = 0V; f = 1MHz$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



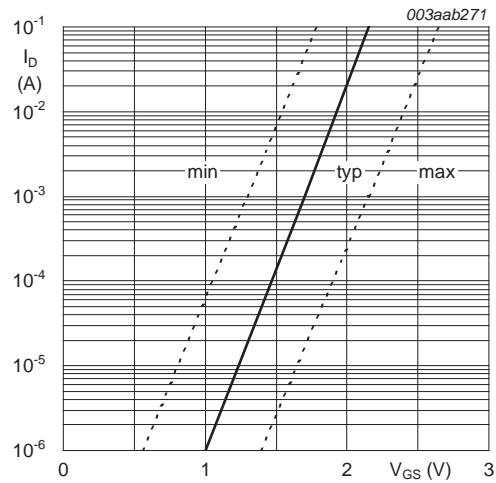
$T_j = 25^\circ C; V_{DS} = 10V$

Fig 8. Forward transconductance as a function of drain current; typical values



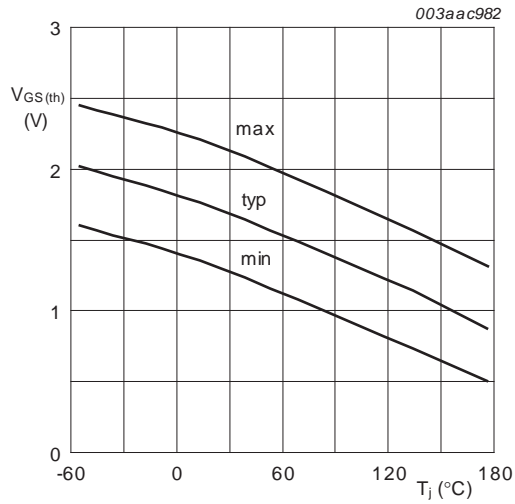
$T_j = 25^\circ C; I_D = 5A$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



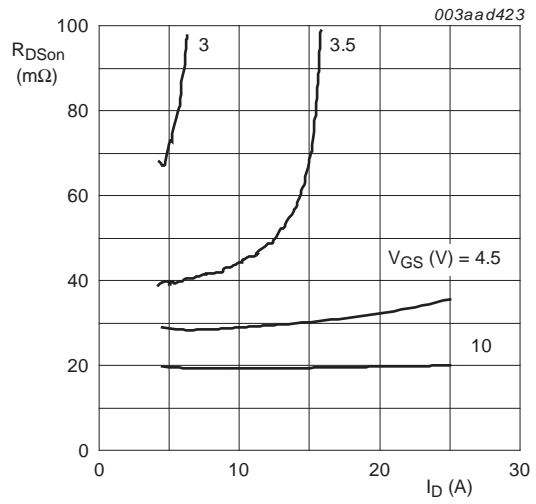
$T_j = 25^\circ C; V_{DS} = 5V$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



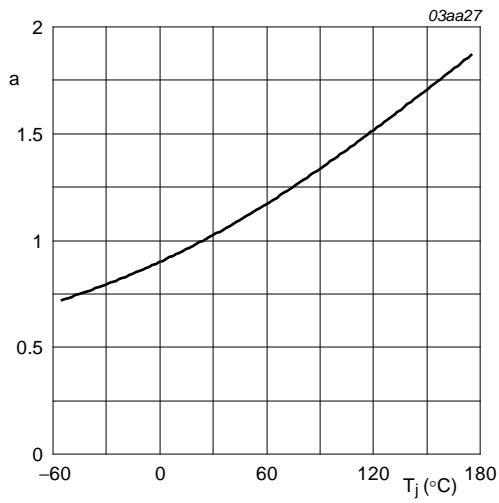
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

Fig 11. Gate-source threshold voltage as a function of junction temperature



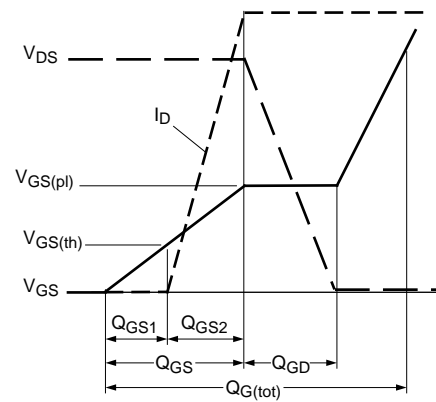
$$T_j = 25\text{ °C}$$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



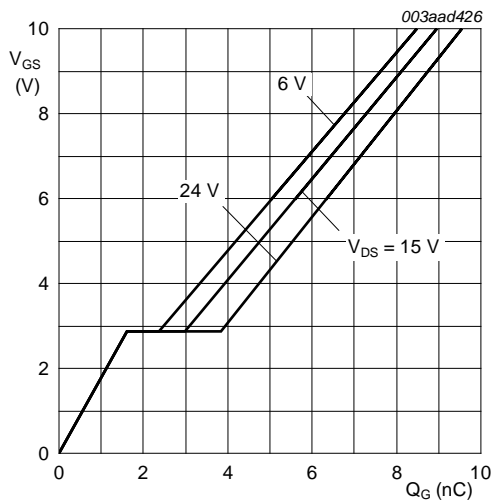
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



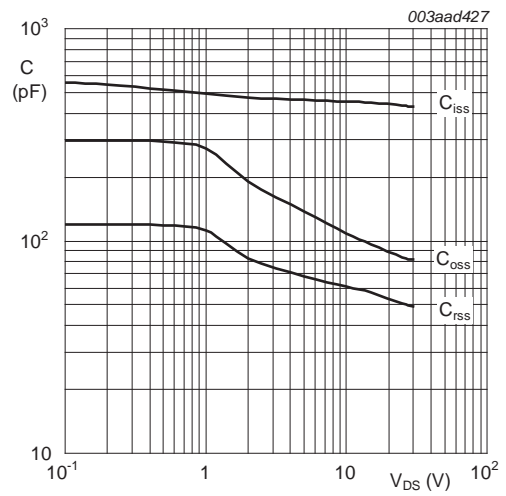
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Fig 14. Gate charge waveform definitions



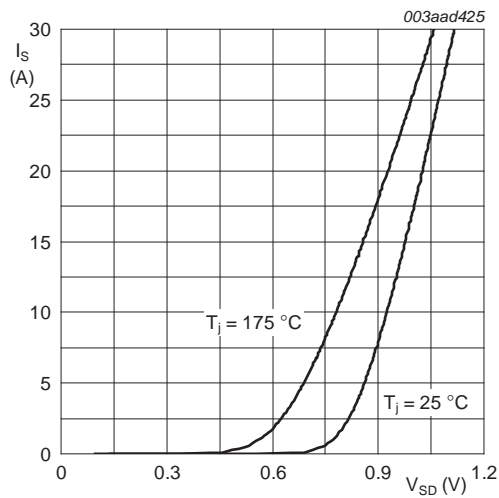
$T_j = 25\text{ }^\circ\text{C}; I_D = 5\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 17. Source current as a function of source-drain voltage;

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

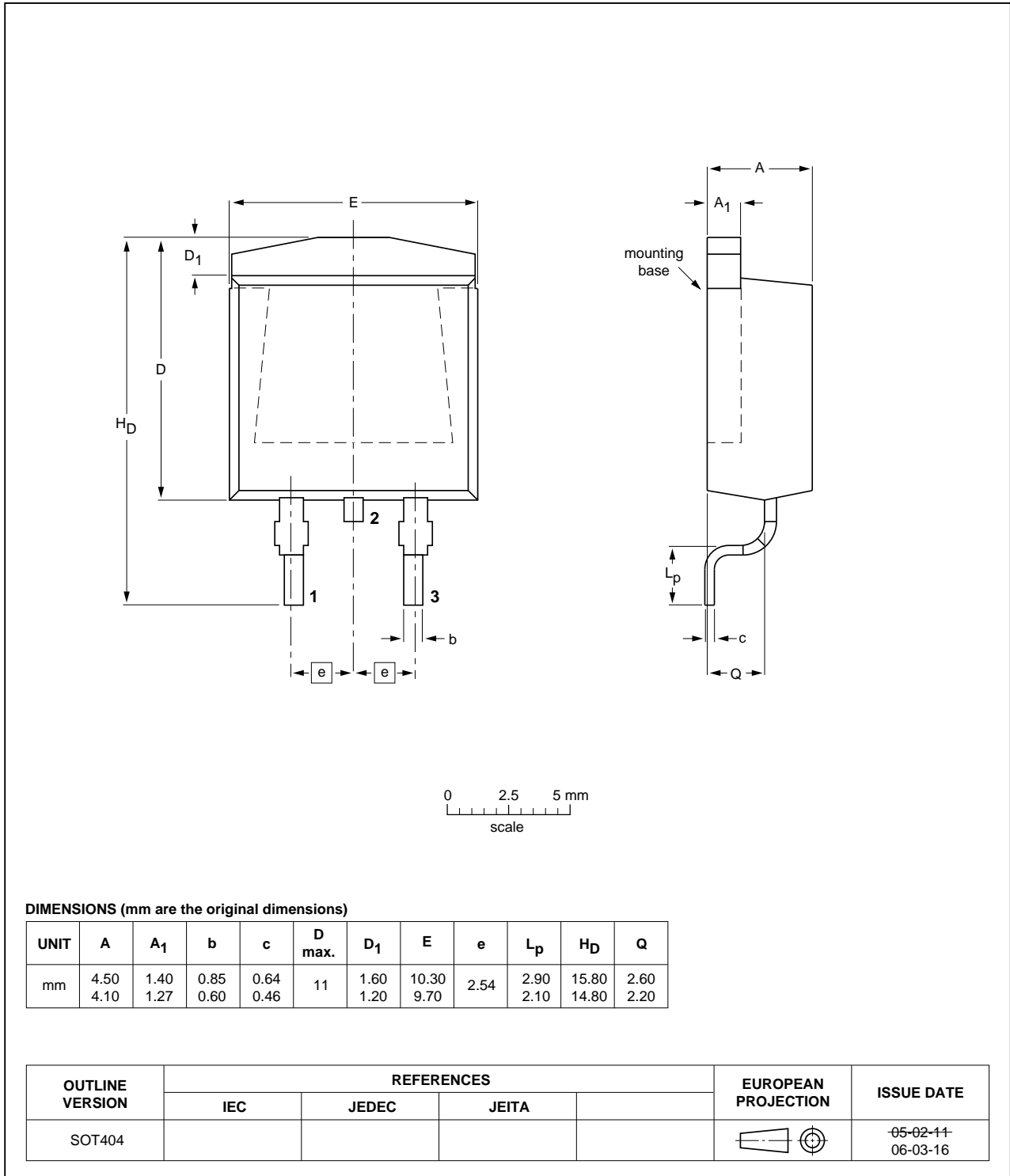


Fig 18. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN022-30BL v.1	20120321	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^[1] [2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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