



PSMN8R5-60YS

N-channel LFPACK 60 V, 8 mΩ standard level MOSFET

22 July 2015

Product data sheet

1. General description

Standard level N-channel MOSFET in LFPACK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- Advanced TrenchMOS provides low R_{DSon} and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPACK provides maximum power density in a Power SO8 package

3. Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

Table 1. Quick reference data

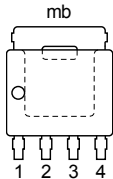
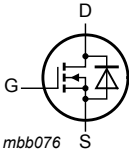
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	60	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 2	-	-	76	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	106	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 100\text{ °C}$; Fig. 12	-	-	12.8	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; Fig. 13	-	5.6	8	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 60\text{ A}$; $V_{DS} = 30\text{ V}$; Fig. 15 ; Fig. 14	-	7.7	-	nC



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	$V_{GS} = 10\text{ V}$; $I_D = 60\text{ A}$; $V_{DS} = 30\text{ V}$; Fig. 14 ; Fig. 15	-	39	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 76\text{ A}$; $V_{sup} \leq 60\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	-	97	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN8R5-60YS	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN8R5-60YS	8R560

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	60	V

Symbol	Parameter	Conditions	Min	Max	Unit
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	106	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	54	A
		V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	76	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	303	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	76	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	303	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 76 A; V _{sup} ≤ 60 V; R _{GS} = 50 Ω; unclamped	-	97	mJ

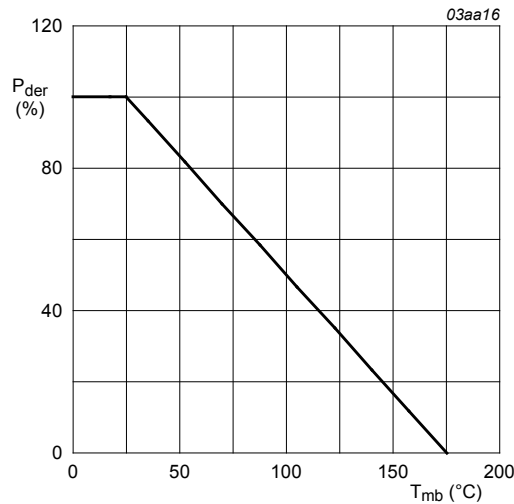


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

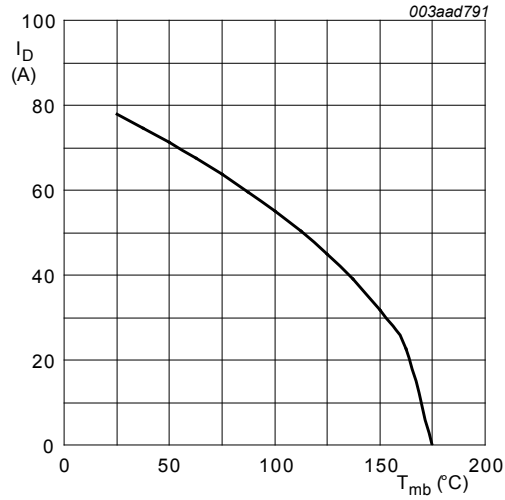


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10 \text{ V}$$

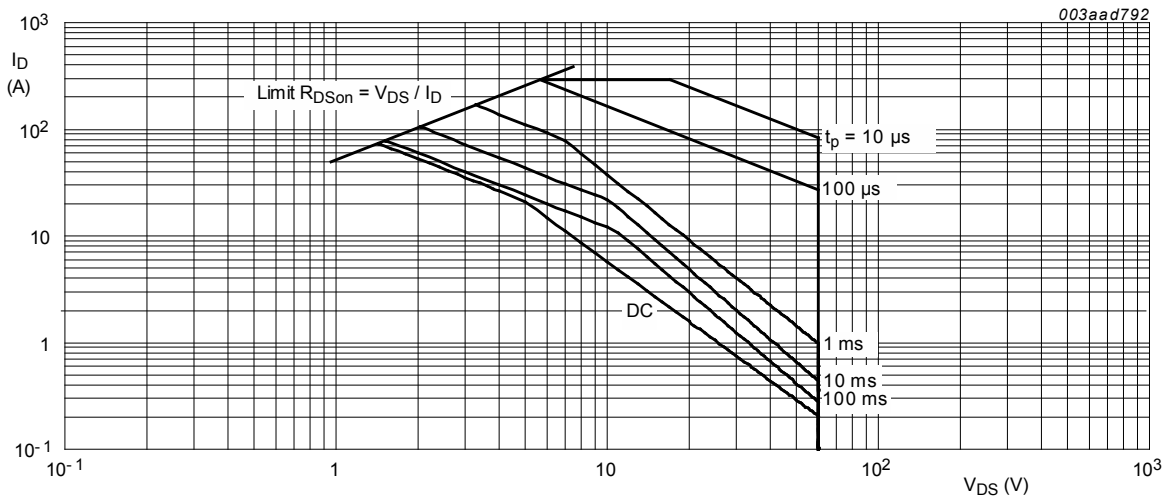


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25 \text{ }^\circ\text{C}; I_{DM} \text{ is a single pulse}$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.63	1.42	K/W

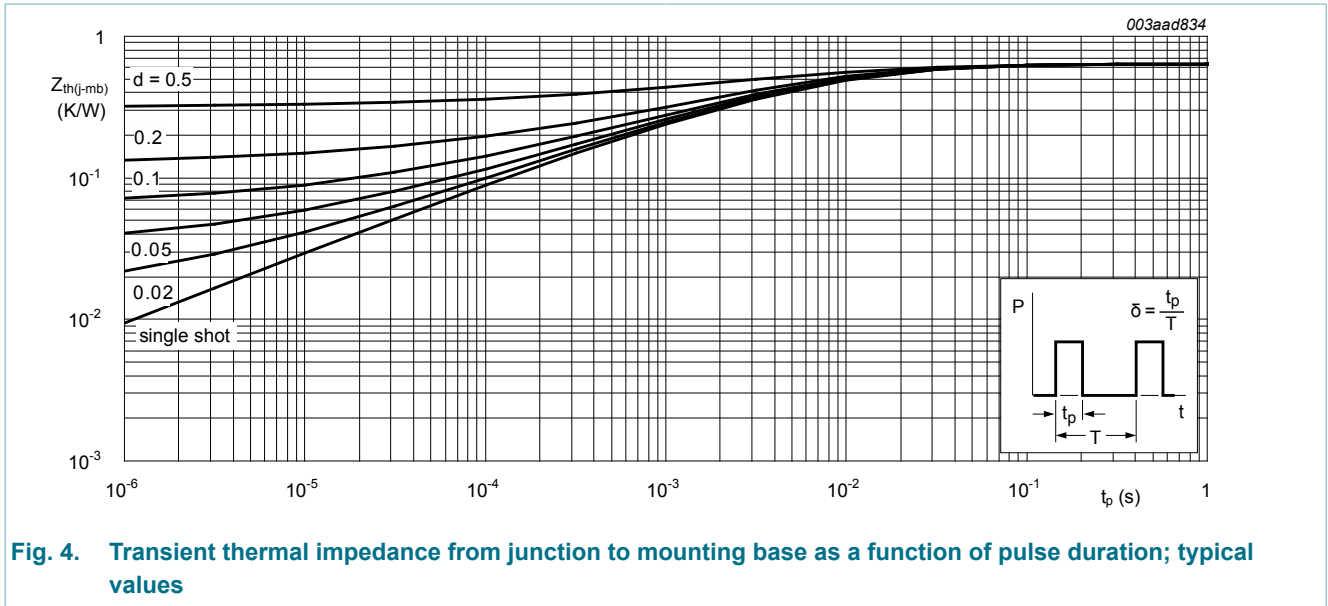


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 10 ; Fig. 11	2	3	3.8	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 11	-	-	4.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 11	0.95	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.03	2	μA
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	-	50	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 12	-	12	18.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ C;$ Fig. 12	-	-	12.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 13	-	5.6	8	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	0.61	-	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 60 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	-	39	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	33	-	nC
Q _{GS}	gate-source charge	I _D = 60 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 15 ; Fig. 14	-	13.3	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	I _D = 60 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 14	-	7	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	6.2	-	nC
Q _{GD}	gate-drain charge	I _D = 60 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 15 ; Fig. 14	-	7.7	-	nC
V _{GS(pl)}	gate-source plateau voltage	V _{DS} = 30 V; Fig. 14 ; Fig. 15	-	5.2	-	V
C _{iss}	input capacitance	V _{DS} = 30 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16	-	2370	-	pF
C _{oss}	output capacitance		-	307	-	pF
C _{rss}	reverse transfer capacitance		-	172	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 0.5 Ω; V _{GS} = 10 V; R _{G(ext)} = 4.7 Ω	-	18.4	-	ns
t _r	rise time		-	13.7	-	ns
t _{d(off)}	turn-off delay time		-	32.4	-	ns
t _f	fall time		-	9.2	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17	-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;	-	43.3	-	ns
Q _r	recovered charge	V _{DS} = 30 V	-	61.4	-	nC

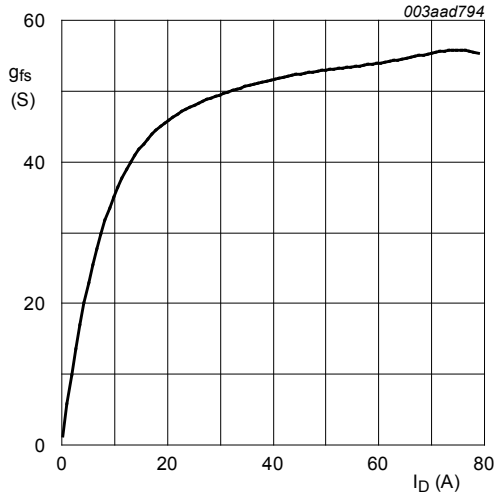


Fig. 5. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 20\text{ V}$

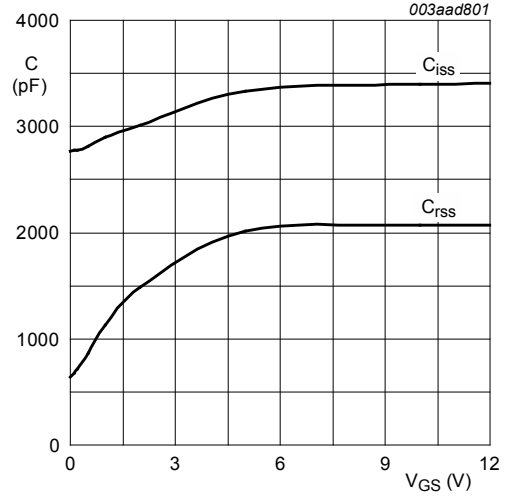


Fig. 6. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

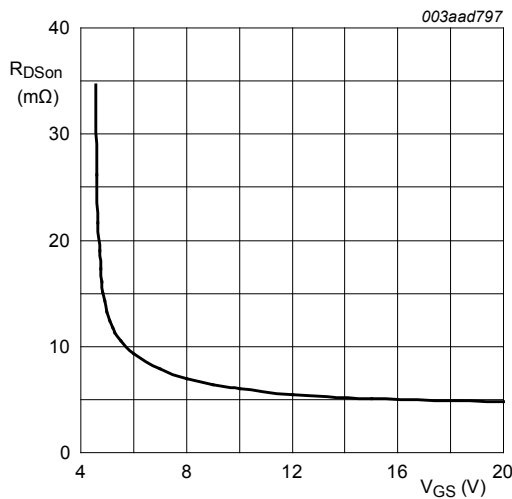


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$

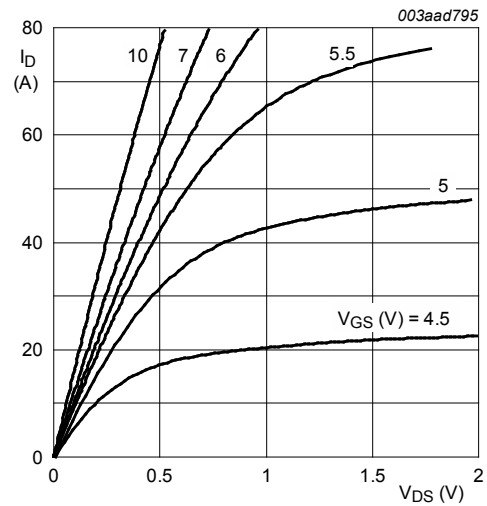


Fig. 8. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$

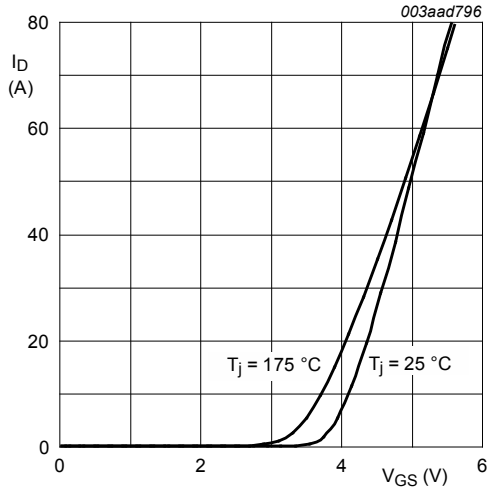
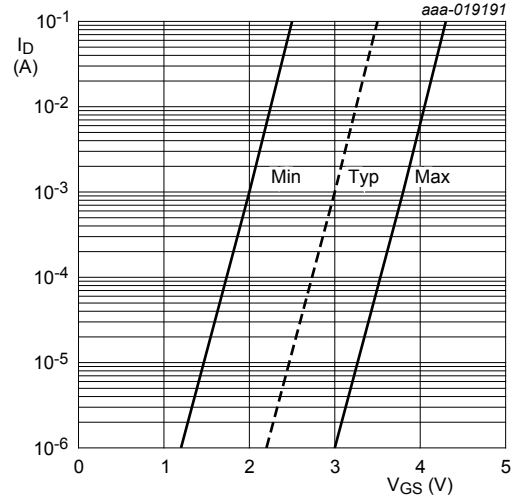


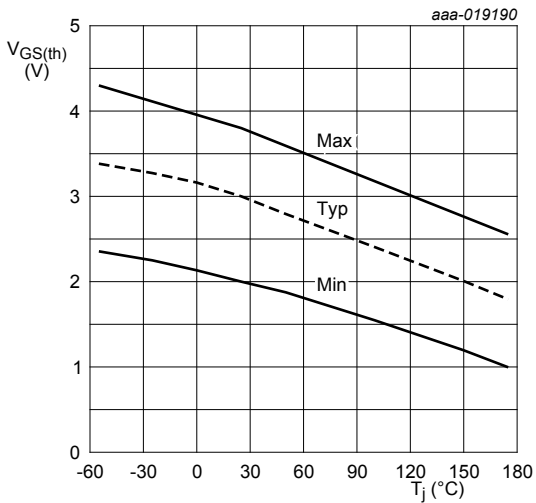
Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} > I_D \times R_{DSon}$$



$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig. 11. Gate-source threshold voltage as a function of junction temperature

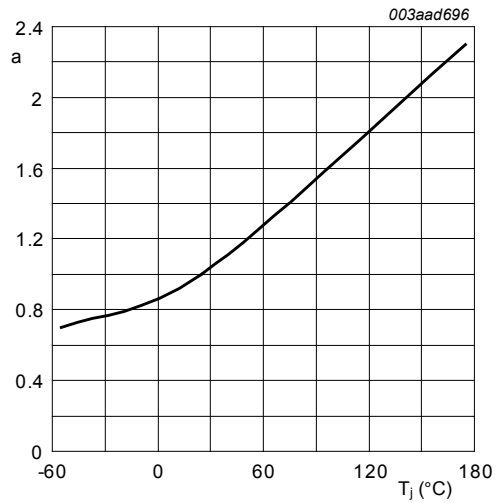


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature.

$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

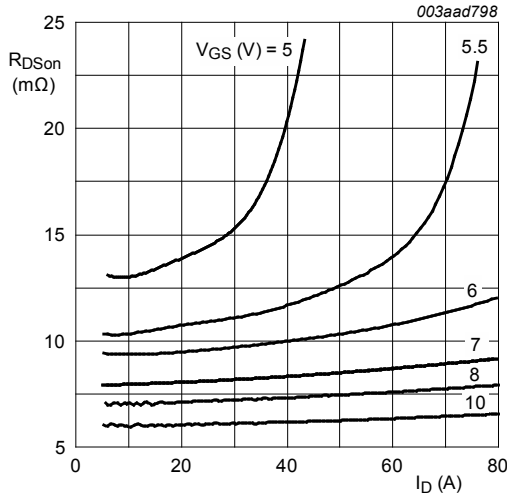


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25\text{ }^\circ\text{C}$

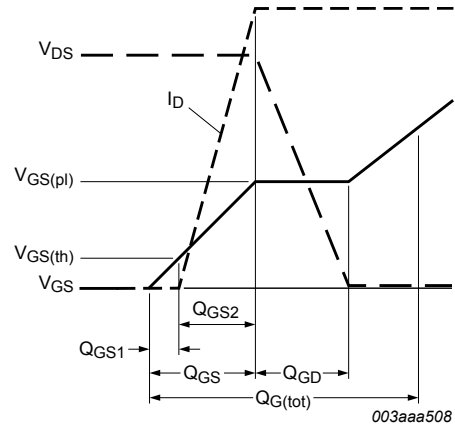


Fig. 14. Gate charge waveform definitions

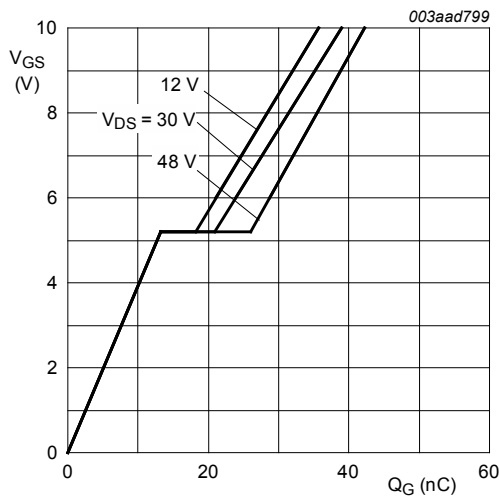


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 60\text{ A}$

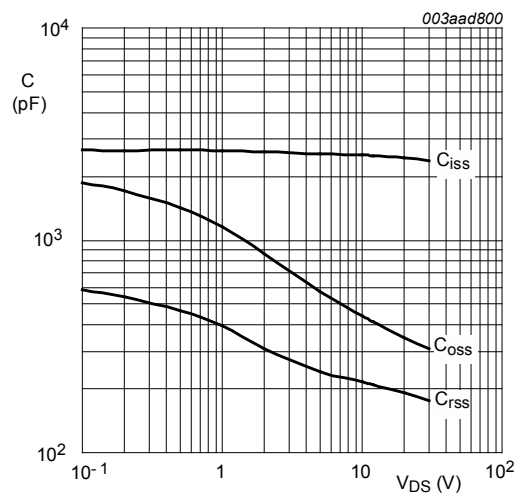


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

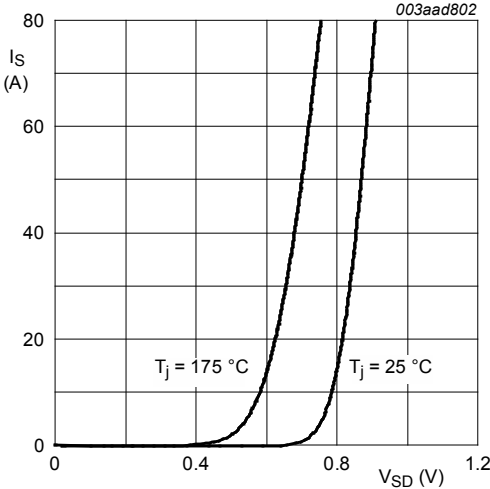


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

11. Package outline

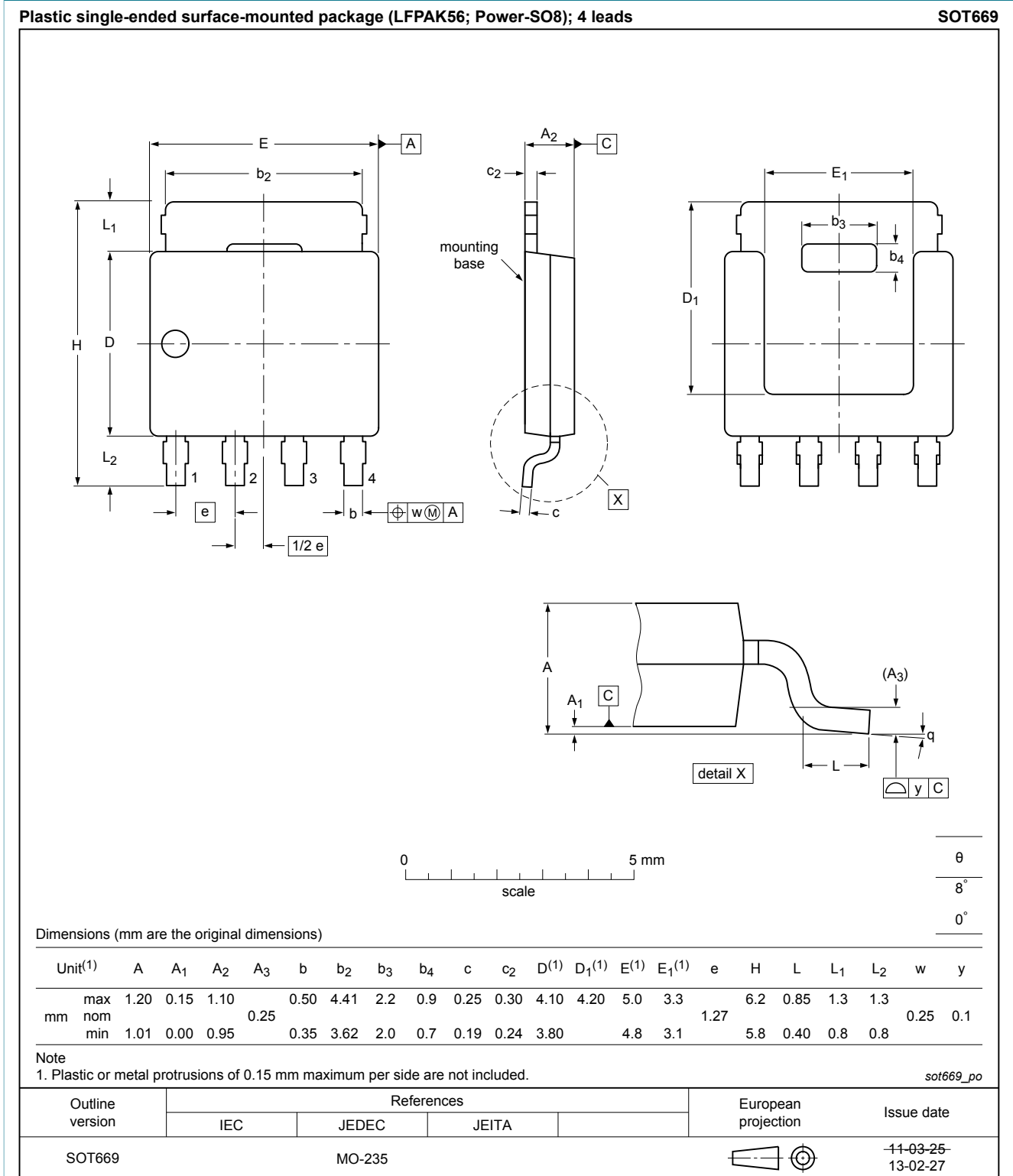


Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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