

# NTHD4P02F

## Power MOSFET and Schottky Diode

-20 V, -3.0 A, Single P-Channel with 3.0 A Schottky Barrier Diode, ChipFET™



ON Semiconductor®

<http://onsemi.com>

### Features

- Leadless SMD Package Featuring a MOSFET and Schottky Diode
- 40% Smaller than TSOP-6 Package with Similar Thermal Characteristics
- Independent Pinout to each Device to Ease Circuit Design
- Ultra Low VF Schottky
- Pb-Free Package is Available

### Applications

- Li-Ion Battery Charging
- High Side DC-DC Conversion Circuits
- High Side Drive for Small Brushless DC Motors
- Power Management in Portable, Battery Powered Products

### MOSFET MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Value	Units	
Drain-to-Source Voltage	V <sub>DSS</sub>	-20	V	
Gate-to-Source Voltage	V <sub>GS</sub>	±12	V	
Continuous Drain Current	Steady State	T <sub>J</sub> = 25°C	I <sub>D</sub> -2.2	A
		T <sub>J</sub> = 85°C	-1.6	
	t ≤ 5 s	T <sub>J</sub> = 25°C	I <sub>D</sub> -3.0	A
Pulsed Drain Current	t <sub>p</sub> = 10 μs	I <sub>DM</sub>	-9.0	A
Power Dissipation	Steady State	T <sub>J</sub> = 25°C	P <sub>D</sub> 1.1	W
		T <sub>J</sub> = 85°C	0.6	
	t ≤ 5 s	T <sub>J</sub> = 25°C	2.1	
Continuous Source Current (Body Diode)	I <sub>S</sub>	-2.1	A	
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C	

### SCHOTTKY DIODE MAXIMUM RATINGS

(T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Value	Units	
Peak Repetitive Reverse Voltage	V <sub>RRM</sub>	20	V	
DC Blocking Voltage	V <sub>R</sub>	20	V	
Average Rectified Forward Current	Steady State	T <sub>J</sub> = 25°C	I <sub>F</sub> 2.2	A
			t ≤ 5 s	3.0

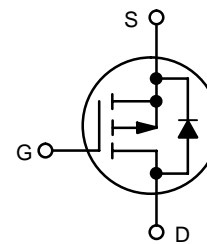
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

### MOSFET

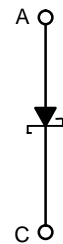
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
-20 V	-130 mΩ @ -4.5 V	-3.0 A
	200 mΩ @ -2.5 V	

### SCHOTTKY DIODE

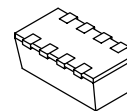
V <sub>R</sub> MAX	V <sub>F</sub> TYP	I <sub>F</sub> MAX
20 V	0.510 V	3.0 A



P-Channel MOSFET

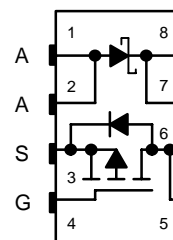


SCHOTTKY DIODE

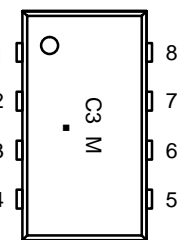


ChipFET CASE 1206A STYLE 3

### PIN CONNECTIONS



### MARKING DIAGRAM



C3 = Specific Device Code  
M = Month Code  
▪ = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NTHD4P02FT1	ChipFET	3000/Tape & Reel
NTHD4P02FT1G	ChipFET (Pb-free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## THERMAL RESISTANCE RATINGS

Parameter		Symbol	Max	Units
Junction-to-Ambient (Note 1)	Steady State	$T_J = 25^\circ\text{C}$	110	$^\circ\text{C/W}$
	$t \leq 5 \text{ s}$			

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

## MOSFET ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20	-23		V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$			-1.0	$\mu\text{A}$
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$			-5.0	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	-0.6	-0.75	-1.2	V
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -2.2 \text{ A}$		0.130	0.155	$\Omega$
		$V_{GS} = -2.5 \text{ V}, I_D = -1.7 \text{ A}$		0.200	0.240	
Forward Transconductance	$g_{FS}$	$V_{DS} = -10 \text{ V}, I_D = -1.7 \text{ A}$		5.0		S

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}, V_{DS} = -10 \text{ V}$		185	300	pF
Output Capacitance	$C_{OSS}$			95	150	
Reverse Transfer Capacitance	$C_{RSS}$			30	50	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -2.2 \text{ A}$		3.0	6.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.2		
Gate-to-Source Charge	$Q_{GS}$			0.5		
Gate-to-Drain Charge	$Q_{GD}$			0.9		

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5 \text{ V}, V_{DD} = -16 \text{ V}, I_D = -2.2 \text{ A}, R_G = 2.5 \Omega$		7.0	12	ns
Rise Time	$t_r$			13	25	
Turn-Off Delay Time	$t_{d(OFF)}$			33	50	
Fall Time	$t_f$			27	40	

### DRAIN-SOURCE DIODE CHARACTERISTICS (Note 2)

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 \text{ V}, I_S = -2.1 \text{ A}$		-0.85	-1.15	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0 \text{ V}, I_S = -2.1 \text{ A}, di_S/dt = 100 \text{ A}/\mu\text{s}$		32		ns
Charge Time	$t_a$			10		
Discharge Time	$t_b$			22		
Reverse Recovery Charge	$Q_{RR}$			15		

### SCHOTTKY DIODE ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Maximum Instantaneous Forward Voltage	$V_F$	$I_F = 0.1 \text{ A}$		0.425		V
		$I_F = 0.5 \text{ A}$		0.480		
		$I_F = 1.0 \text{ A}$		0.510	0.575	
Maximum Instantaneous Reverse Current	$I_R$	$V_R = 10 \text{ V}$			1.0	$\mu\text{A}$
		$V_R = 20 \text{ V}$			5.0	
Maximum Voltage Rate of Change	$dv/dt$	$V_R = 20 \text{ V}$		10,000		V/ns
Non-Repetitive Peak Surge Current	$I_{FSM}$	Halfwave, Single Pulse, 60 Hz			23	A

2. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

3. Switching characteristics are independent of operating junction temperatures.

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## TYPICAL MOSFET PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

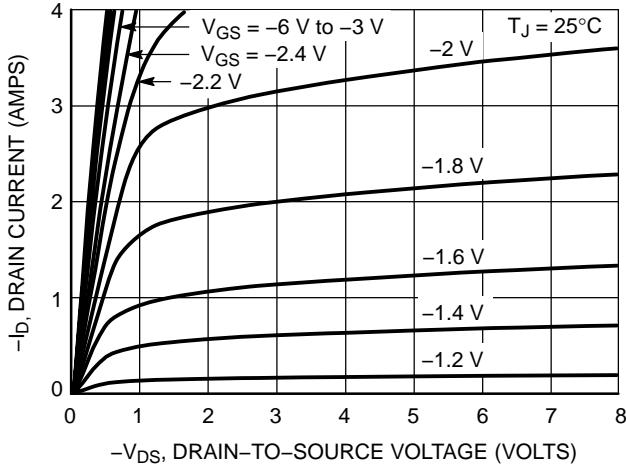


Figure 1. On-Region Characteristics

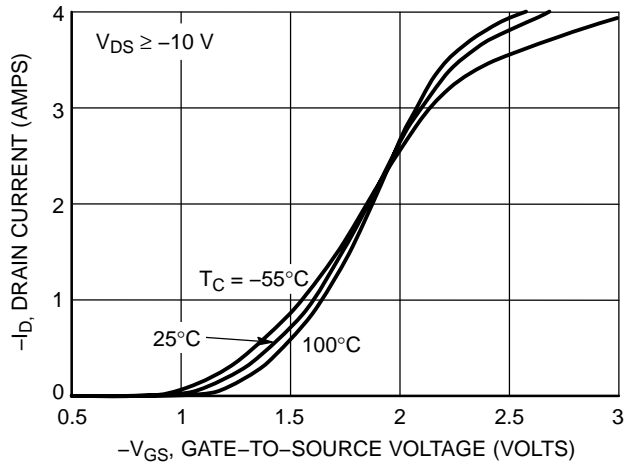


Figure 2. Transfer Characteristics

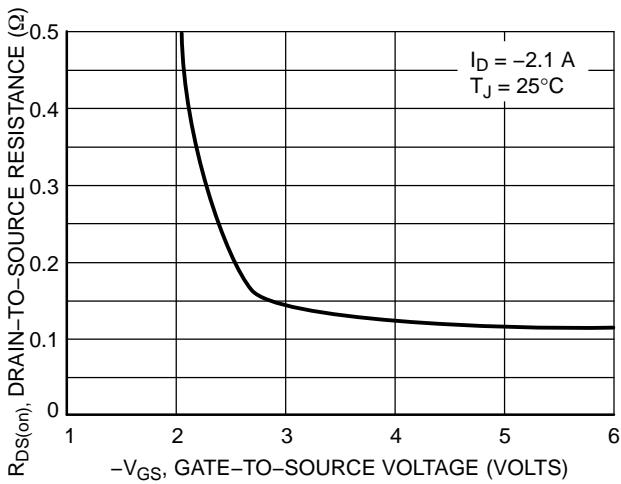


Figure 3. On-Resistance vs. Gate-to-Source Voltage

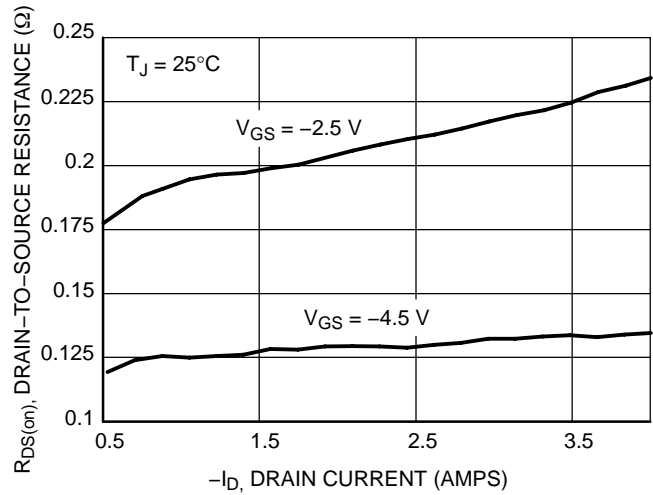


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

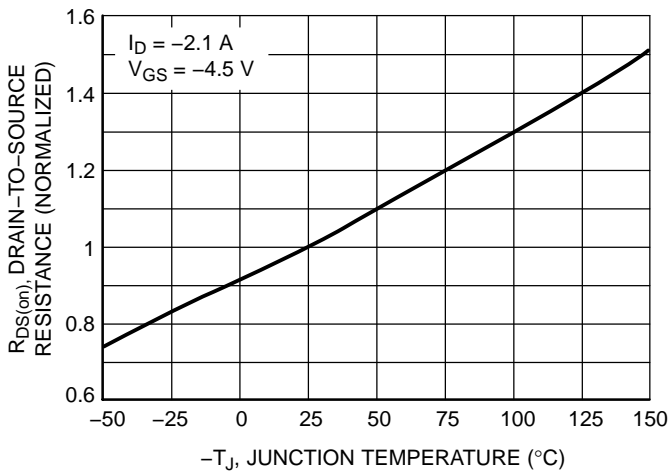


Figure 5. On-Resistance Variation with Temperature

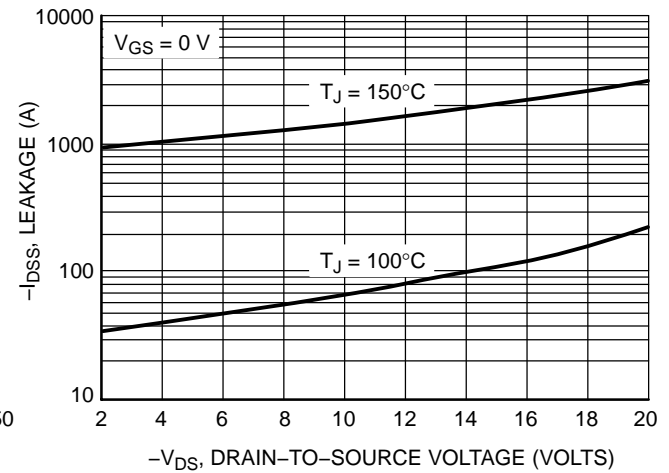


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL MOSFET PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

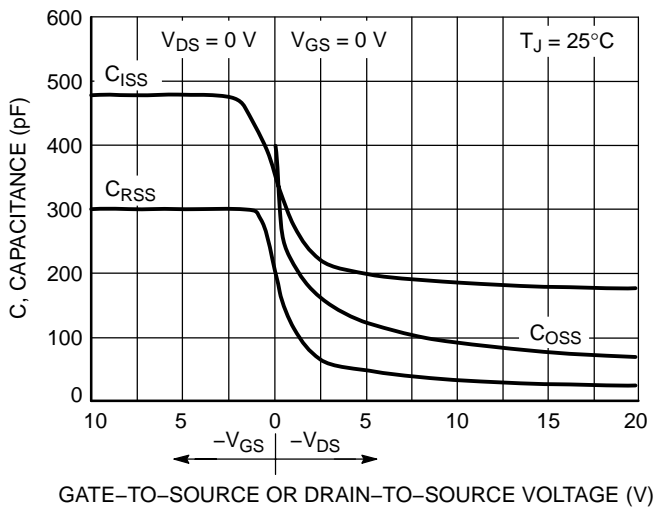


Figure 7. Capacitance Variation

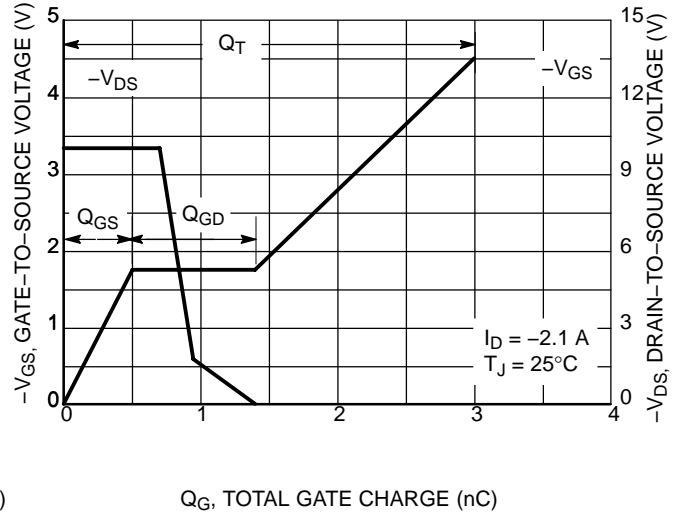


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

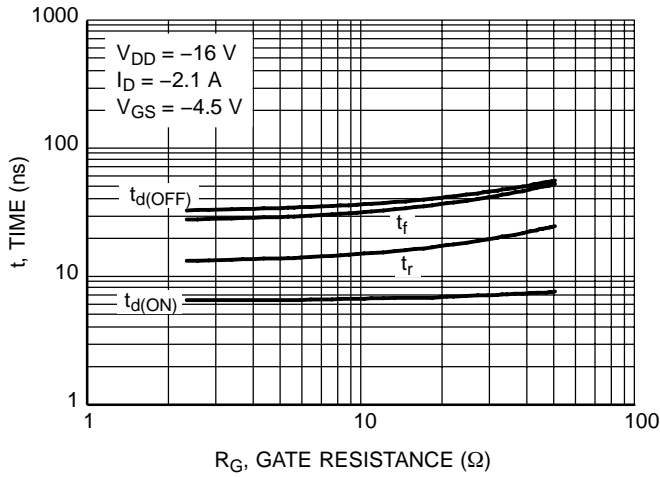


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

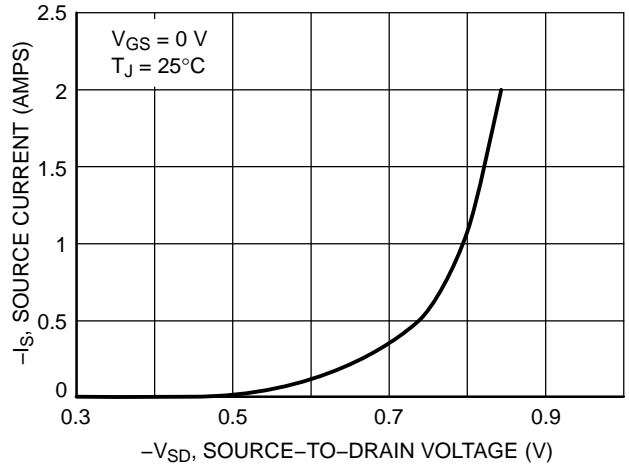


Figure 10. Diode Forward Voltage vs. Current

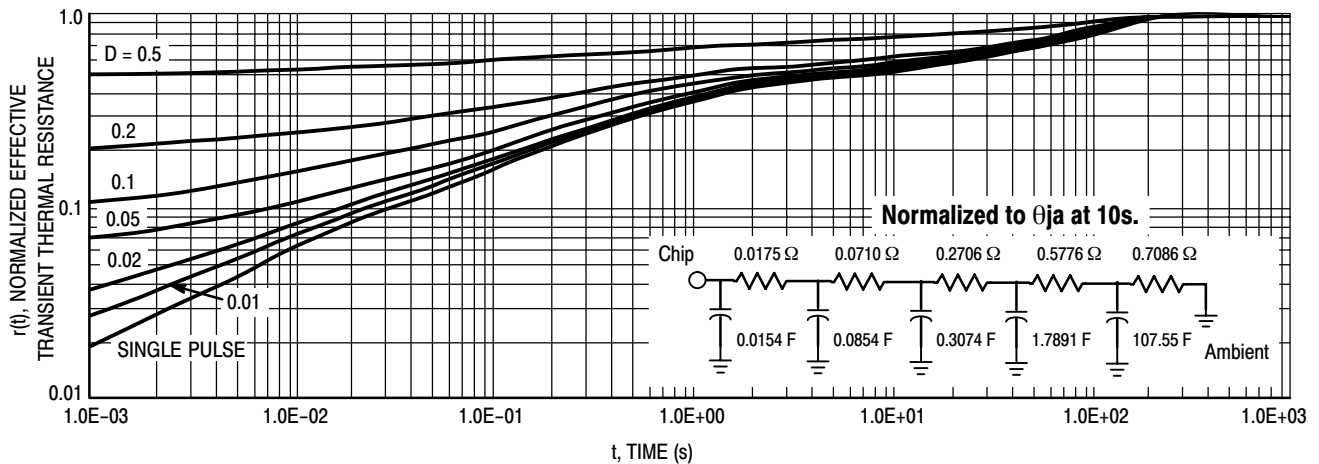


Figure 11. Thermal Response

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## TYPICAL SCHOTTKY PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

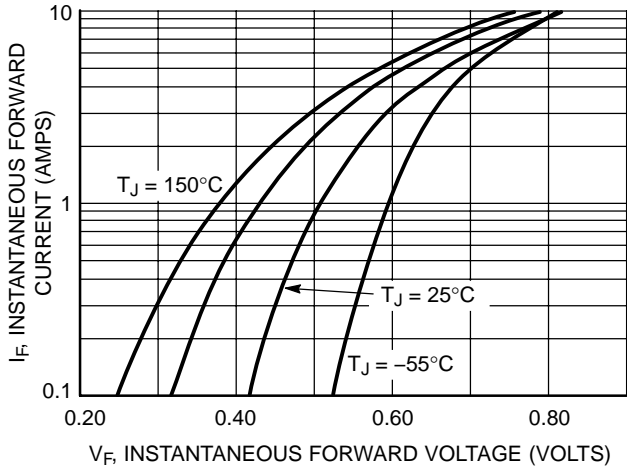


Figure 12. Typical Forward Voltage

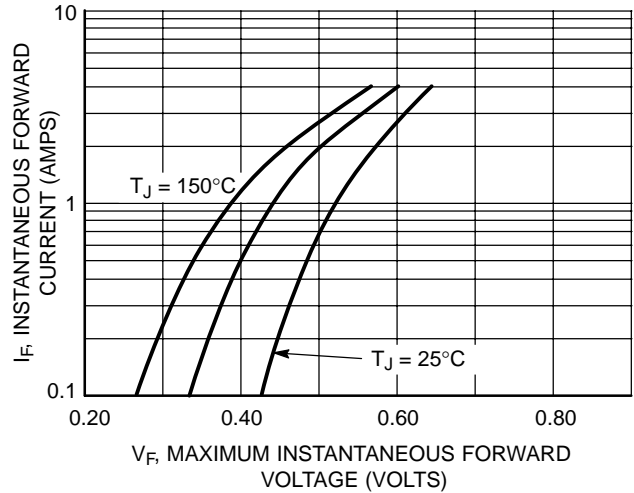


Figure 13. Maximum Forward Voltage

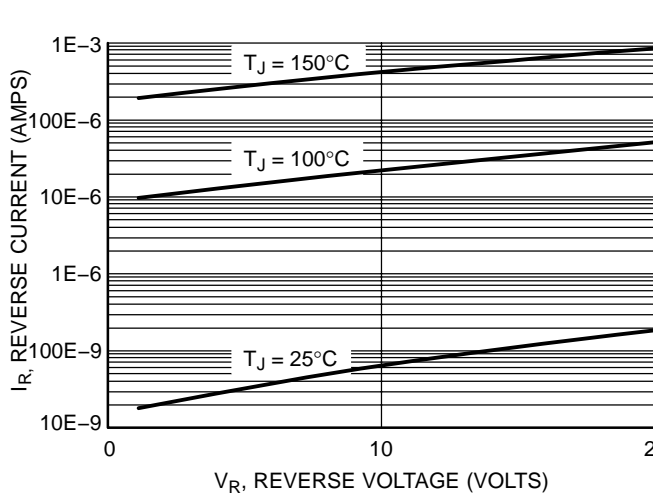


Figure 14. Typical Reverse Current

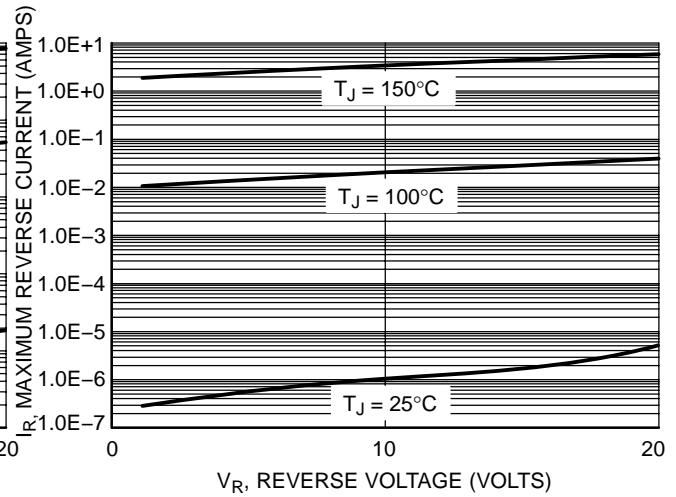


Figure 15. Maximum Reverse Current

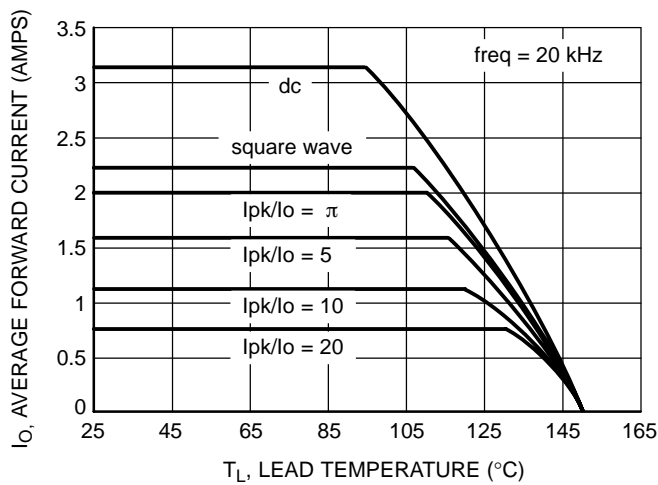


Figure 16. Current Derating

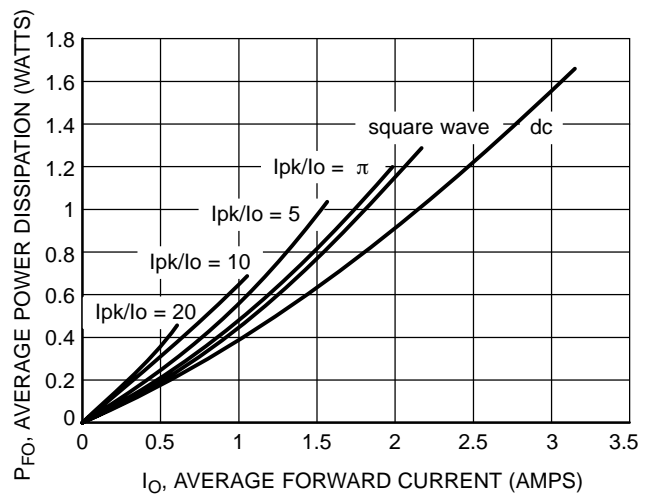


Figure 17. Forward Power Dissipation

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## SOLDERING FOOTPRINT\*

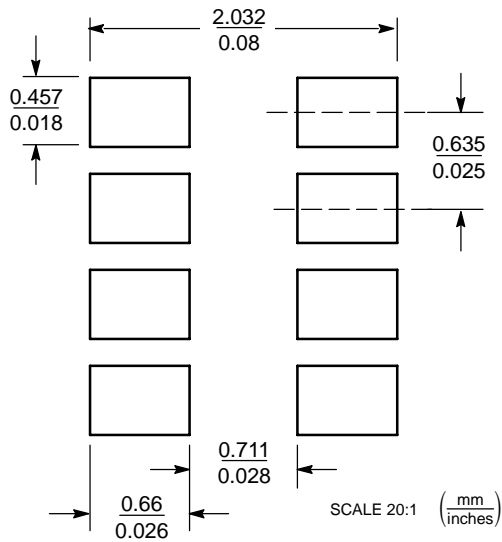


Figure 18. Basic

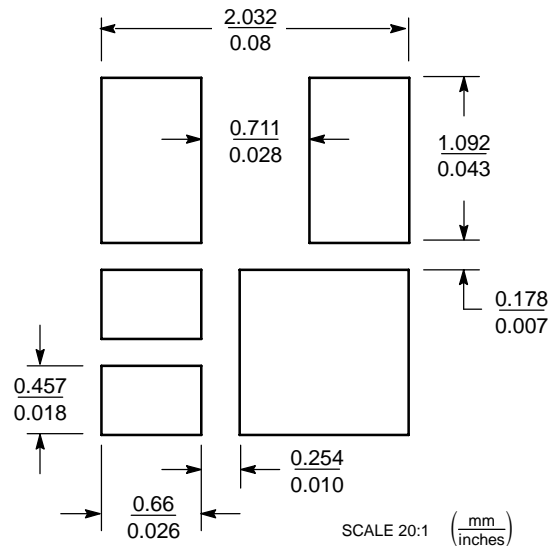


Figure 19. Style 3

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 18. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

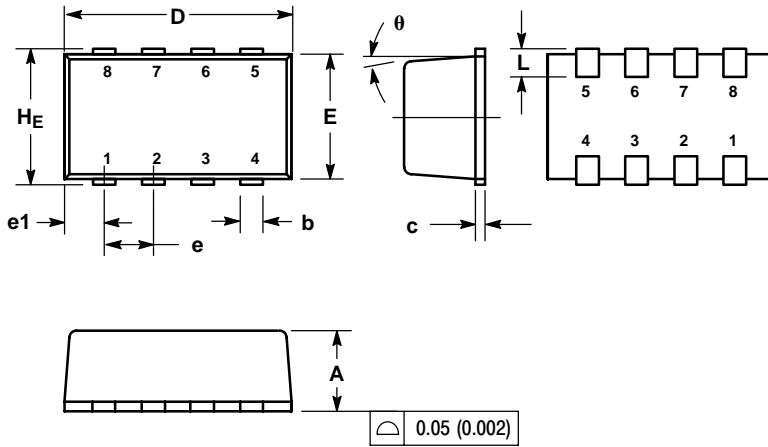
The minimum recommended pad pattern shown in Figure 19 improves the thermal area of the drain connections (pins 5, 6) while remaining within the confines

of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper lead-frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

# NTHD4P02F

## PACKAGE DIMENSIONS

ChipFET™  
CASE 1206A-03  
ISSUE G



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

### STYLE 3:

- PIN 1: A  
2: A  
3: S  
4: G  
5: D  
6: D  
7: C  
8: C

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