



FC8V22040L

Gate Resistor installed Dual N-Channel MOS Type

For lithium-ion secondary battery protection circuit

■ Features

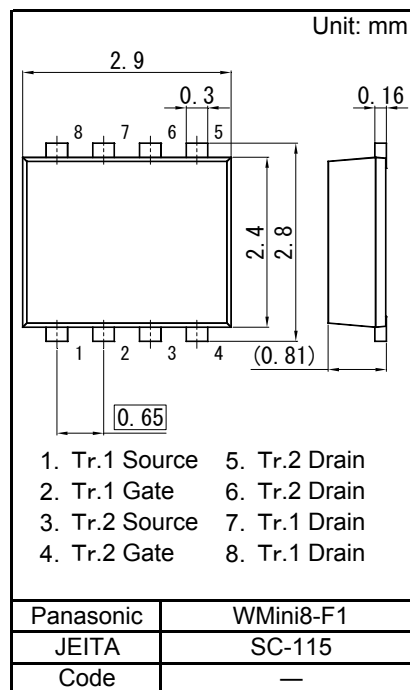
- Low drain-source On-state Resistance:
 $R_{DS(on)typ.} = 10.5 \text{ m}\Omega$ ($V_{GS} = 4.5 \text{ V}$)
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol: 4C

■ Basic Part Number : Dual Nch MOS 24V (Drain Common type)

■ Packaging

Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)



1. Tr.1 Source
2. Tr.1 Gate
3. Tr.2 Source
4. Tr.2 Gate
5. Tr.2 Drain
6. Tr.2 Drain
7. Tr.1 Drain
8. Tr.1 Drain

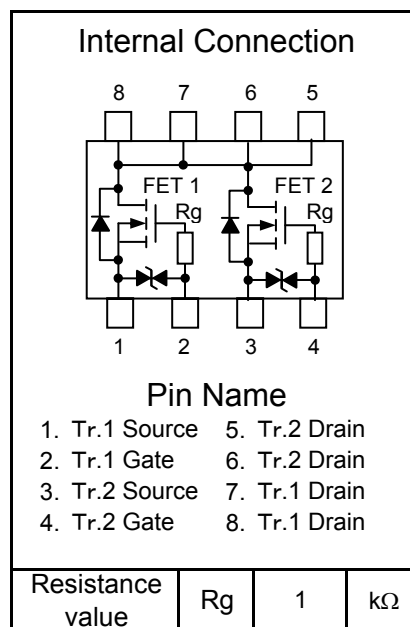
■ Absolute Maximum Ratings $T_a = 25 \text{ }^\circ\text{C}$ Tr.1,Tr.2

Parameter		Symbol	Rating	Unit
FET1	Drain-source Voltage	VDS	24	V
	Gate-source Voltage	VGS	± 12	V
FET2	Drain Current	ID	8	A
	Drain Current (Pulsed)	IDp	48	A
Overall	Power Dissipation	PD1 ^{*1}	1.0	W
		PD2 ^{*1,2}	1.2	
		PD3 ^{*3}	0.4	
	Channel Temperature	Tch	150	$^\circ\text{C}$
Operating Ambient Temperature	Topr	-40 to + 85	$^\circ\text{C}$	
Storage Temperature Range	Tstg	-55 to +150	$^\circ\text{C}$	

Note) *1 Glass epoxy board: 25.4 mm × 25.4 mm × 0.8 mm Copper foil of the drain portion should have a area of 300 mm² or more
PD absolute maximum rating without a heat sink: 400 mW

*2 t = 10 s

*3 Stand-alone (without the board)



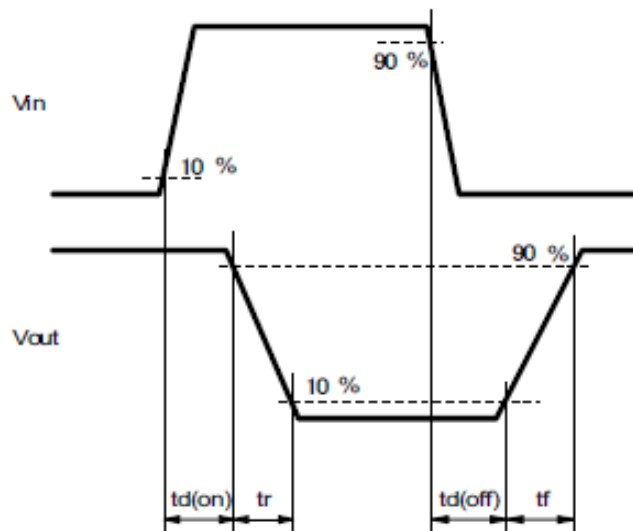
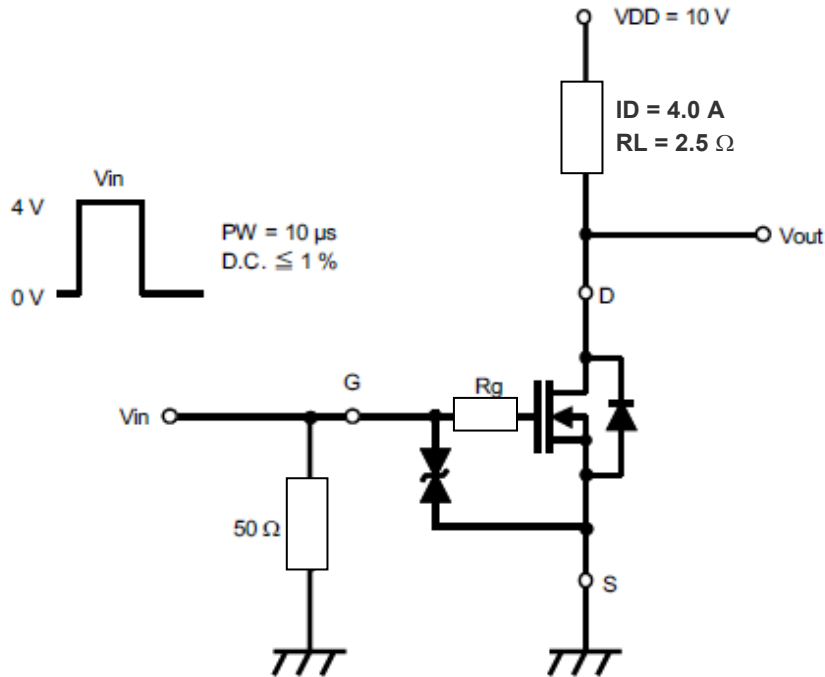


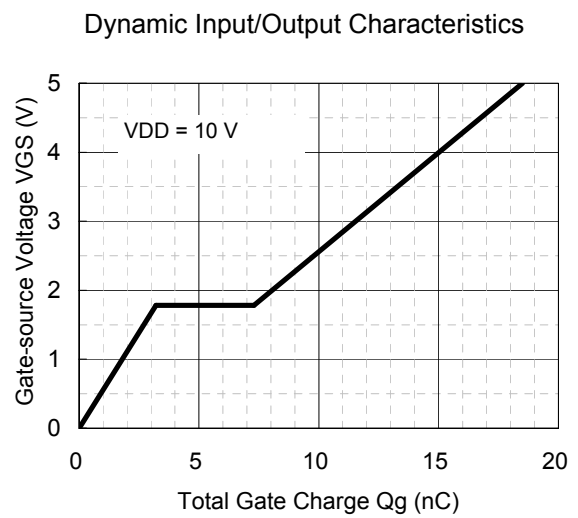
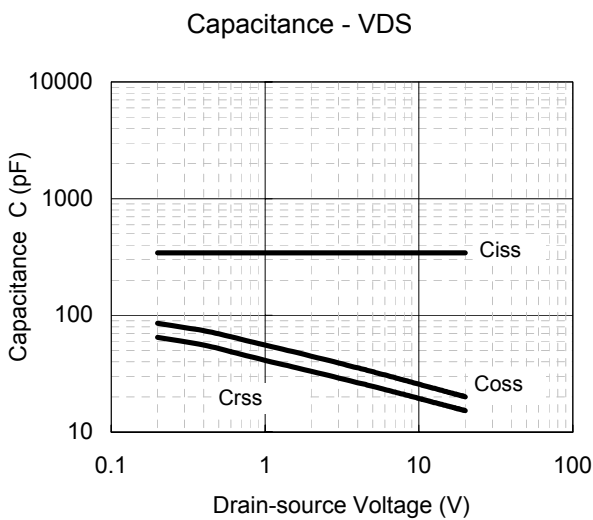
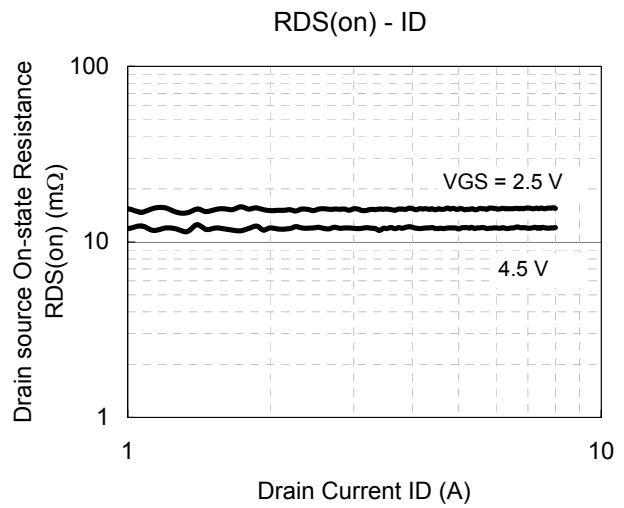
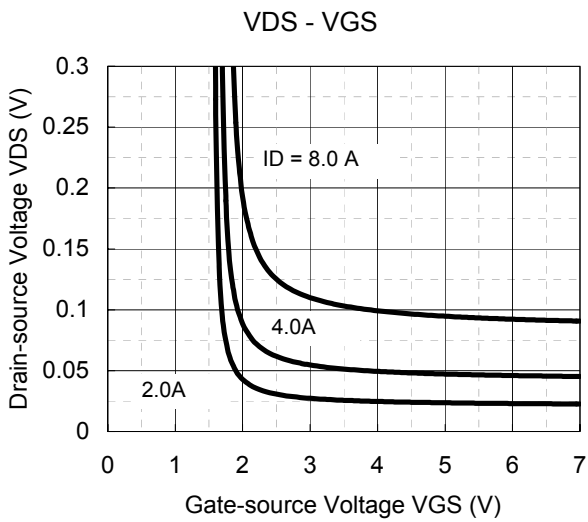
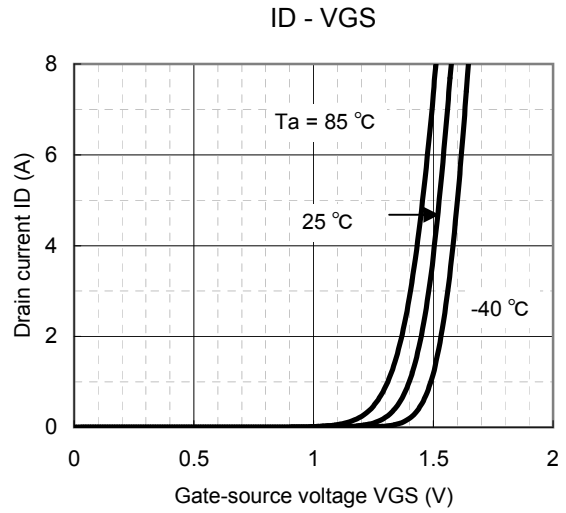
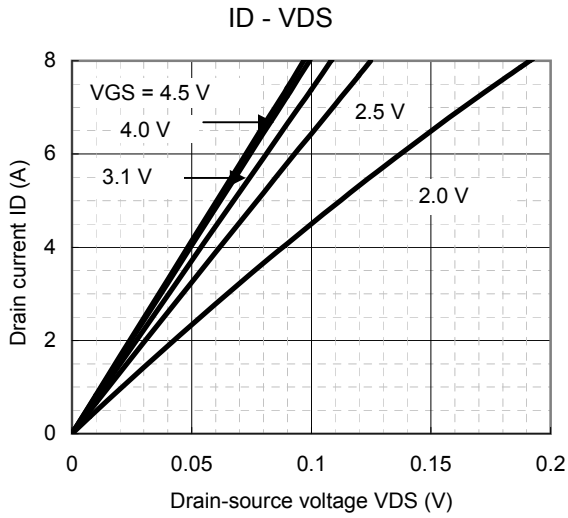
■ Electrical Characteristics Ta = 25°C ± 3°C Tr.1,Tr.2

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	VDSS	ID = 1.0 mA, VGS = 0	24			V
Drain-source cutoff current	IDSS	VDS = 24 V, VGS = 0			1.0	μA
Gate-source cutoff current	IGSS	VGS = ±8.0 V, VDS = 0			±10	μA
Gate threshold voltage	Vth	ID = 1.0 mA, VDS = 10 V	0.40	0.85	1.50	V
Drain-source ON resistance	RDS(ON)1	ID = 4.0 A, VGS = 4.5 V	7.0	10.5	15	mΩ
	RDS(ON)2	ID = 4.0 A, VGS = 4.0 V	7.2	11.0	16	mΩ
	RDS(ON)3	ID = 4.0 A, VGS = 3.1 V	7.5	12.0	18	mΩ
	RDS(ON)4	ID = 4.0 A, VGS = 2.5 V	8.0	13.5	20	mΩ
Turn-on delay time *1	td(on)	VDD = 10 V, VGS = 0 V to 4 V		0.6		μs
Rise time *1	tr	ID = 4.0 A		1.5		μs
Turn-off delay time *1	td(off)	VDD = 10 V, VGS = 4 V to 0 V		4.4		μs
Fall time *1	tf	ID = 4.0 A		2.8		μs
Source to Drain Diode Forward Voltage	VSD	IS = 4.0 A, VGS = 0 V		0.8	1.2	V

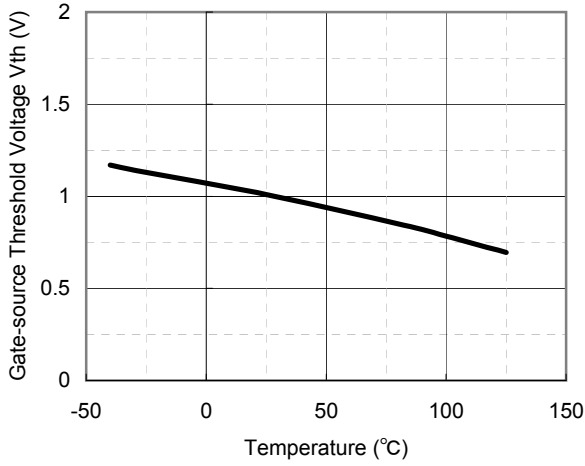
- Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
2. *1 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

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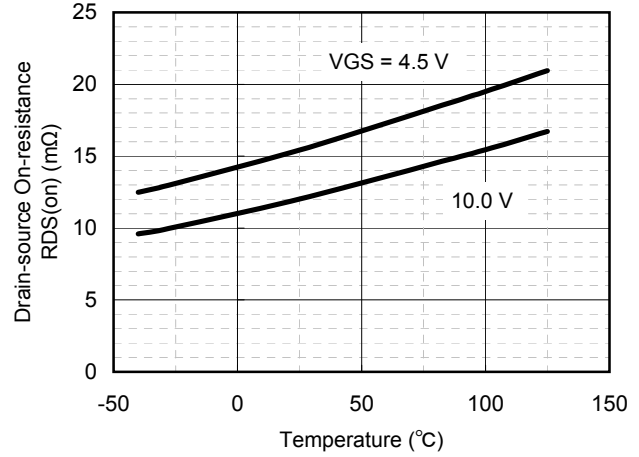




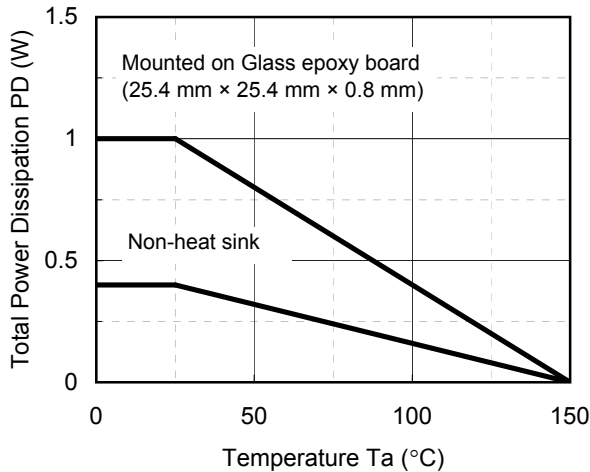
Vth - Ta



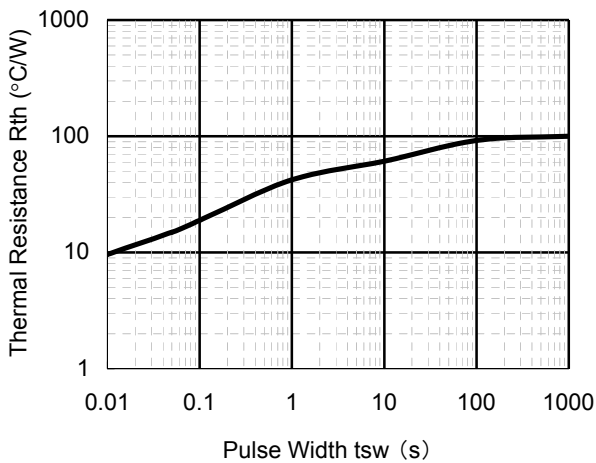
RDS(on) - Ta



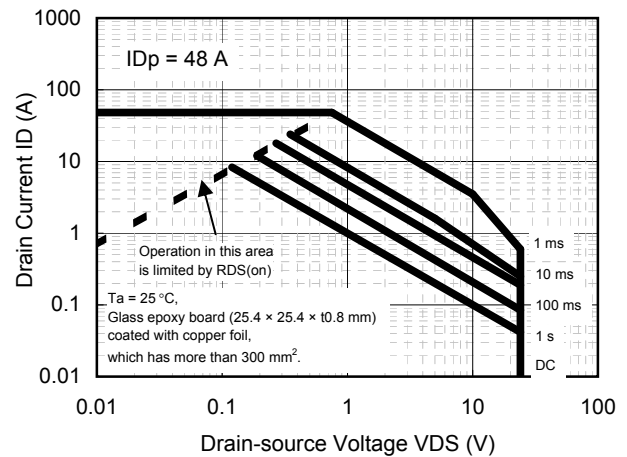
PD - Ta



Rth - tsw

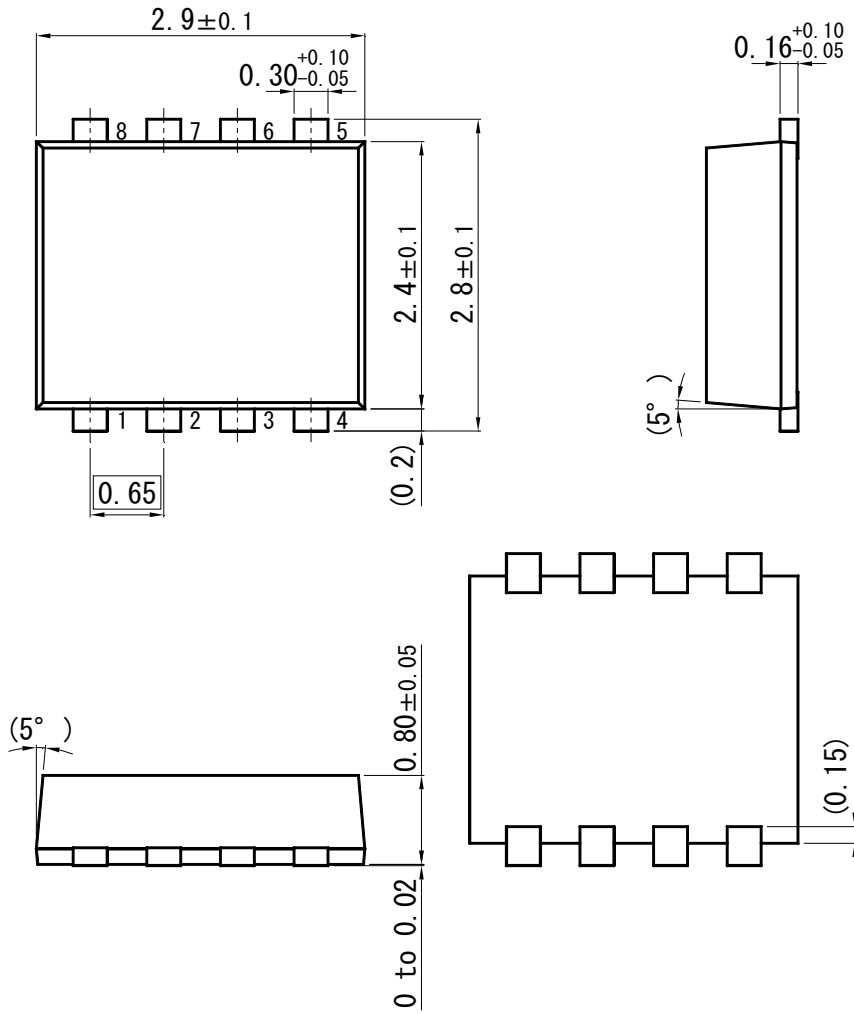


Safe Operating Area

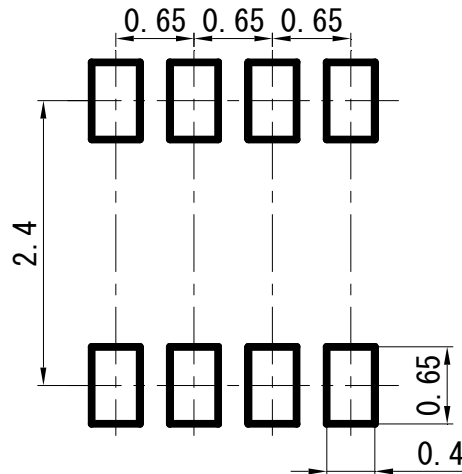


WMini8-F1

Unit : mm



■ Land Pattern (Reference) (Unit : mm)



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