STB4N62K3, STD4N62K3

N-channel 620 V, 1.7 Ω typ., 3.8 A SuperMESH3™ Power MOSFETs in D²PAK and DPAK packages

Datasheet - production data

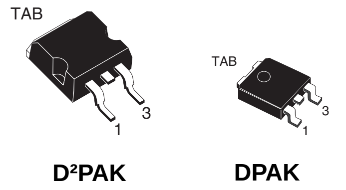
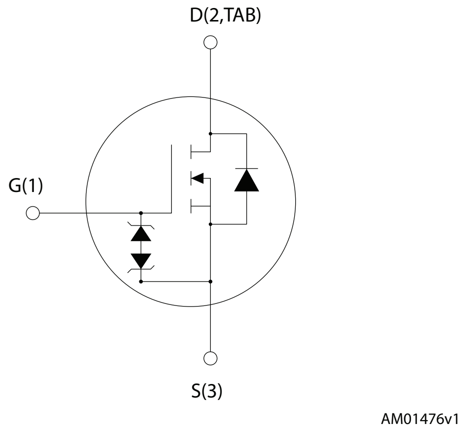


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_W
STB4N62K3	620 V	2 Ω	3.8 A	70 W
STD4N62K3				

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STB4N62K3	4N62K3	D²PAK	Tape and reel
STD4N62K3		DPAK	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	620	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	3.8	A
I_D	Drain current (continuous) at T_C = 100 °C	2	A
I_{DM} (1)	Drain current (pulsed)	15.2	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	3.8	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	115	mJ
$V_{ESD(G-S)}$	Gate source ESD(HBM-C = 100 pF, R = 1.5 kΩ)	2500	V
dv/dt (2)	Peak diode recovery voltage slope	12	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)		V
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 3.8 A, di/dt = 400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$, VDS peak ≤ V(BR)DSS.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D²PAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max		1.79	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb max	30	50	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	620			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 620V			1	µA
		V_{GS} = 0 V_{DS} = 620V, T_C=125 °C			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.9 A		1.7	2	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		550		pF
C_{oss}	Output capacitance			42		pF
C_{rss}	Reverse transfer capacitance			7		pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 496 V, V_{GS} = 0		27		pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	2	5	10	Ω
Q_g	Total gate charge	V_{DD} = 496 V, I_D = 3.8 A, V_{GS} = 10 V (see *Figure 18*)		22		nC
Q_{gs}	Gate-source charge			4		nC
Q_{gd}	Gate-drain charge			13		nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 1.9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17*)	-	10	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off-delay time		-	29	-	ns
t_f	Fall time		-	19	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.8	A
I_{SDM} (1)	Source-drain current (pulsed)		-		15.2	A
V_{SD} (2)	Forward on voltage	I_{SD} = 3.8 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 3.8 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 22*)	-	220		ns
Q_{rr}	Reverse recovery charge		-	1.4		µC
I_{RRM}	Reverse recovery current		-	13		A
t_{rr}	Reverse recovery time	I_{SD} = 3.8 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 22*)	-	270		ns
Q_{rr}	Reverse recovery charge		-	1.9		µC
I_{RRM}	Reverse recovery current		-	14		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK

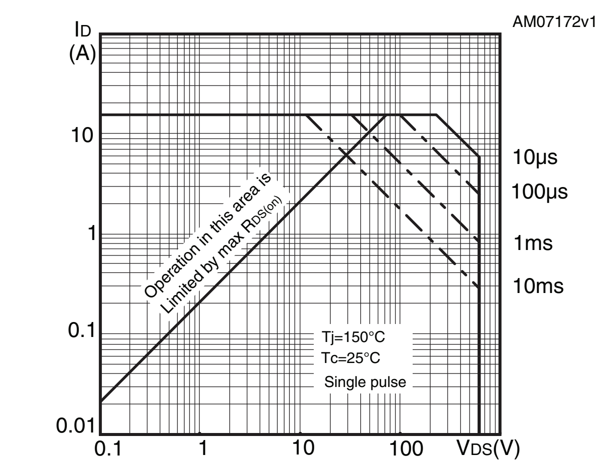


Figure 3. Thermal impedance for D²PAK

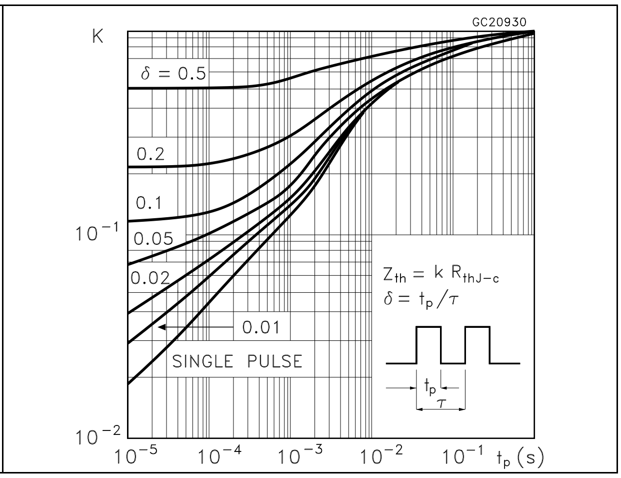


Figure 4. Safe operating area for DPAK

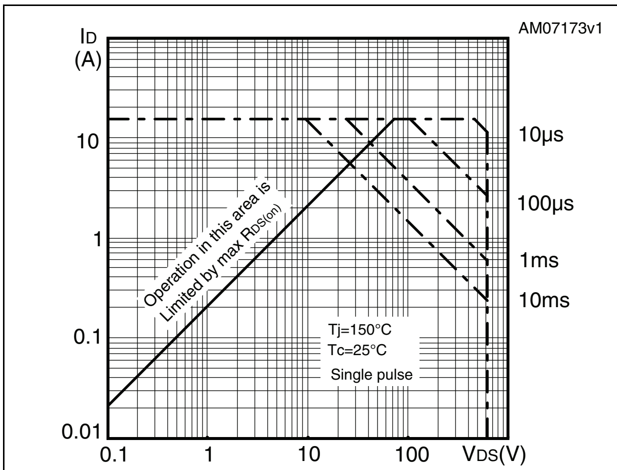


Figure 5. Thermal impedance for DPAK

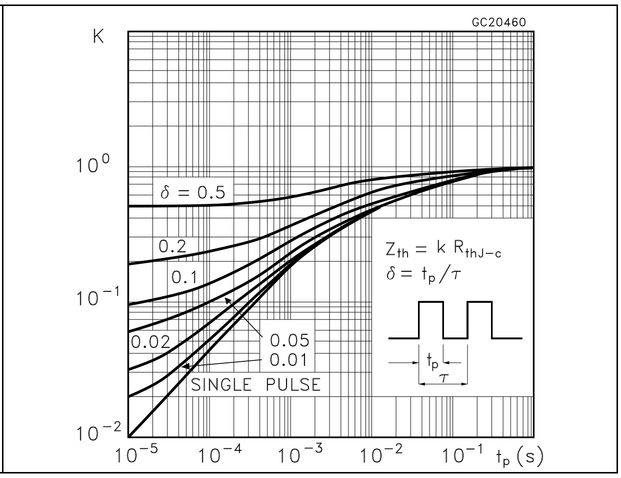


Figure 6. Output characteristics

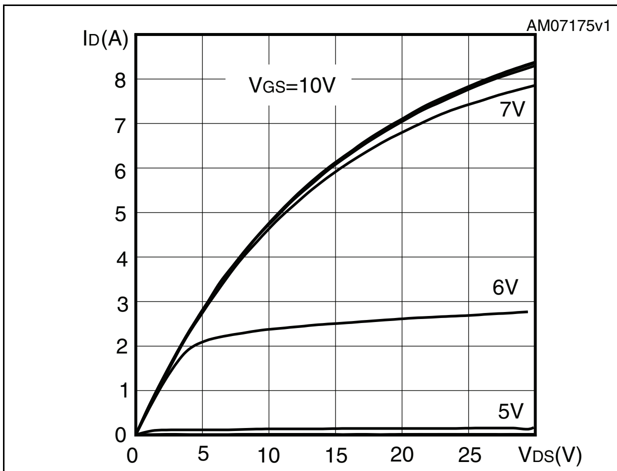


Figure 7. Transfer characteristics

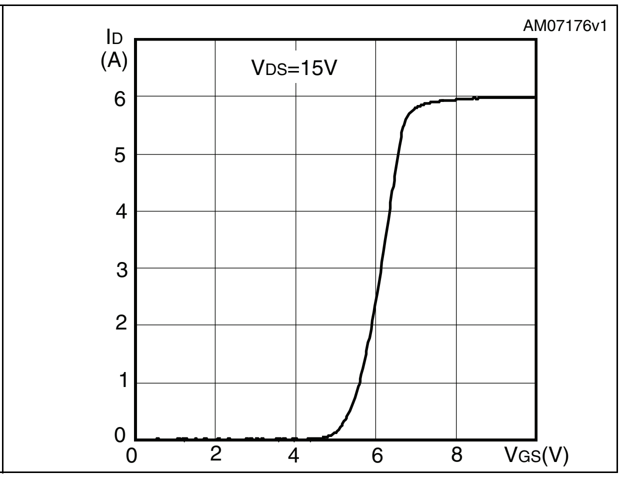


Figure 8. Gate charge vs gate-source voltage

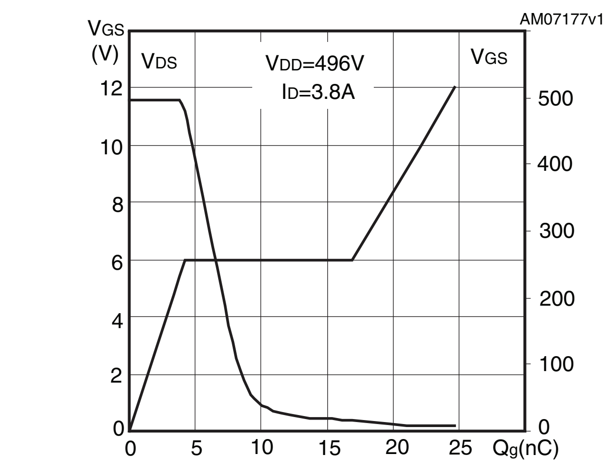


Figure 9. Static drain-source on resistance

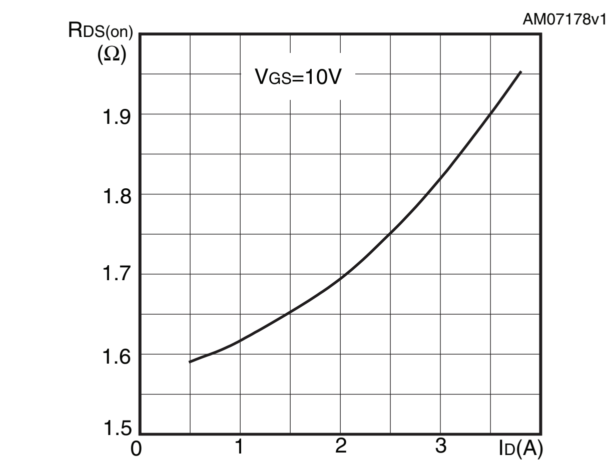


Figure 10. Capacitance variations

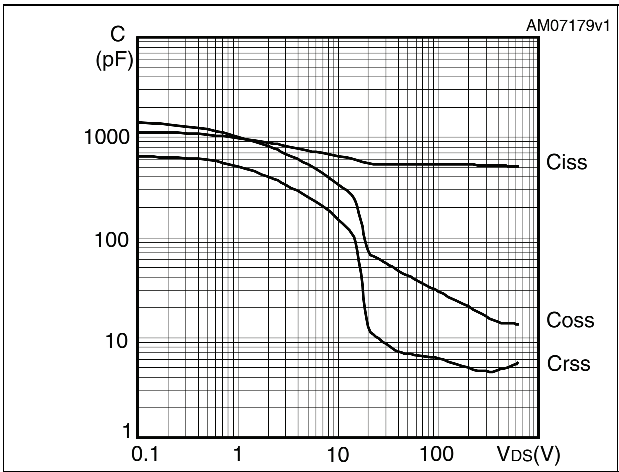


Figure 11. Output capacitance stored energy

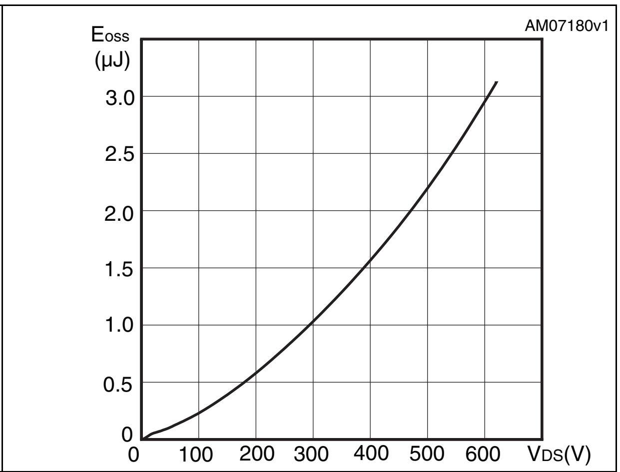


Figure 12. Normalized gate threshold voltage vs temperature

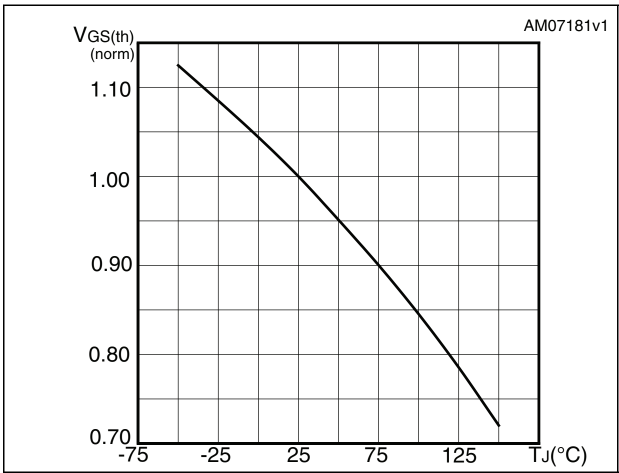


Figure 13. Normalized on-resistance vs temperature

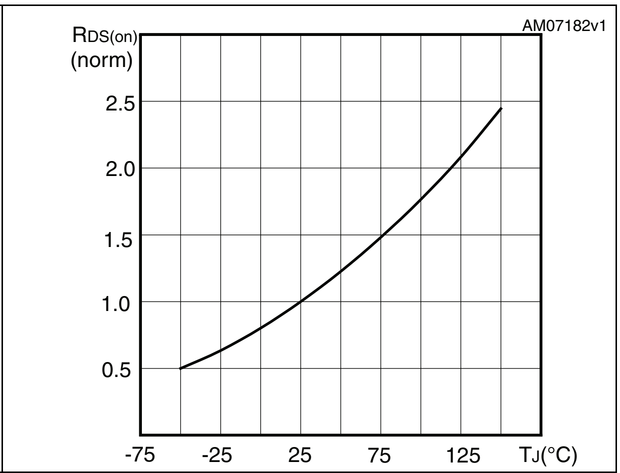


Figure 14. Maximum avalanche energy vs starting Tj

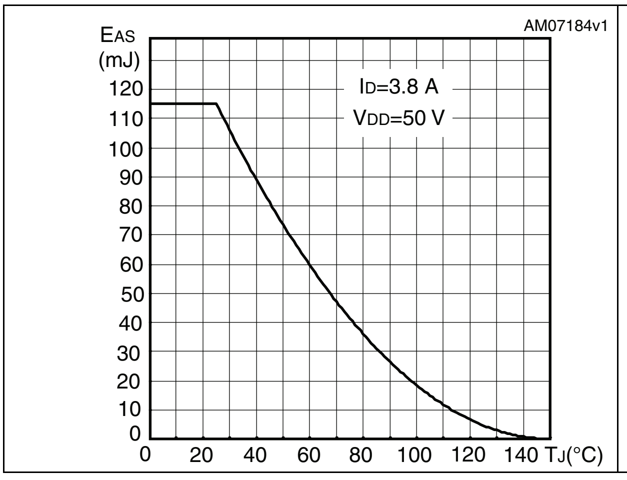


Figure 15. Normalized B_{VDSS} vs temperature

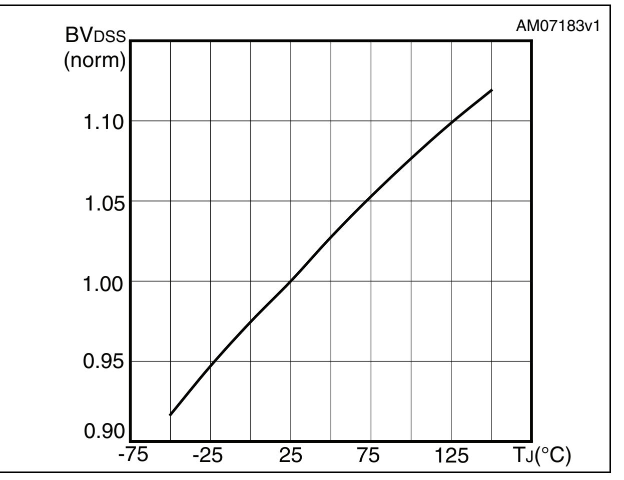
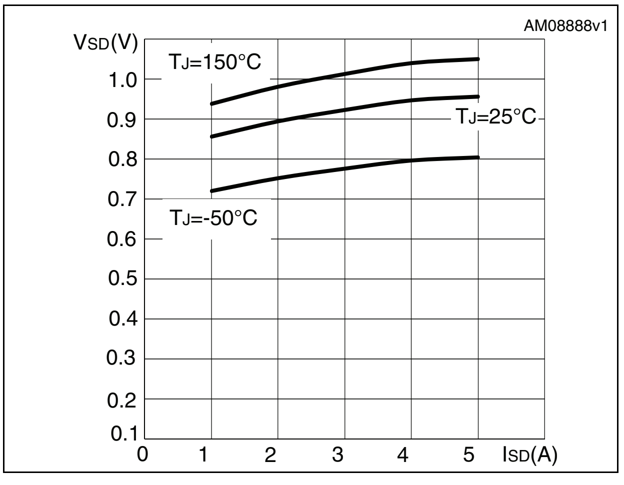


Figure 16. Source-drain diode forward characteristics



3 Test circuits

Figure 17. Switching times test circuit for resistive load

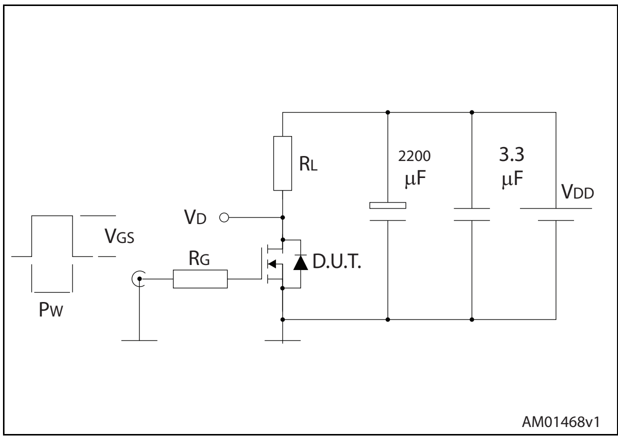


Figure 18. Gate charge test circuit

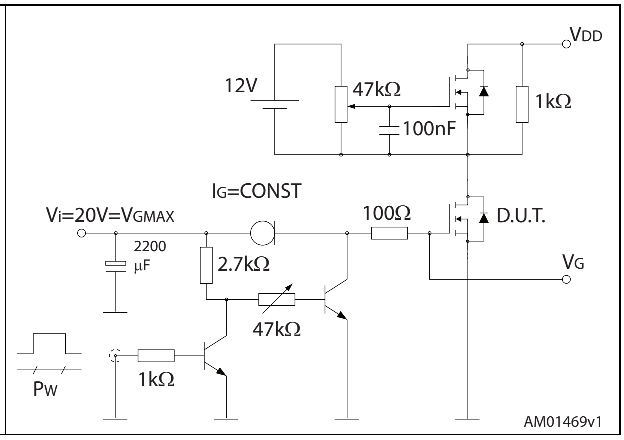


Figure 19. Test circuit for inductive load switching and diode recovery times

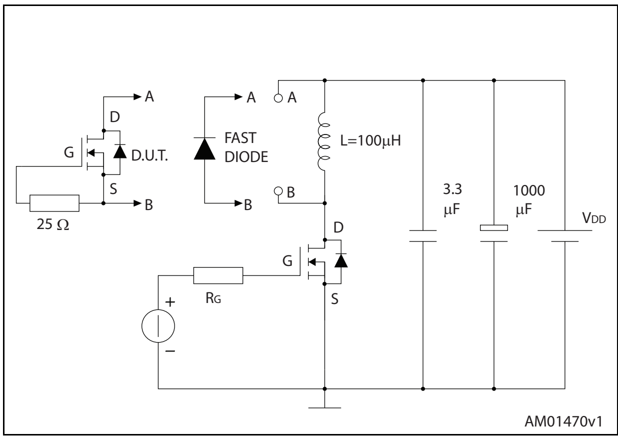


Figure 20. Unclamped Inductive load test circuit

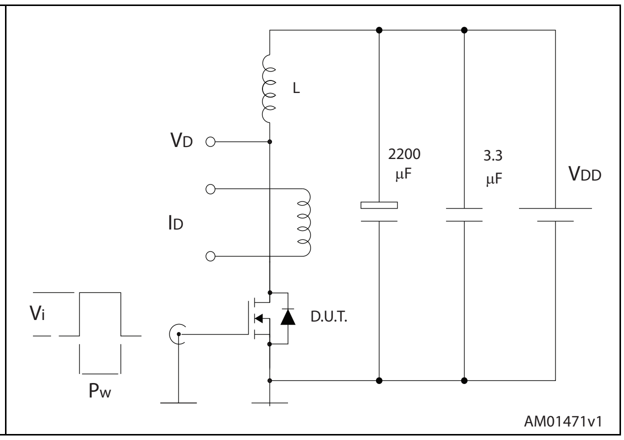


Figure 21. Unclamped inductive waveform

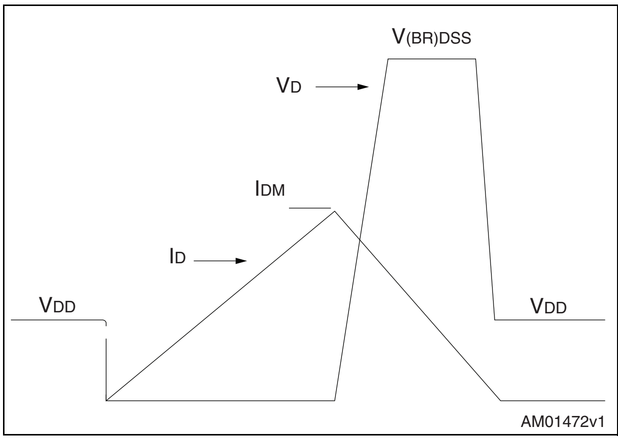
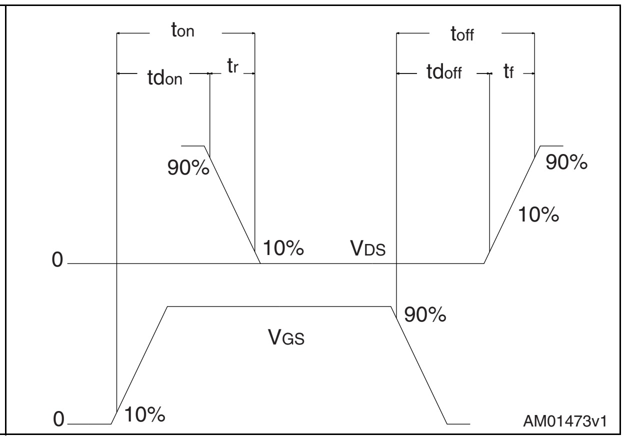


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. D^2PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D²PAK (TO-263) drawing

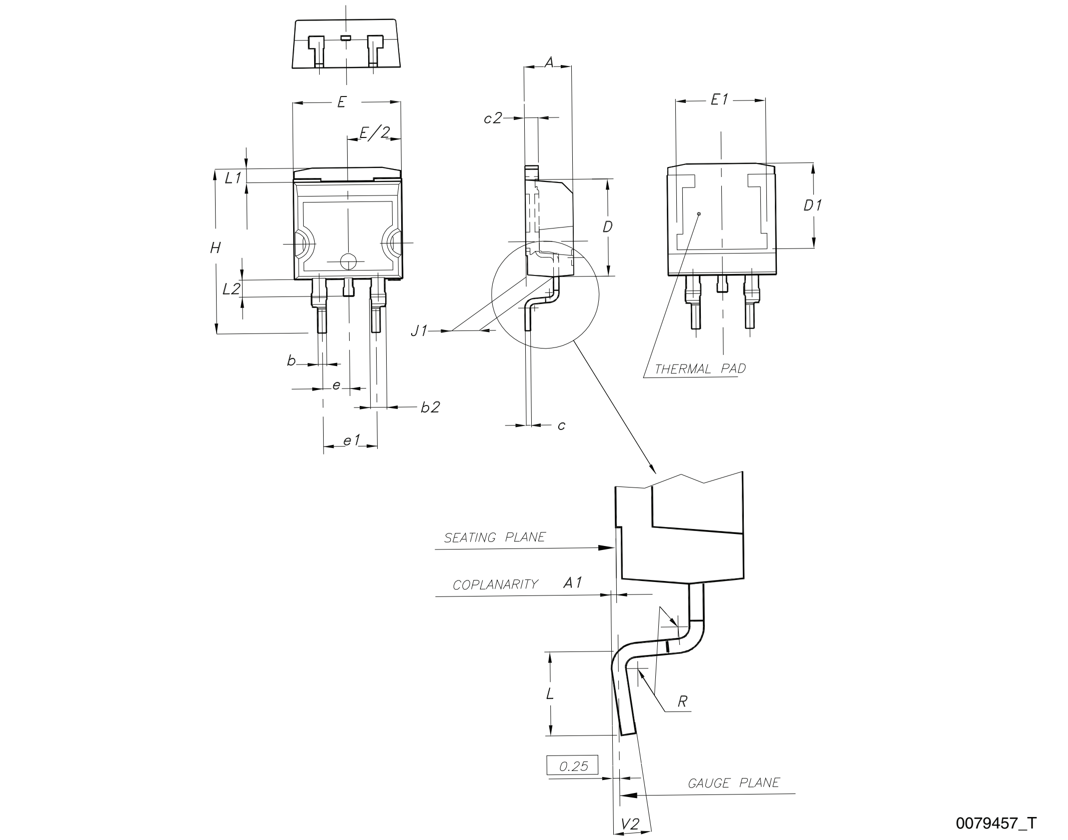
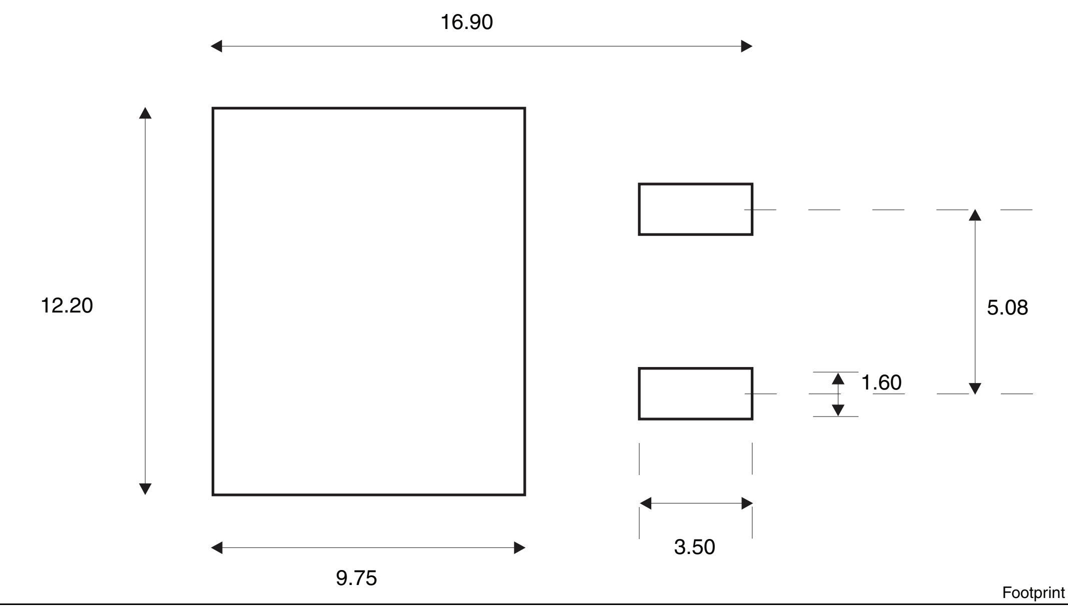


Figure 24. D²PAK footprint[(a)]



a. All dimension are in millimeters

Table 10. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) type A drawing

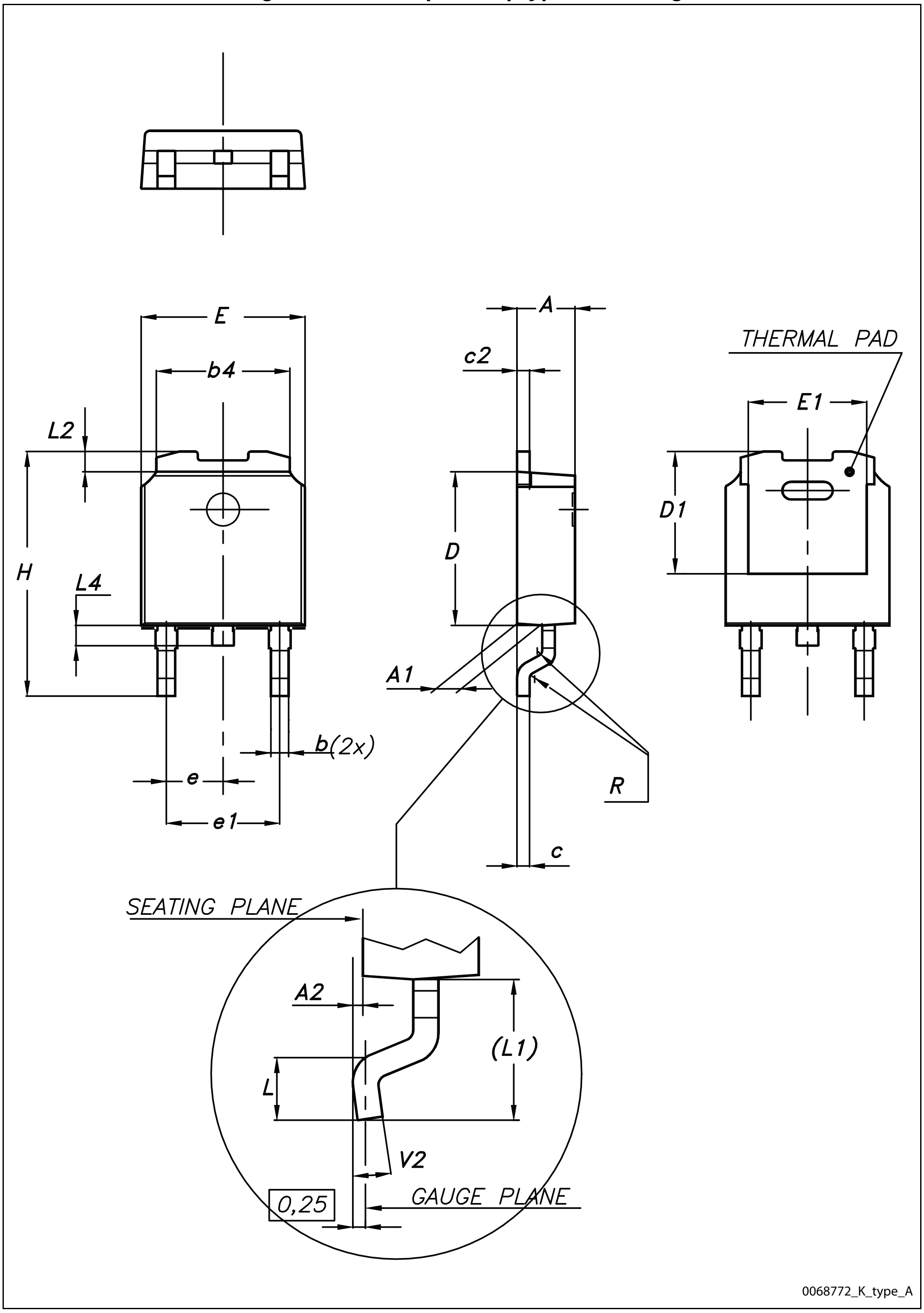


Table 11. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 26. DPAK (TO-252) type E drawing

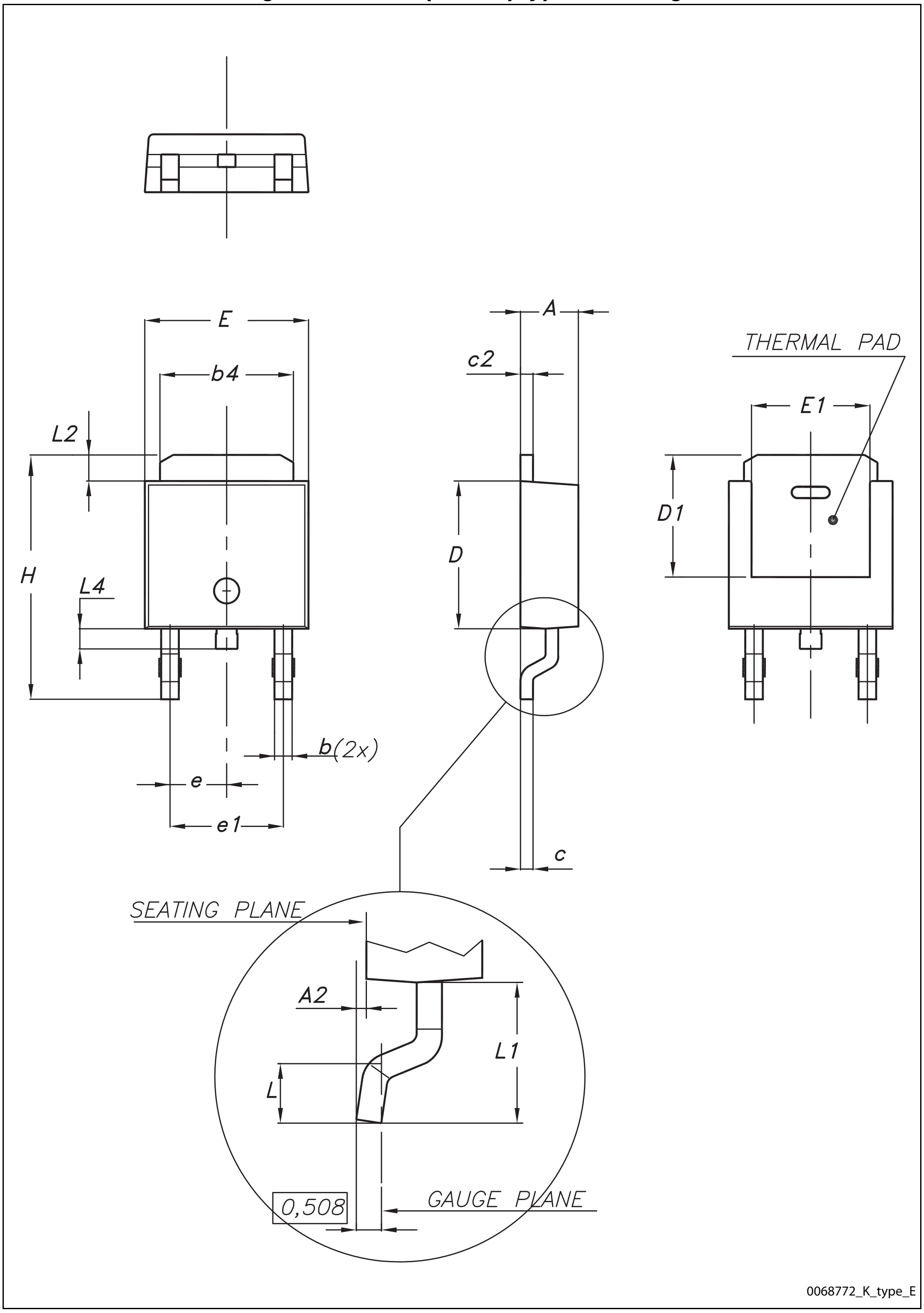
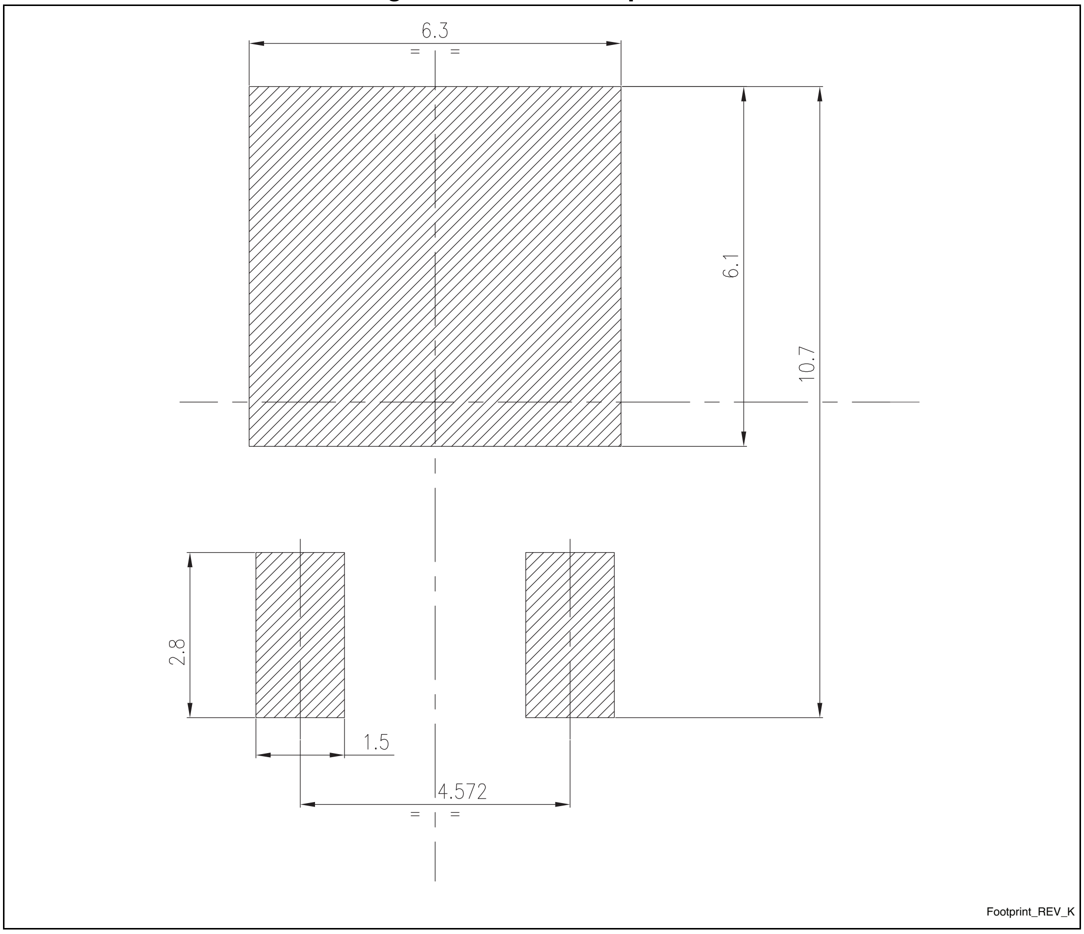


Figure 27. DPAK footprint [(b)]



b. All dimensions are in millimeters

5 Packaging mechanical data

Table 12. D^2PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 13. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500

Table 13. DPAK (TO-252) tape and reel mechanical data (continued)

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 28. Tape for D²PAK (TO-263) and DPAK (TO-252)

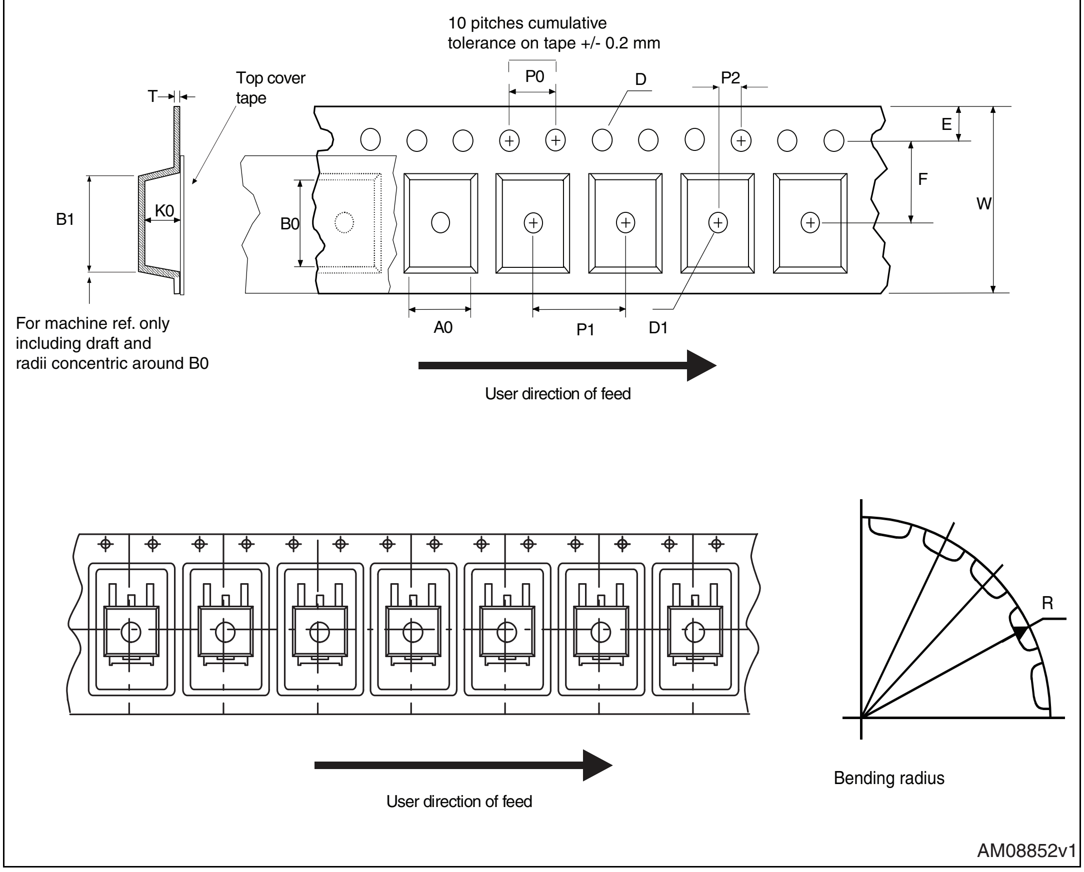
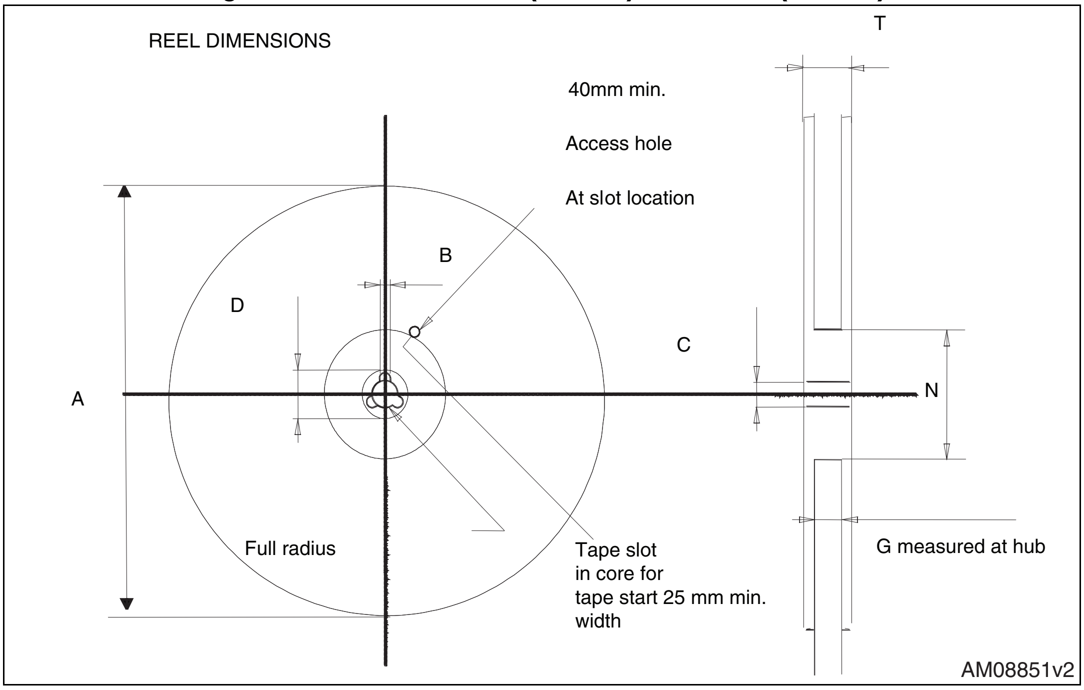


Figure 29. Reel for D²PAK (TO-263) and DPAK (TO-252)



6 Revision history

Table 14. Document revision history

Date	Revision	Changes
16-Dec-2010	1	First release.
26-Apr-2012	2	Added min and max values for R_G in *Table 5: Dynamic* and *Section 5: Packaging mechanical data*. Updated *Section 4: Package mechanical data*. Minor text changes.
09-Sep-2013	3	– Updated: *Section 4: Package mechanical data* – Minor text changes