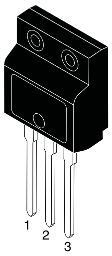
N-channel 650 V, 15 A, 0.250 Ω typ., MDmesh™ II Power MOSFET in a I²PAKFP package

Datasheet - production data



I^2PAKFP (TO-281)

Features

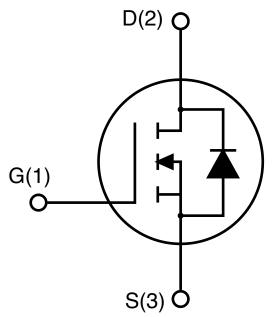
Order code	V_{DSS} @T_{jmax}	$R_{DS(on)}$ max.	I_D
STFI20NM65N	710 V	0.270 Ω	15 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Figure 1. Internal schematic diagram



Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STFI20NM65N	20NM65N	I^2PAKFP (TO-281)	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	650	V
V_{GS}	Gate source voltage	± 25	V
I_D	Drain current continuous T_C =25 °C	15(1)	A
I_D	Drain current continuous T_C =100 °C	9.45	A
I_{DM} (2)	Drain current pulsed	60	A
P_{TOT}	Total dissipation at T_C=25 °C	30	W
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heatsink (t=1 s; T_C = 25 °C)	2500	V
T_{stg} T_J	Storage temperature Max. operating junction temperature	-55 to 150 150	°C

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 15$ A, di/dt $\leq$ 400 A/μs, $V_{DS\ peak} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameters	Value	Unit
R_{thjc}	Thermal resistance junction-case max.	4.17	°C/W
R_{thja}	Thermal resistance junction-ambient max.	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameters	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\ max}$)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	115	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS}=0)	V_{DS} = 650 V			1	µA
		V_{DS} = 650 V, T_C=0			100	µA
I_{GSS}	Gate body leakage (V_{DS}=0)	V_{GS}= ±25 V, V_{DS}=0			100	nA
$V_{GS(th)}$	Gate threshold voltage	I_D = 250 µA, V_{GS} = V_{DS}	2	3	4	V
$R_{DS(on)}$	Static drain-source on- resistance	I_D=7.5 A, V_{GS}=10 V		0.250	0.270	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1MHz, V_{GS} = 0	-	1280	-	pF
C_{oss}	Output capacitance		-	110	-	pF
C_{rss}	Reverse capacitance		-	10	-	pF
$C_{oss\ eq}$ (1)	Equivalent output capacitance	V_{DS} = 0 to V_{GS} = 0	-	260	-	pF
R_G	Intrinsic gate resistance	f = 1MHz, I_D=0	-	4.8	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 15 A, V_{GS} = 10 V (see *Figure 14*)	-	44	-	nC
Q_{gs}	Gate source charge		-	8	-	nC
Q_{gd}	Gate-drain charge		-	22	-	nC

1. $C_{oss\ eq}$: defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80 % V_{DSS}.

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D=7.5 A R_g=4.7 Ω, V_{GS}=10 V (see *Figure 13*) (see *Figure 18*)	-	15	-	ns
t_r	Rise time		-	13.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	75	-	ns
t_f	Fall time		-	21	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source drain current		-		15	A
I_{SDM} (1)	Source drain current (pulsed)		-		60	A
V_{SD} (2)	Forward on voltage	I_{SD} = 15 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 15*)	-	455		ns
Q_{rr}	Reverse recovery charge		-	5.5		µC
I_{RRM}	Reverse recovery current		-	24.5		A
t_{rr}	Reverse recovery time	I_{SD} =15 A, di/dt = 100 A/µs V_{DD} = 60 V, Tj = 150 °C (see *Figure 15*)	-	710		ns
Q_{rr}	Reverse recovery charge		-	8		µC
I_{RRM}	Reverse recovery current		-	24		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

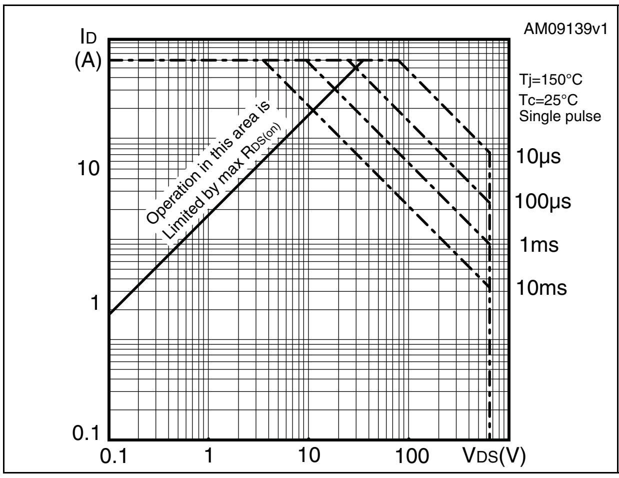


Figure 3. Thermal impedance

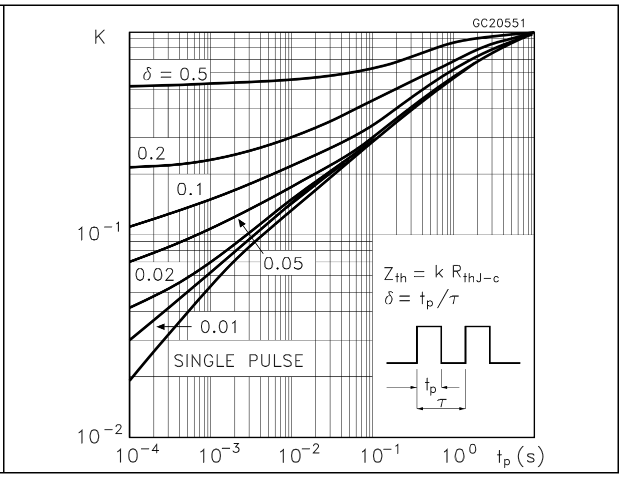


Figure 4. Output characteristics

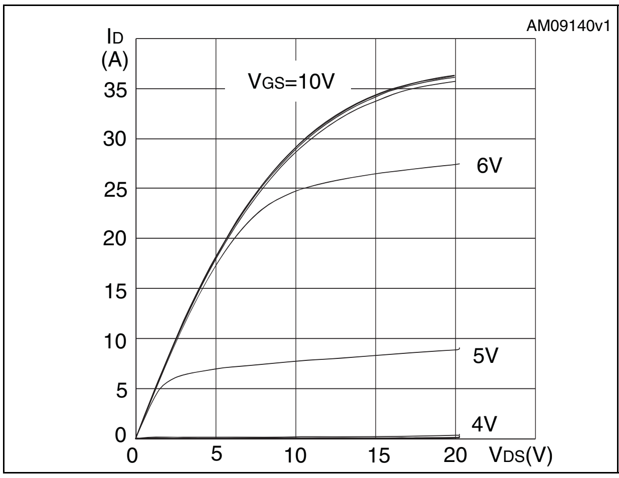


Figure 5. Transfer characteristics

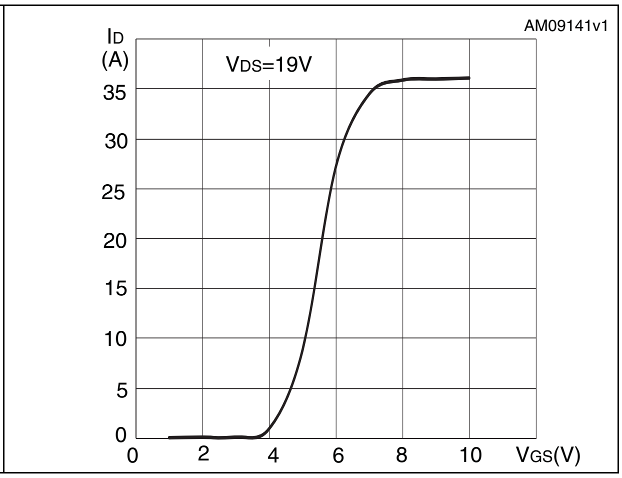


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

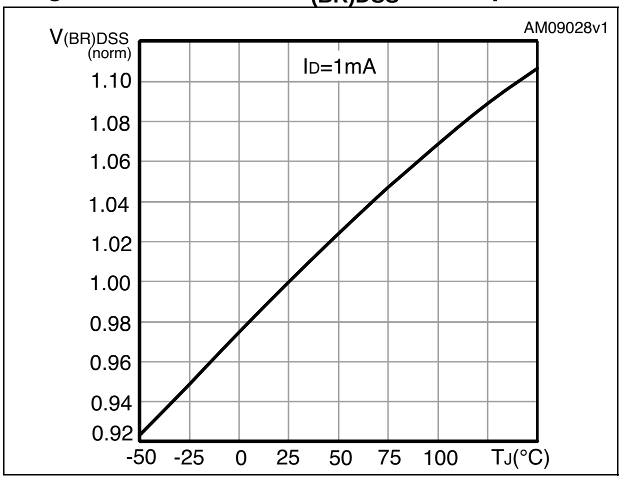


Figure 7. Static drain-source on-resistance

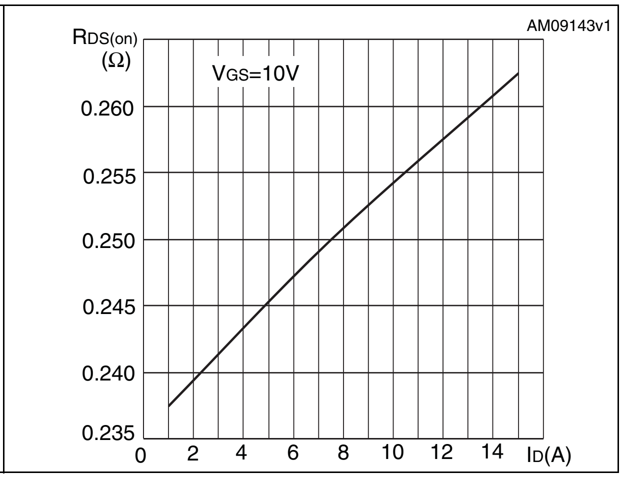


Figure 8. Gate charge vs gate-source voltage

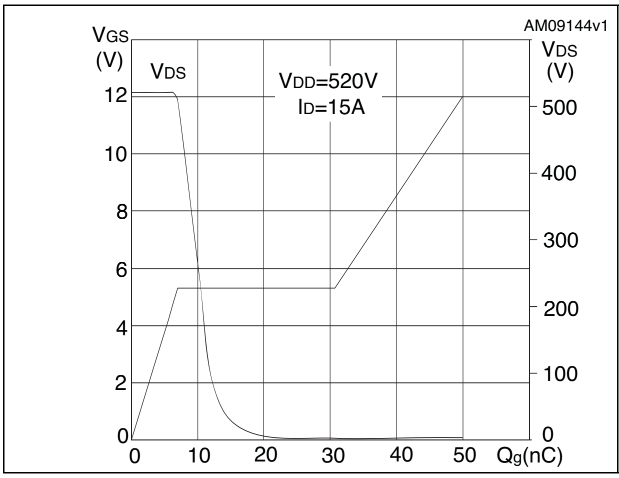


Figure 9. Capacitance variations

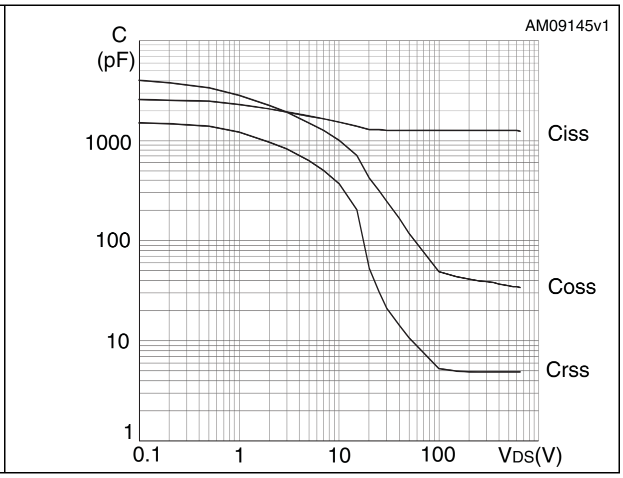


Figure 10. Normalized gate threshold voltage vs temperature

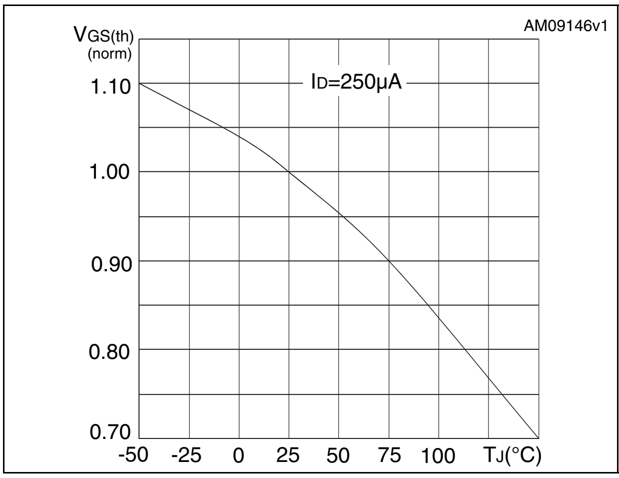


Figure 11. Normalized on-resistance vs temperature

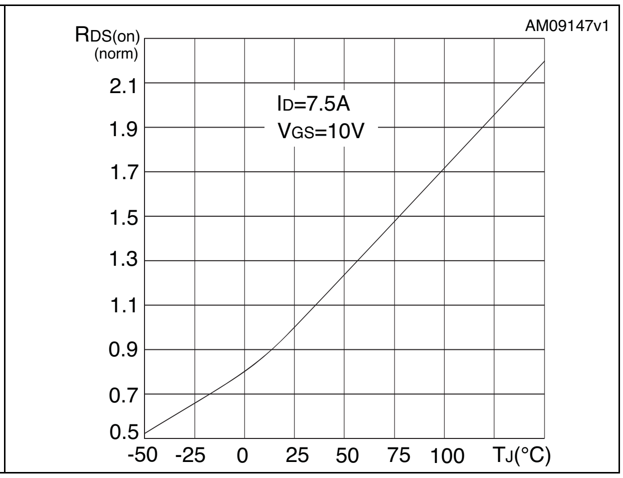
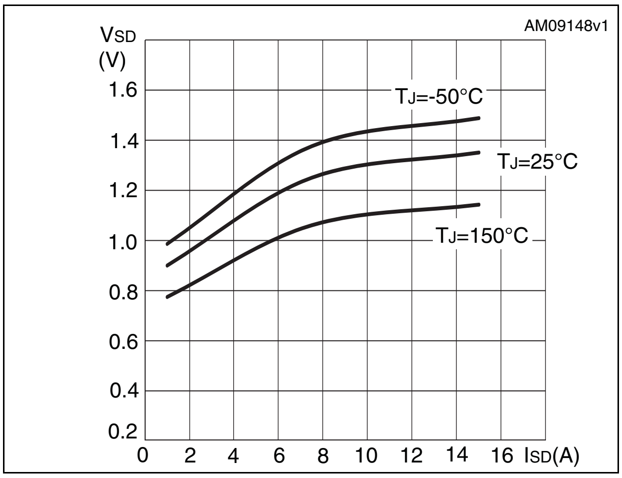


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

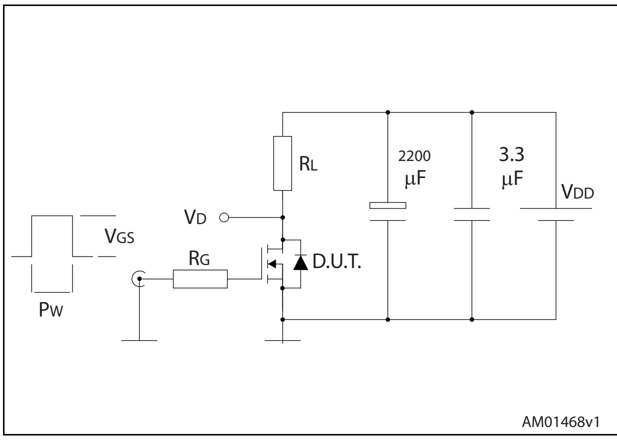


Figure 14. Gate charge test circuit

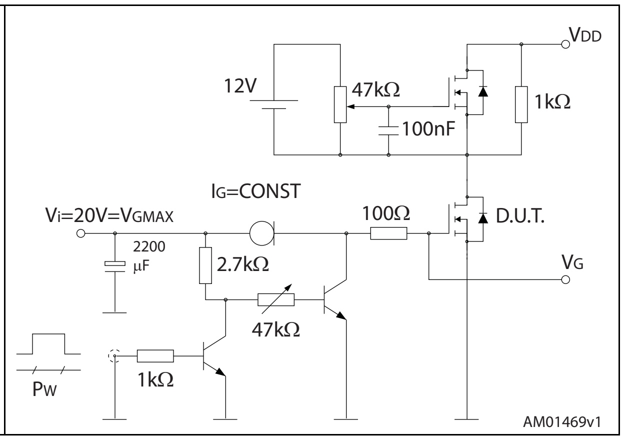


Figure 15. Test circuit for inductive load switching and diode recovery times

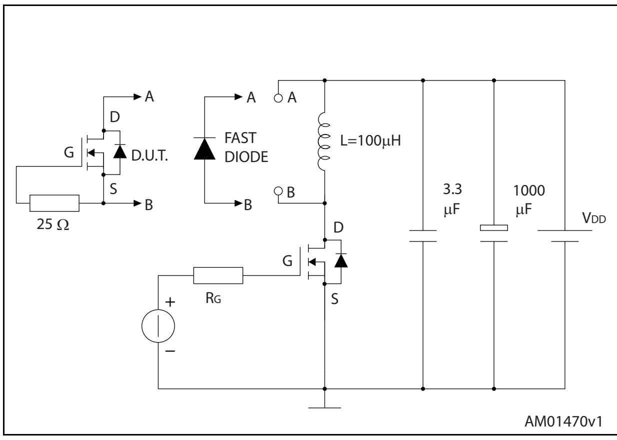


Figure 16. Unclamped inductive load test circuit

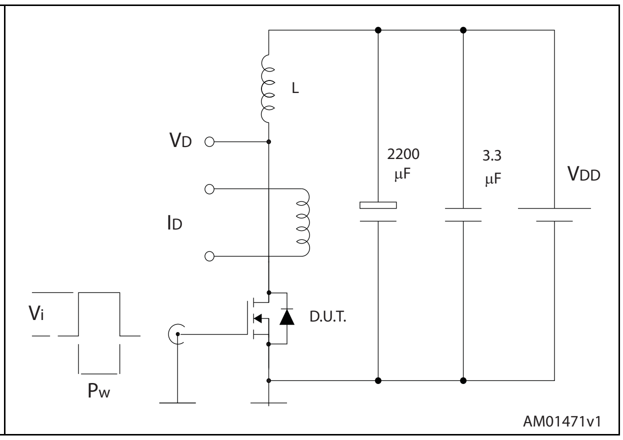


Figure 17. Unclamped inductive waveform

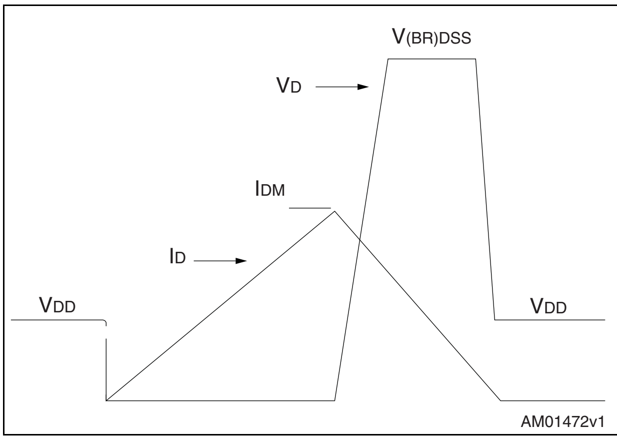
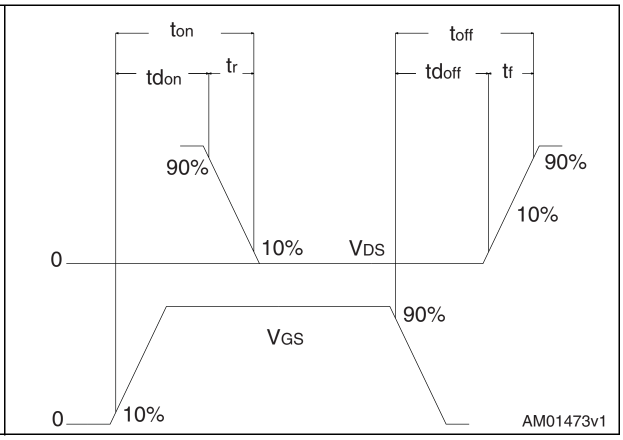


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. I^2PAKFP (TO-281) drawing

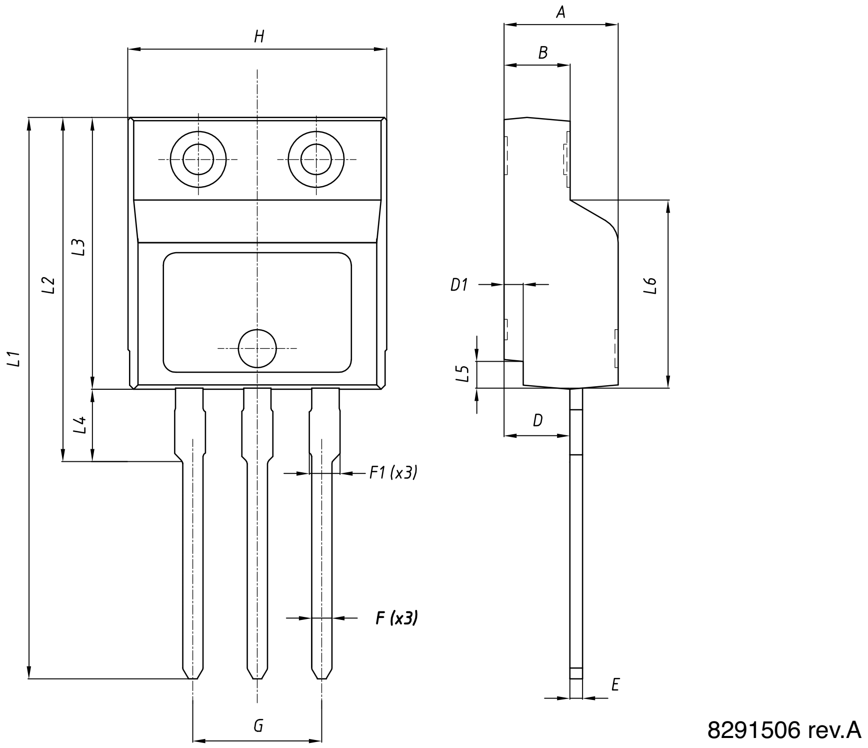


Table 9. I^2PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

5 Revision history

Table 10. Revision history

Date	Revision	Changes
20-Dec-2013	1	Initial release.