

N-channel 650 V, 15 A, 0.250 Ω typ., MDmesh™ II Power MOSFET in a I²PAKFP package

Datasheet - production data

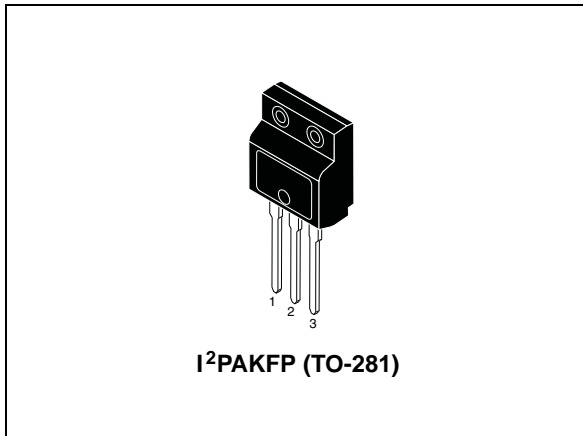
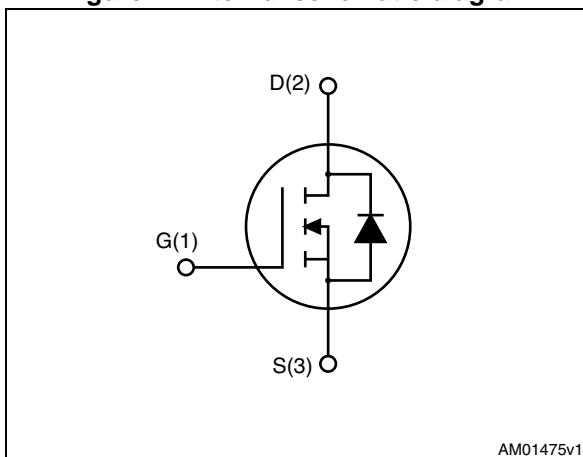


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS} @T _{jmax}	R _{DS(on)} max.	I _D
STFI20NM65N	710 V	0.270 Ω	15 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STFI20NM65N	20NM65N	I ² PAKFP (TO-281)	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	650	V
V_{GS}	Gate source voltage	± 25	V
I_D	Drain current continuous $T_C = 25\text{ }^\circ\text{C}$	15 ⁽¹⁾	A
I_D	Drain current continuous $T_C = 100\text{ }^\circ\text{C}$	9.45	A
$I_{DM}^{(2)}$	Drain current pulsed	60	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heatsink (t=1 s; $T_C = 25\text{ }^\circ\text{C}$)	2500	V
T_{stg} T_J	Storage temperature Max. operating junction temperature	-55 to 150 150	$^\circ\text{C}$

- Limited only by maximum temperature allowed.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 15\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameters	Value	Unit
R_{thjc}	Thermal resistance junction-case max.	4.17	$^\circ\text{C}/\text{W}$
R_{thja}	Thermal resistance junction-ambient max.	62.5	$^\circ\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameters	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\text{ max}}$)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	115	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS}=0$)	$V_{DS} = 650\text{ V}$			1	μA
		$V_{DS} = 650\text{ V}$, $T_C=0$			100	μA
I_{GSS}	Gate body leakage ($V_{DS}=0$)	$V_{GS} = \pm 25\text{ V}$, $V_{DS}=0$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = V_{DS}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on- resistance	$I_D=7.5\text{ A}$, $V_{GS}=10\text{ V}$		0.250	0.270	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1280	-	pF
C_{OSS}	Output capacitance		-	110	-	pF
C_{RSS}	Reverse capacitance		-	10	-	pF
$C_{OSS\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0$ to $V_{GS} = 0$	-	260	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D=0$	-	4.8	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 14)	-	44	-	nC
Q_{GS}	Gate source charge		-	8	-	nC
Q_{GD}	Gate-drain charge		-	22	-	nC

1. $C_{OSS\text{ eq}}$: defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80 % V_{DSS} .

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D=7.5\text{ A}$ $R_g=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$ (see Figure 13) (see Figure 18)	-	15	-	ns
t_r	Rise time		-	13.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	75	-	ns
t_f	Fall time		-	21	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source drain current		-		15	A
$I_{SDM}^{(1)}$	Source drain current (pulsed)		-		60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15 \text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 15 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 15)	-	455		ns
Q_{rr}	Reverse recovery charge		-	5.5		μC
I_{RRM}	Reverse recovery current		-	24.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 15 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15)	-	710		ns
Q_{rr}	Reverse recovery charge		-	8		μC
I_{RRM}	Reverse recovery current		-	24		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

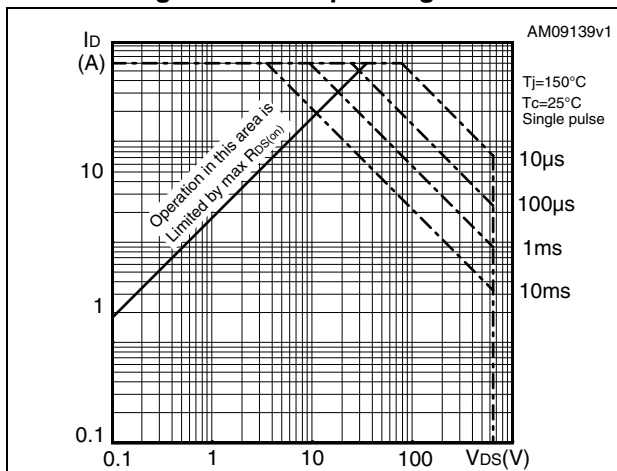


Figure 3. Thermal impedance

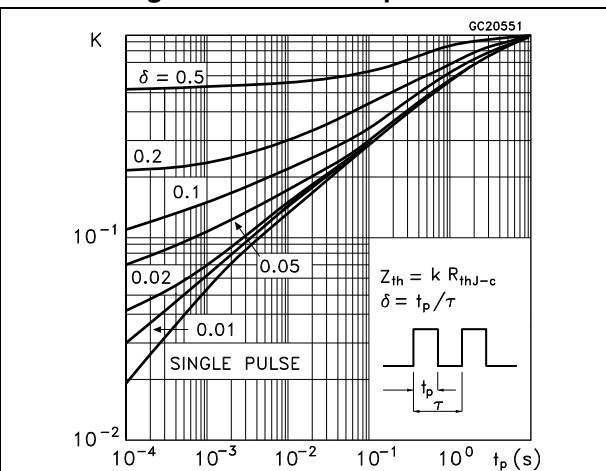


Figure 4. Output characteristics

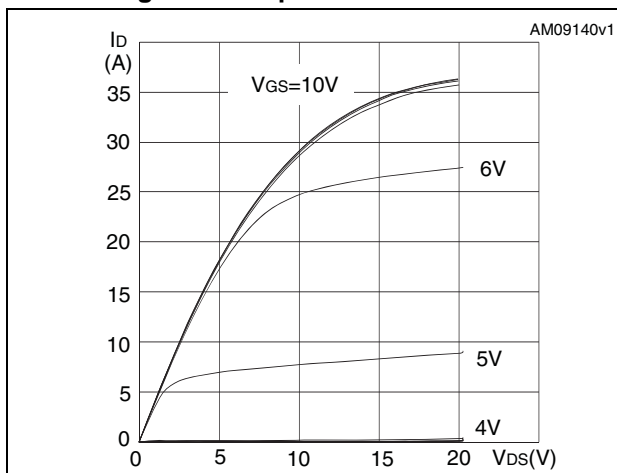


Figure 5. Transfer characteristics

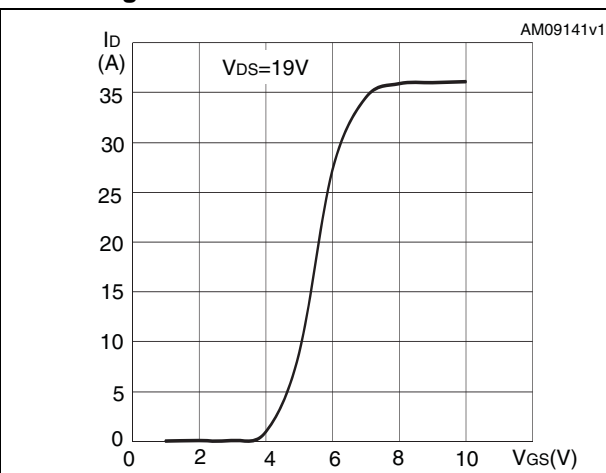


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

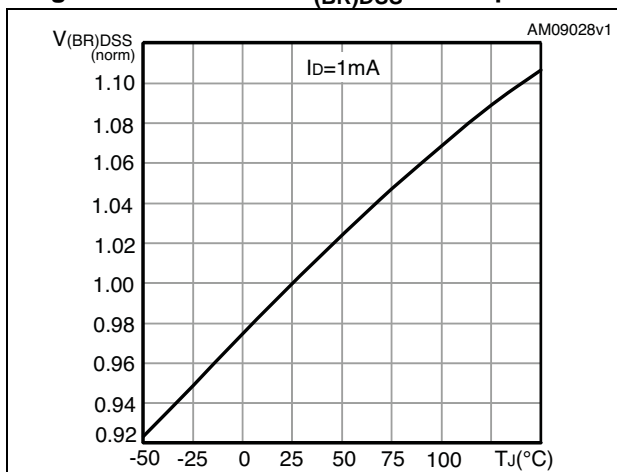


Figure 7. Static drain-source on-resistance

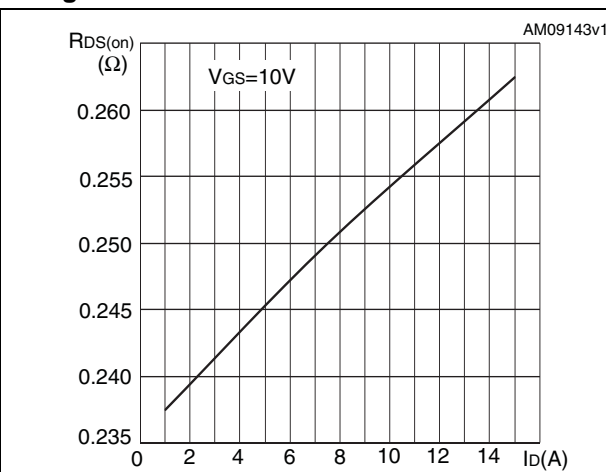


Figure 8. Gate charge vs gate-source voltage

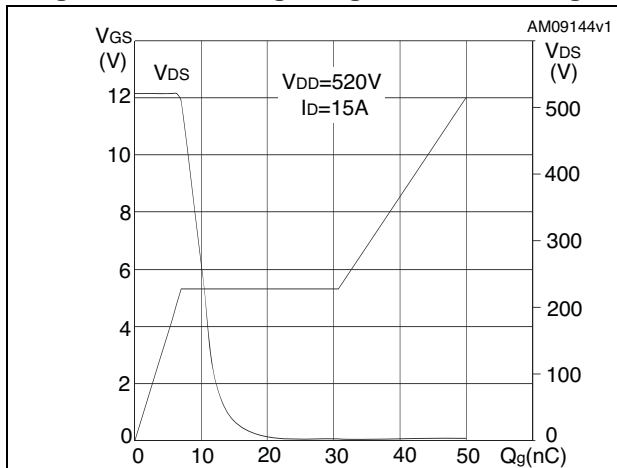


Figure 9. Capacitance variations

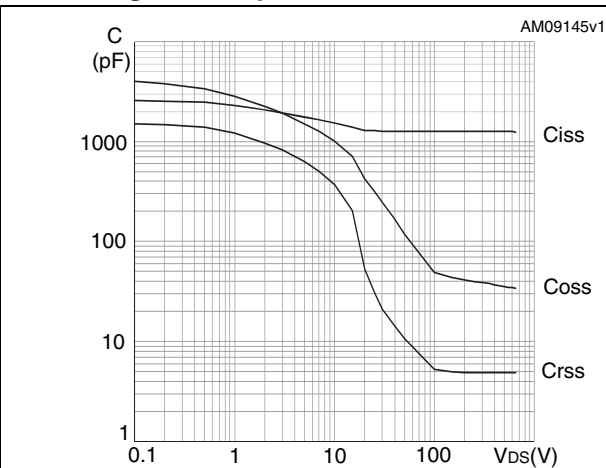


Figure 10. Normalized gate threshold voltage vs temperature

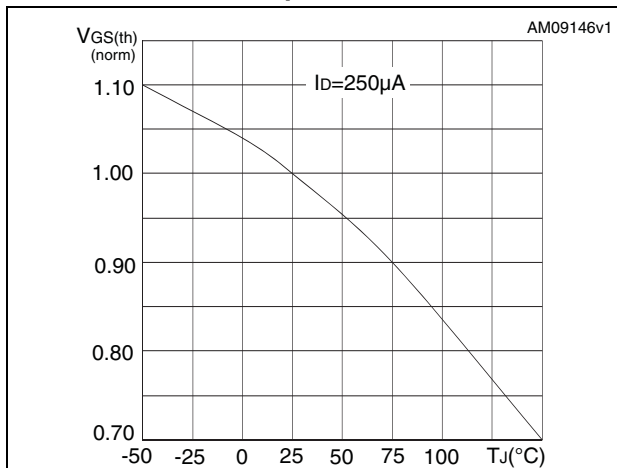


Figure 11. Normalized on-resistance vs temperature

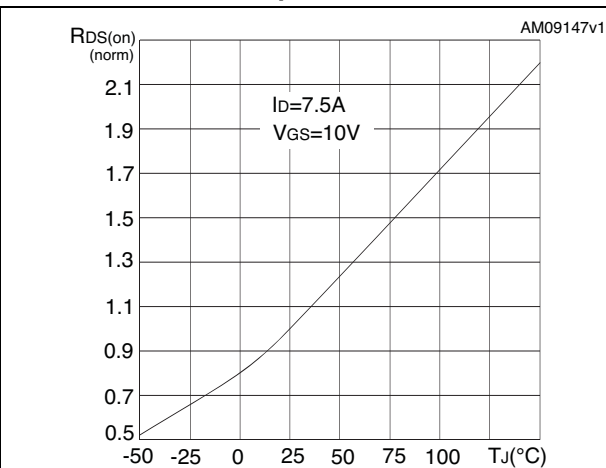
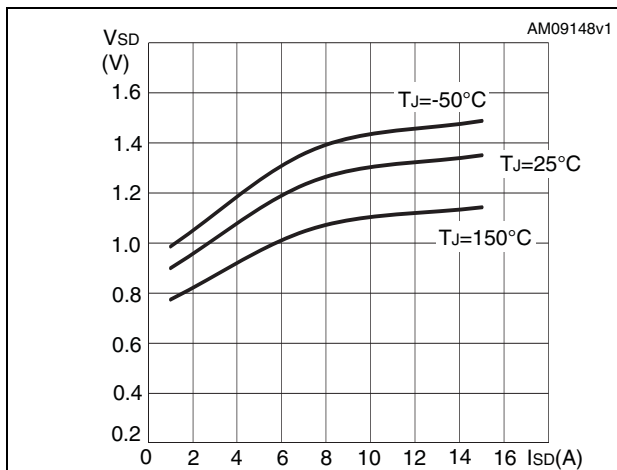


Figure 12. Source-drain diode forward characteristics



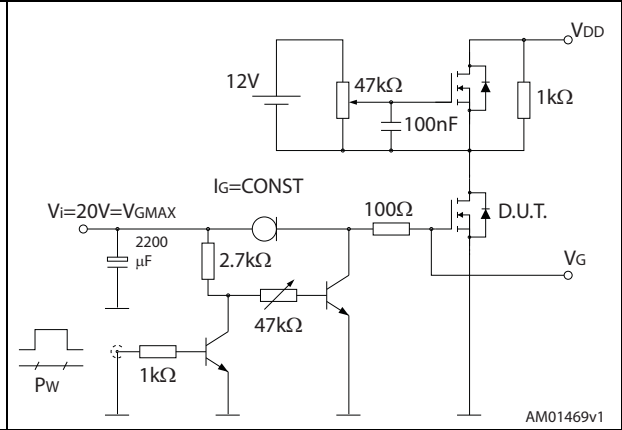
3 Test circuits

Figure 13. Switching times test circuit for resistive load



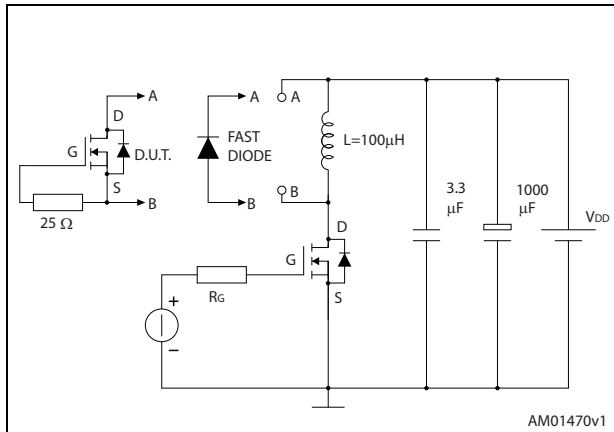
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Figure 14. Gate charge test circuit



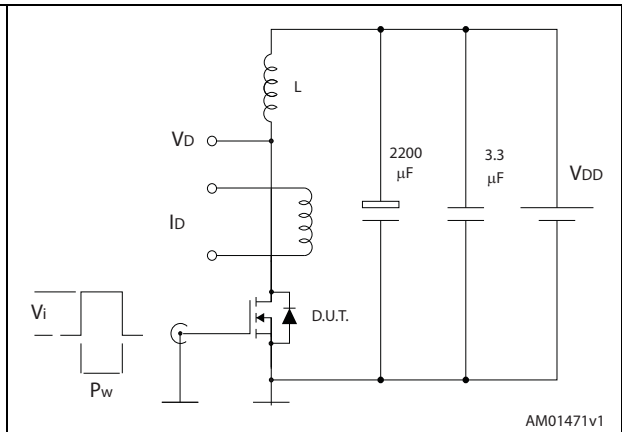
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Figure 15. Test circuit for inductive load switching and diode recovery times



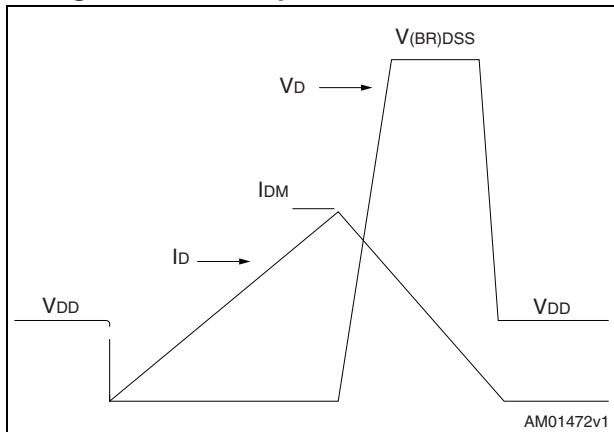
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Figure 16. Unclamped inductive load test circuit



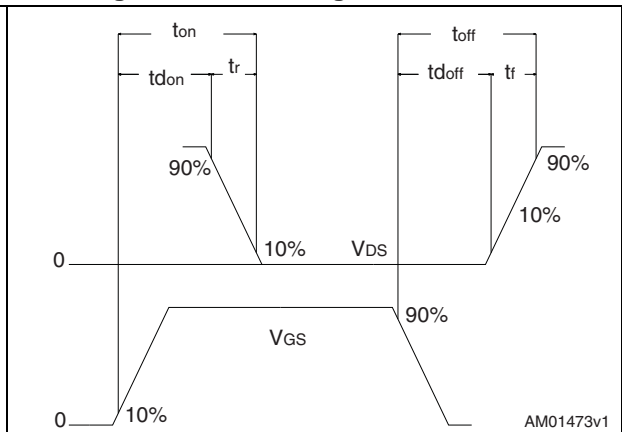
AM01471v1

Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform

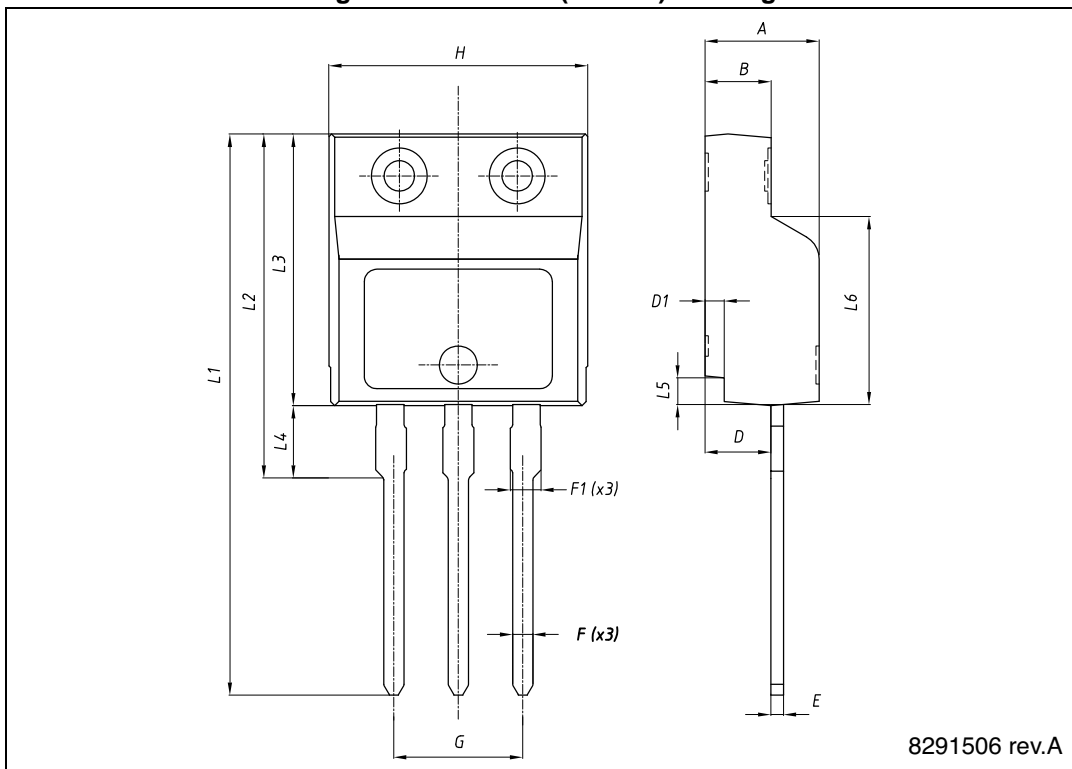


AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. I²PAKFP (TO-281) drawing



8291506 rev.A

Table 9. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

5 Revision history

Table 10. Revision history

Date	Revision	Changes
20-Dec-2013	1	Initial release.

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