



## STP40NF10L

N-channel 100V - 0.028 $\Omega$  - 40A TO-220  
Low gate charge STripFET™ Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP40NF10L	100V	<0.033 $\Omega$	40A

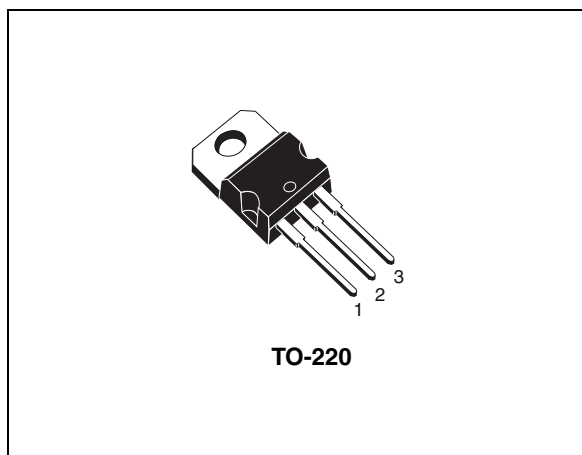
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

### Description

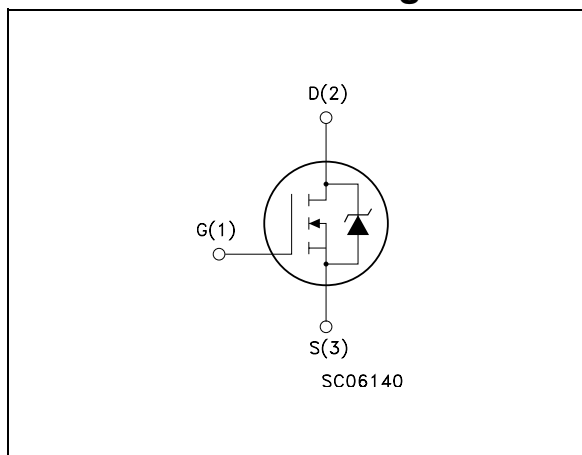
This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STP40NF10L	P40NF10L	TO-220	Tube

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $v_{GS} = 0$ )	100	V
$V_{GS}$	Gate- source voltage	$\pm 17$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	40	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	25	A
$I_{DM}^{(1)}$	Drain current (pulsed)	160	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	150	W
	Derating factor	1	W/°C
$E_{AS}^{(2)}$	Single pulse avalanche energy	430	mJ
$T_{stg}$	Storage temperature	- 65 to 175	°C
$T_j$	Max. operating junction temperature		

1. Pulse width limited by safe operating area

2. Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 20\text{A}$ ,  $V_{DD} = 40\text{V}$

**Table 2. Thermal data**

$R_{thj-case}$	Thermal resistance junction-case Max	1	°C/W
$R_{thj-a}$	Thermal resistance junction-ambient Max	62.5	°C/W
$T_l$	Maximum lead temperature for soldering purpose	300	°C

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage	$V_{DS} = \text{Max rating}$			1	$\mu A$
	Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}, T_C = 125^{\circ}C$			10	$\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 17V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 20A$		0.028	0.033	$\Omega$
		$V_{GS} = 5V, I_D = 20A$		0.030	0.036	$\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 20A$		25		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		2300		pF
$C_{oss}$	Output capacitance			290		pF
$C_{rss}$	Reverse transfer capacitance			125		pF
$Q_g$	Total gate charge	$V_{DD} = 80V, I_D = 40A, V_{GS} = 5V$		46	64	nC
$Q_{gs}$	Gate-source charge			12		nC
$Q_{gd}$	Gate-drain charge			22		nC

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5.

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time	$V_{DD} = 50V, I_D = 20A, R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 13)		25		ns
	Rise time			82		ns
$t_{d(off)}$ $t_f$	Turn-off-delay time	$V_{DD} = 50V, I_D = 20A, R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 13)		64		ns
	Fall time			24		ns
$t_{d(off)}$ $t_f$ $t_c$	Off-voltage Rise Time	$V_{clamp} = 80V, I_D = 40A, R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 15)		51		ns
	Fall Time			29		ns
	Cross-over time			53		ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current				40	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				160	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40A, V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 40A, V_{DD} = 30V$ $di/dt = 100A/\mu s,$ $T_j = 150^\circ C$ (see Figure 15)		110		ns
$Q_{rr}$	Reverse recovery charge			467		nC
$I_{RRM}$	Reverse recovery current			8		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

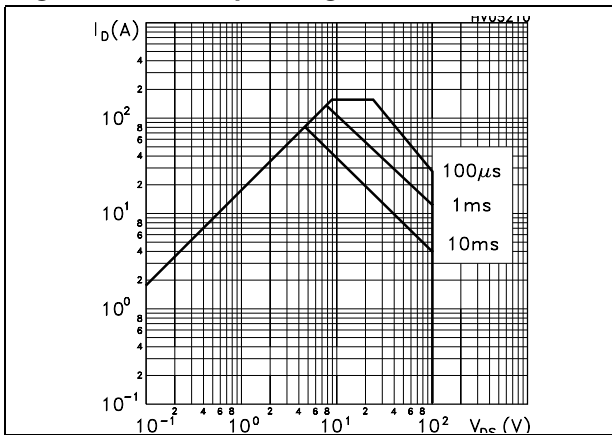


Figure 2. Thermal impedance

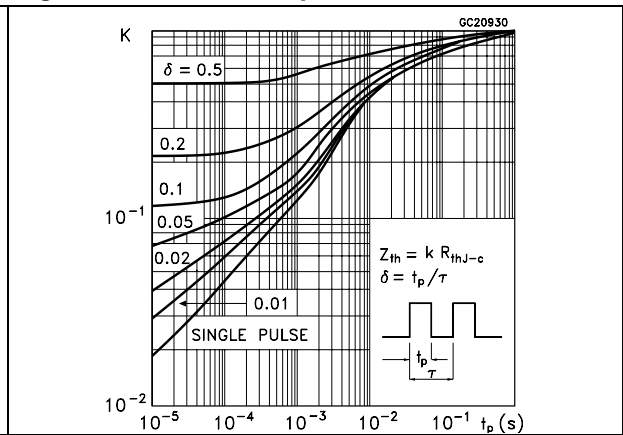


Figure 3. Output characteristics

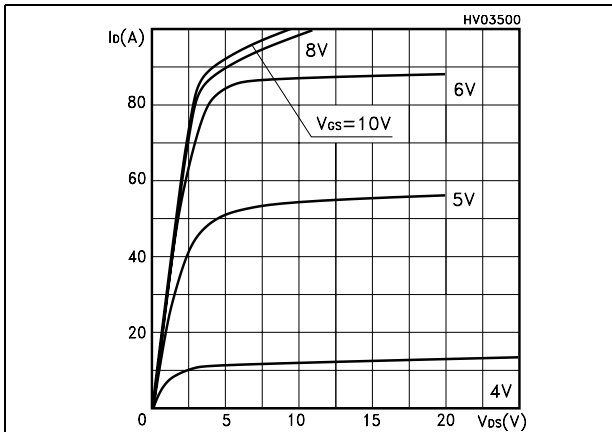


Figure 4. Transfer characteristics

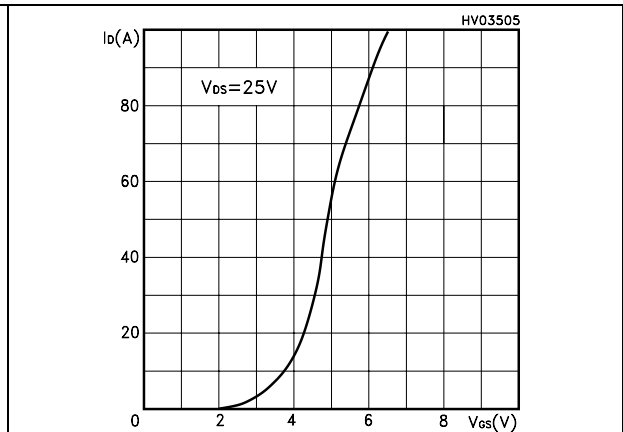


Figure 5. Transconductance

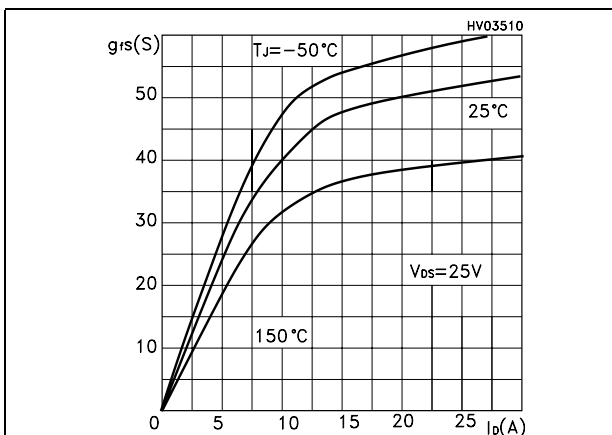


Figure 6. Static drain-source on resistance

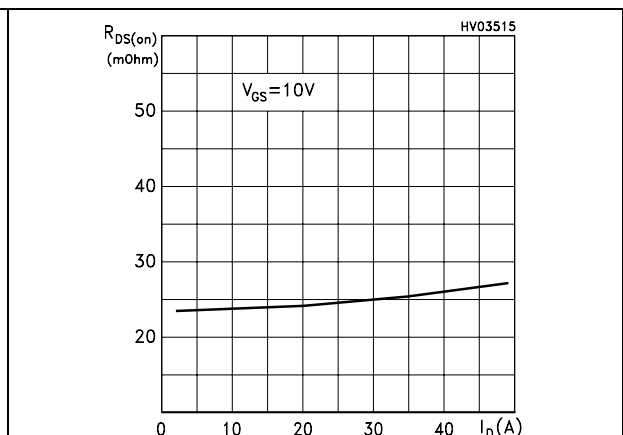


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

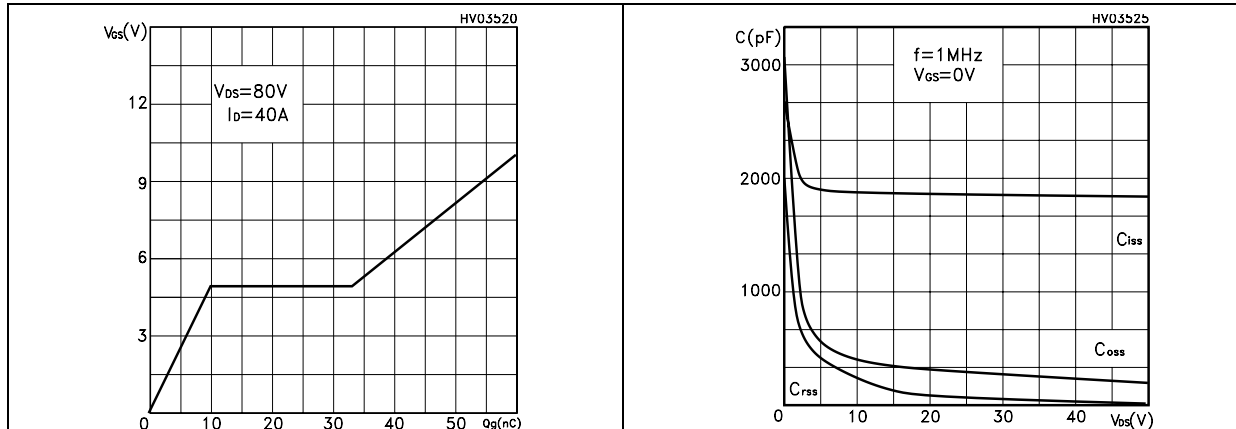


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

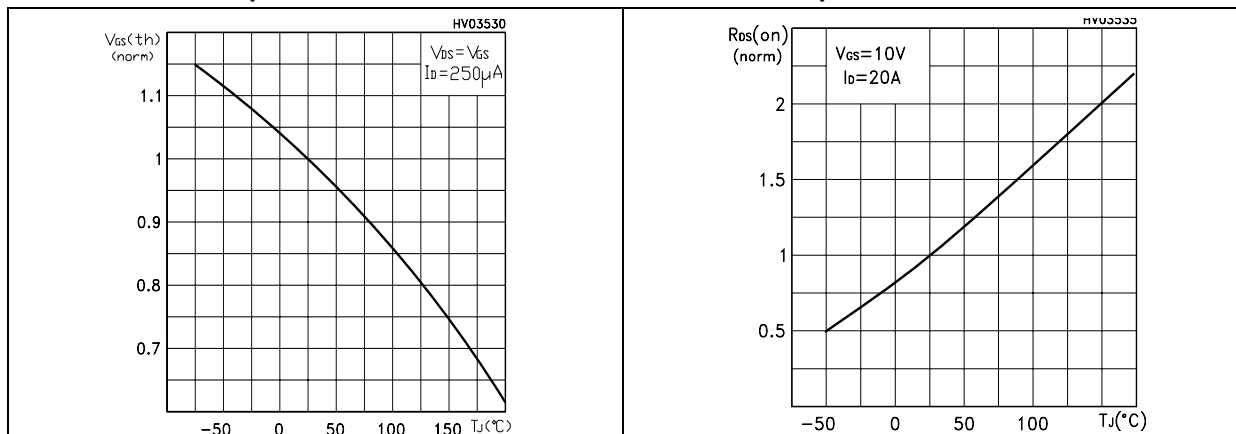
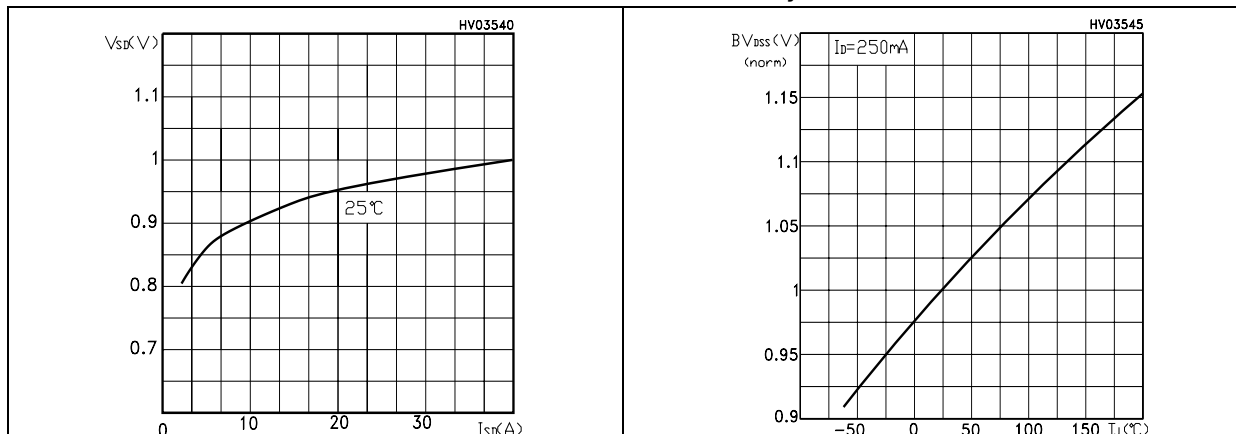


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs.  $t_j$



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

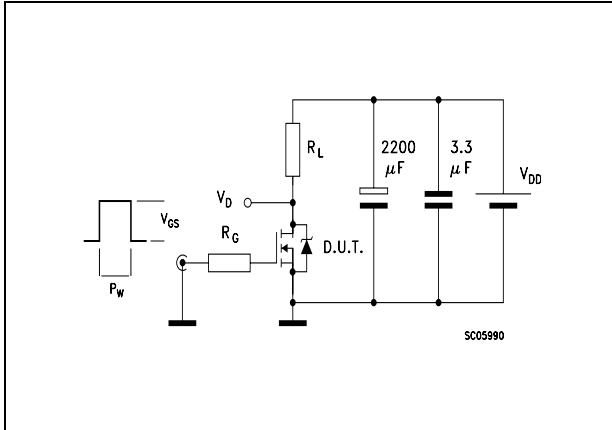


Figure 14. Gate charge test circuit



Figure 15. Test circuit for inductive load switching and diode recovery times

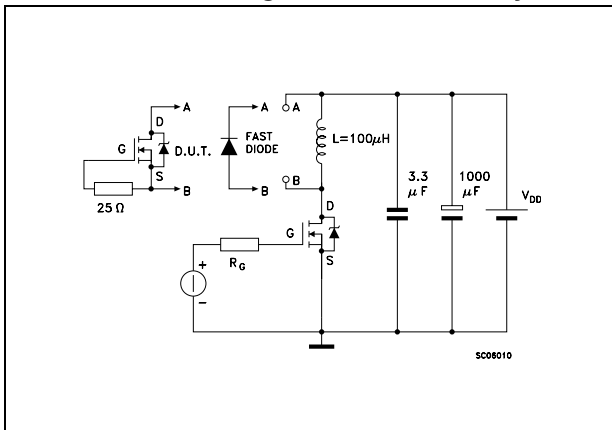


Figure 16. Unclamped Inductive load test circuit



Figure 17. Unclamped inductive waveform

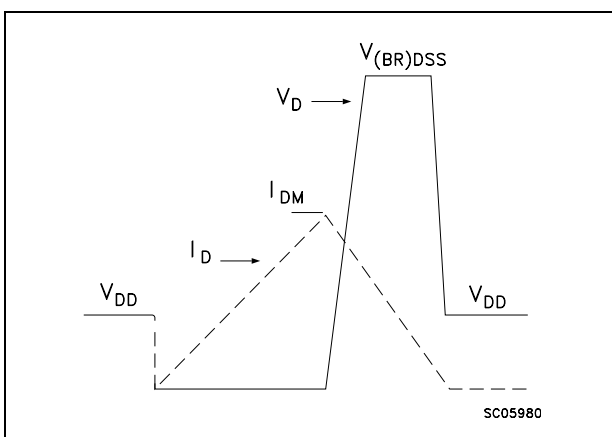


Figure 18. Switching time waveform



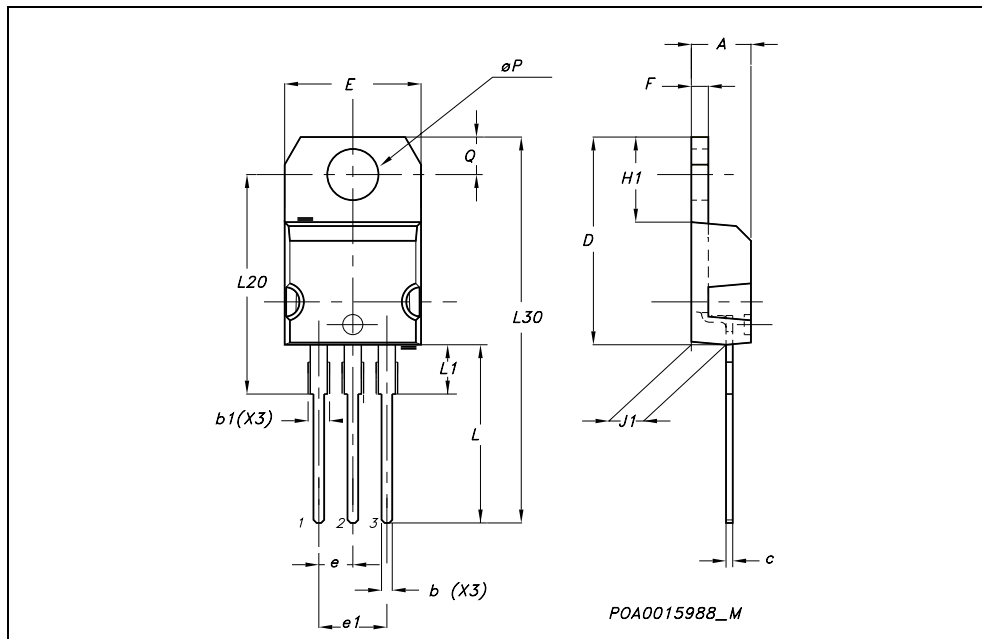


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : [www.st.com](http://www.st.com)

**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



## 5 Revision history

**Table 7. Revision history**

Date	Revision	Changes
09-Sep-2004	1	First version.
17-Aug-2006	2	The document has been reformatted.
31-Jan-2007	3	Typo mistake on <a href="#">Table 1</a> .

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