



VN330SP-E

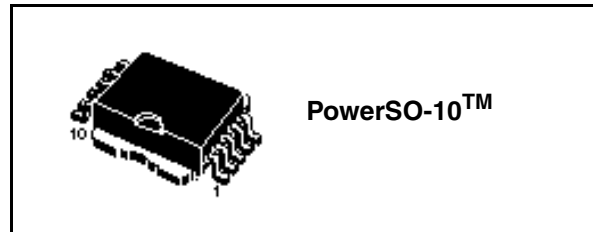
Quad high side smart
Power solid state relay

Features

Type	$V_{\text{demag}}^{(1)}$	$R_{\text{DSon}}^{(1)}$	$I_{\text{out}}^{(1)}$	V_{CC}
VN330SP-E	$V_{\text{CC}}-55\text{V}$	$0.32\Omega^{(2)}$	0.7A	36V

1. Per channel.
2. At $T_J = 85^\circ\text{C}$

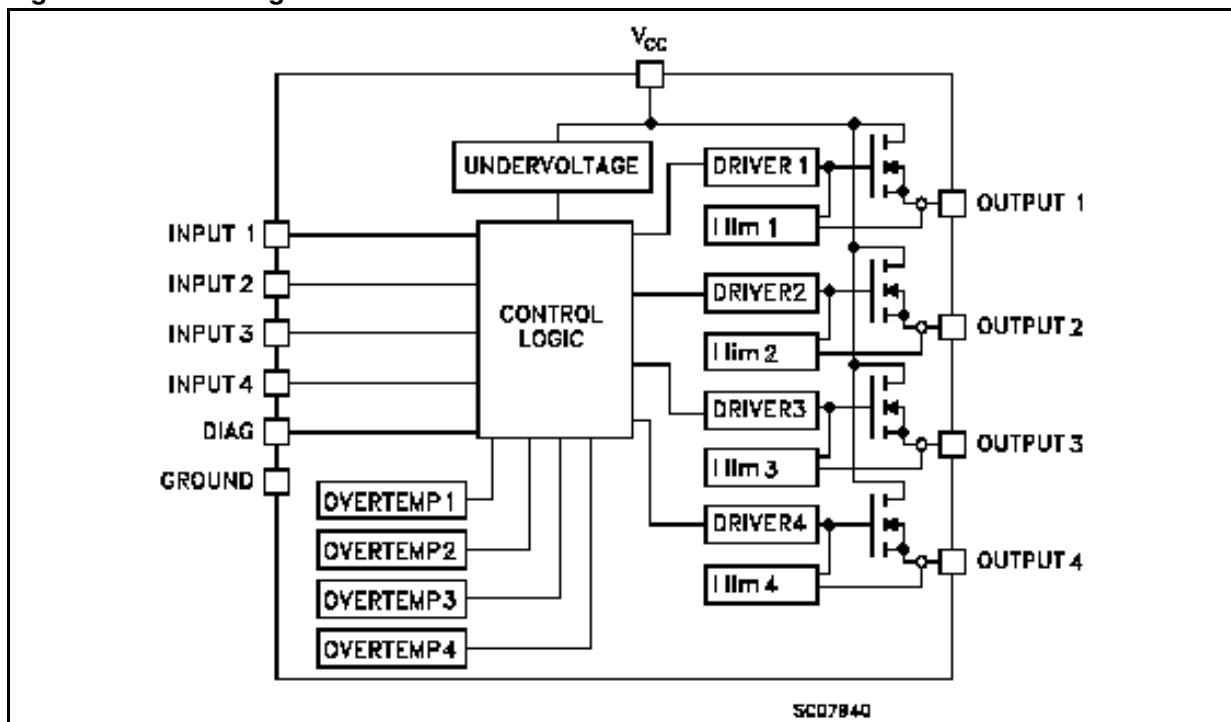
- Output current : 0.7A per channel
- Digital input clamped at 32V minimum voltage
- Shorted load and overtemperature protections
- Built-in current limiter
- Undervoltage shut-down
- Open drain diagnostic output
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2



Description

The VN330SP-E is a monolithic device made using STMicroelectronics VIPower technology, intended for driving four independent resistive or inductive loads, with one side connected to ground. Active current limitation avoids dropping the system power supply in case of shorted load. Built-in thermal shut-down protects the chip from overtemperature and short circuit. The open drain diagnostic output indicates overtemperature conditions.

Figure 1. Block diagram



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1 Maximum ratings

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
I_{OUT}	Output current (continuous)	Internally limited	A
I_R	Reverse output current (per channel)	-6	A
I_{IN}	Input current (per channel)	± 10	mA
I_{DIAG}	Diag pin current	± 10	mA
V_{ESD}	Electrostatic discharge (R = 1.5K Ω ; C = 100pF)	2000	V
E_{AS}	Single pulse avalanche energy per channel not simultaneously <i>Figure 4.</i>	400	mJ
P_{tot}	Power dissipation at $T_c = 25^\circ\text{C}$	Internally limited	w
T_J	Junction operating temperature	Internally limited	$^\circ\text{C}$
T_{STG}	Storage temperature	-55 to 150	$^\circ\text{C}$

Table 2. Thermal data

Symbol	Parameter	Max Value	Unit
R_{thJC}	Thermal resistance junction-case ⁽¹⁾	Max 2	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance junction-ambient ⁽²⁾	Max 50	$^\circ\text{C}/\text{W}$

1. Per channel
2. When mounted using minimum recommended pad size on FR-4 board

2 Pin connections

Figure 2. Connection diagram (top view)

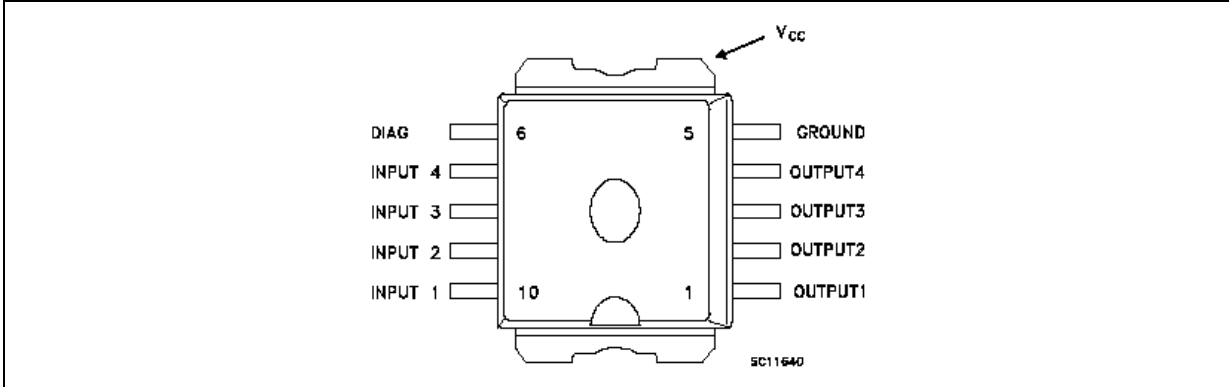
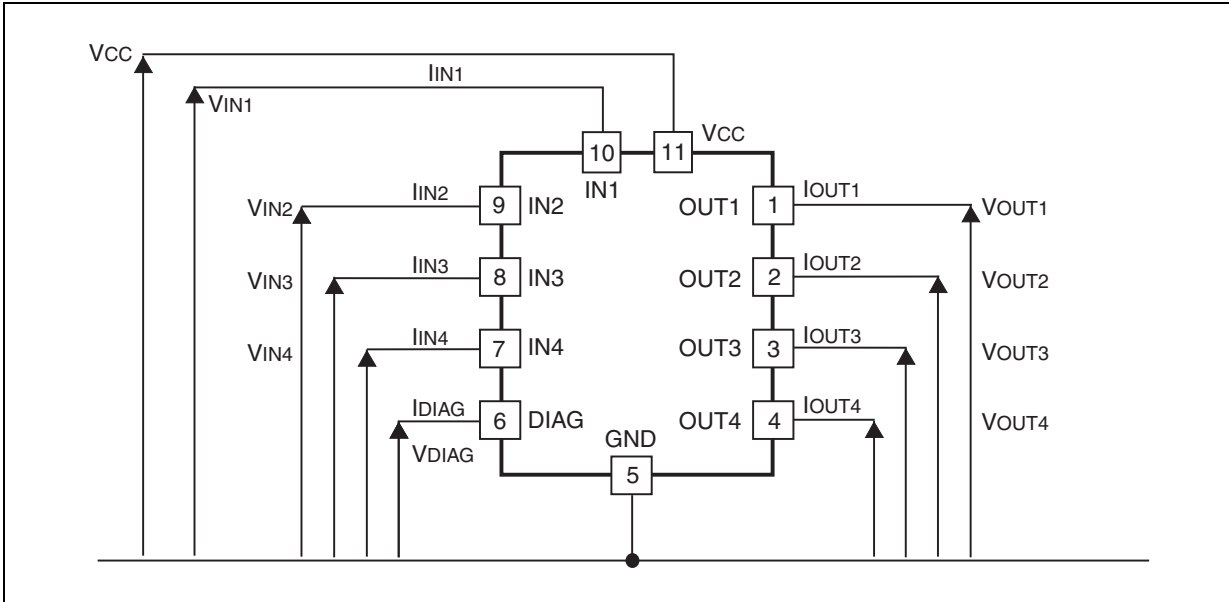


Figure 3. Current and voltage conventions



3 Electrical characteristics

$10V < V_{CC} < 36V$; $-40^{\circ}C < T_J < 125^{\circ}C$; unless otherwise specified

Table 3. Power section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage		10		36	V
R_{ON}	On state resistance	$I_{OUT} = 0.5A$; $T_J = 25^{\circ}C$ $I_{OUT} = 0.5A$; $T_J = 85^{\circ}C$ $I_{OUT} = 0.5A$; $T_J = 125^{\circ}C$			0.2 0.32 0.4	Ω Ω Ω
I_S	Supply current	All channels OFF On state; $V_{IN} = 30V$; $I_{OUT} = 0V$ ($T_J = 125^{\circ}C$)			1 6	mA mA
V_{demag}	Output voltage at turn-off	$I_{OUT} = 0.5A$; $L_{LOAD} \geq 1mH$	$V_{CC}-65$	$V_{CC}-55$	$V_{CC}-45$	V

Table 4. Switching ($V_{CC} = 24V$)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(ON)}$	Turn-on delay time of Output current	$I_{OUT} = 0.5A$, Resistive Load Input rise time $< 0.1\mu s$, $T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$		30	40 60	μs μs
t_r	Rise time of Output current	$I_{OUT} = 0.5A$, Resistive Load Input rise time $< 0.1\mu s$, $T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$		50	100 115	μs μs
$t_{d(OFF)}$	Turn-off delay time of Output current	$I_{OUT} = 0.5A$, Resistive Load Input rise time $< 0.1\mu s$, $T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$		20	30 40	μs μs
t_f	Fall time of Output current	$I_{OUT} = 0.5A$, Resistive Load Input rise time $< 0.1\mu s$, $T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$		8	15 20	μs μs
$(di/dt)_{on}$	Turn-on current slope	$I_{OUT} = 0.5A$, $I_{OUT} = I_{LIM}$, $T_J = 25^{\circ}C$			0.5 2	A/ μs A/ μs
$(di/dt)_{off}$	Turn-off current slope	$I_{OUT} = 0.5A$, $I_{OUT} = I_{LIM}$, $T_J = 25^{\circ}C$			2 4	A/ μs A/ μs

Table 5. Logical input

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				2	V
V_{IH}	Input high level voltage ⁽¹⁾		3.5			V
$V_{I(HYST)}$	Input hysteresis voltage			0.5		V
I_{IN}	Input current	$V_{IN} = 0$ to 30V			600	μ A
I_{LGND}	Output current in ground disconnection	$V_{CC} = V_{INn} = GND = DIAG = 24V$; $T_J = 25^\circ C$			25	mA
V_{ICL}	Input clamp voltage ⁽¹⁾	$I_{IN} = 1mA$ $I_{IN} = -1mA$	32	36 -0.7		V V

1. The input voltage is internally clamped at 32V minimum, however, it is possible to connect the input pins to an higher voltage via an external resistor that is calculated not to exceed 10mA.

Table 6. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DIAG}^{(1)}$	Status voltage output low	$I_{DIAG} = 5mA$ (Fault condition)			1	V
$V_{SCL}^{(1)}$	Status clamp voltage	$I_{DIAG} = 1mA$ $I_{DIAG} = -1mA$	32	36 -0.7		V V
V_{USD}	Undervoltage shut down		5		8	V
V_{OL}	Low state output voltage	$V_{IN} = V_{IL}$; $R_{LOAD} < 10m\Omega$			1.5	V
I_{LIM}	DC Short circuit current	$V_{CC} = 24V$; $R_{LOAD} < 10m\Omega$	0.7		2.5	A
I_{OVPK}	Peak Short circuit current	$V_{CC} = 24V$; $V_{IN} = 30$; $R_{LOAD} < 10m\Omega$			4	A
I_{DIAGH}	Leakage on DIAG pin in high state	$V_{DIAG} = 24V$			100	μ A
I_{LOAD}	Output leakage current	$V_{CC} = 10$ to 36V; $V_{IN} = V_{IL}$			50	μ A
t_{SC}	Delay time of current limiter				100	μ s
T_{TSD}	Thermal shutdown temperature		150	170		$^\circ C$
T_R	Thermal reset temperature		135	155		$^\circ C$

1. Status determination > 100 μ s after the switching edge.

Note: If INPUT pin is floating the corresponding channel will automatically switch OFF. If GND pin is disconnected, the channel will switch OFF provided V_{CC} not exceed 36V.

4 Test circuits

Figure 4. Avalance energy test circuit

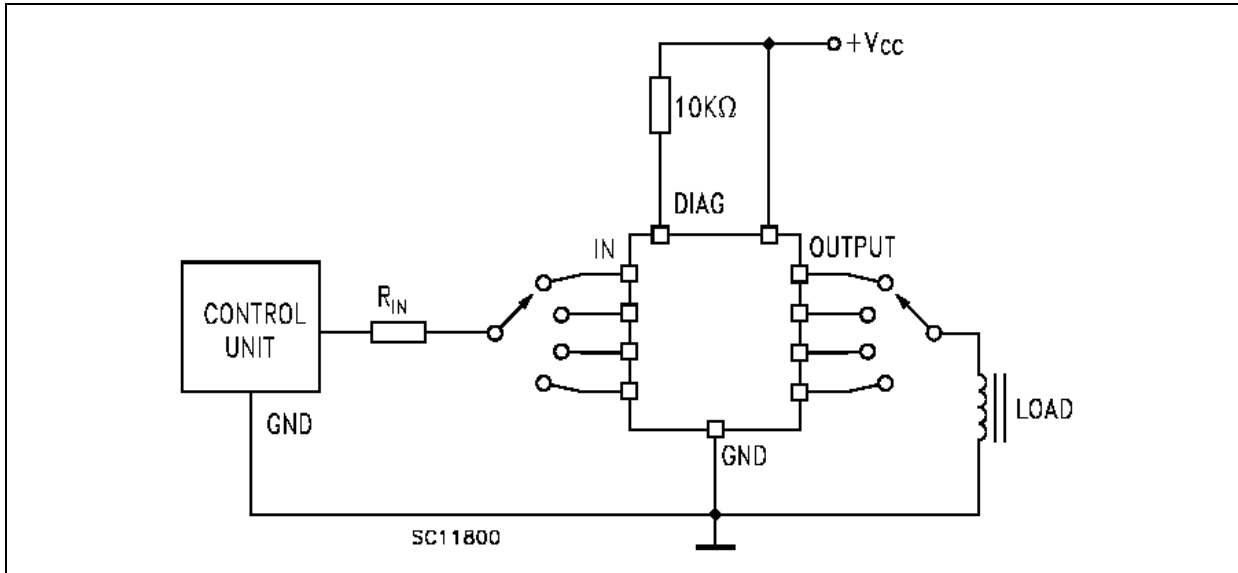
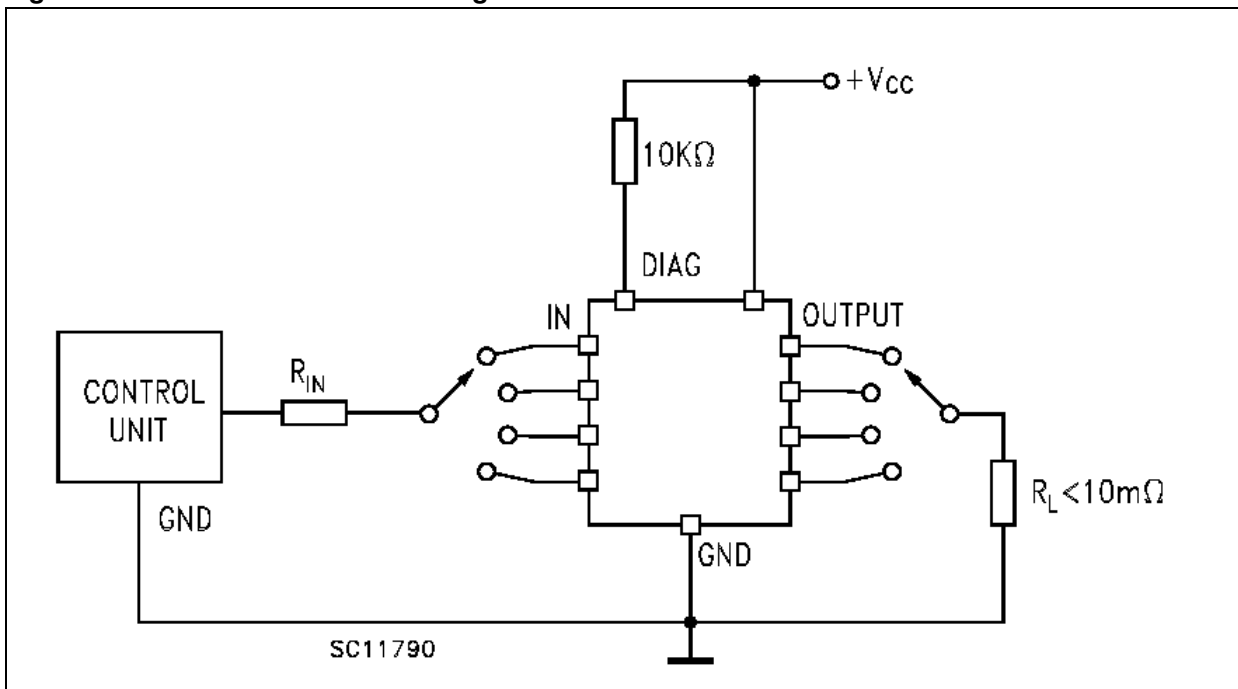


Figure 5. Peak short circuit test diagram



5 Switching time waveforms and truth table

Table 7. Truth table

	INPUTn	OUTPUTn	Diagnostic
Normal operation	L	L	H
	H	H	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	H
	H	L	H
Shorted load (Current limitation)	L	L	H
	H	H	H

Figure 6. Switching waveforms

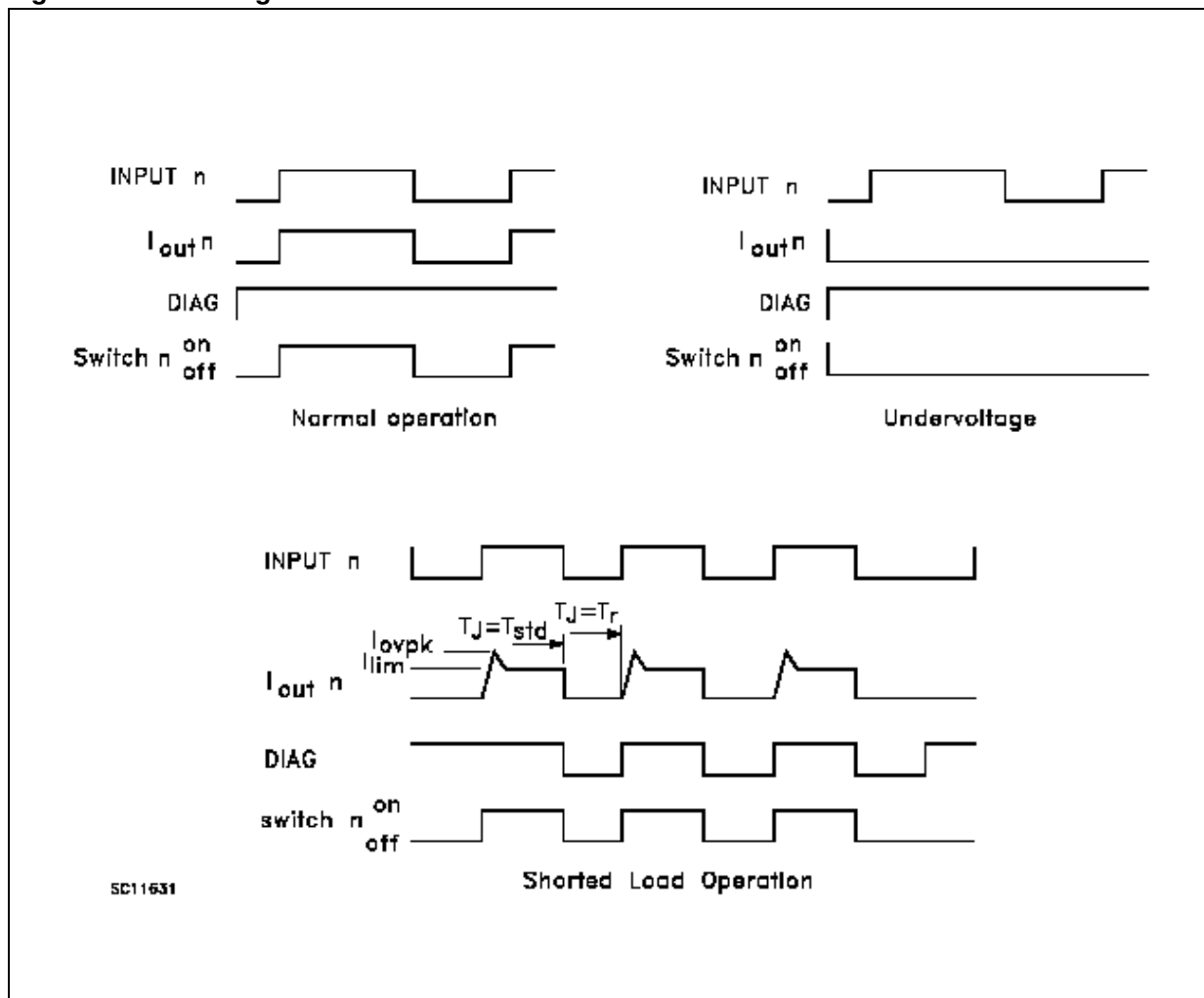


Figure 7. Switching parameter test conditions

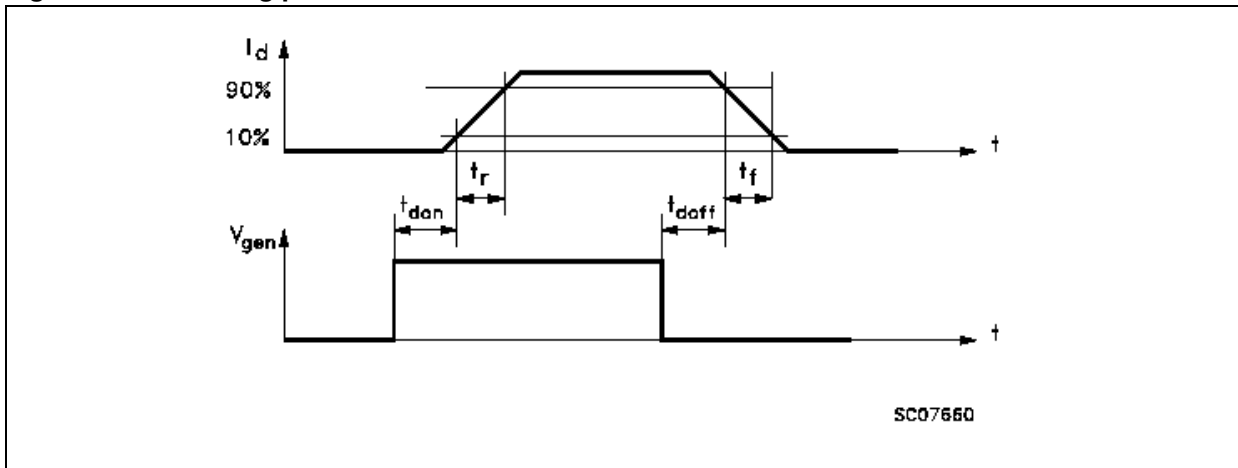
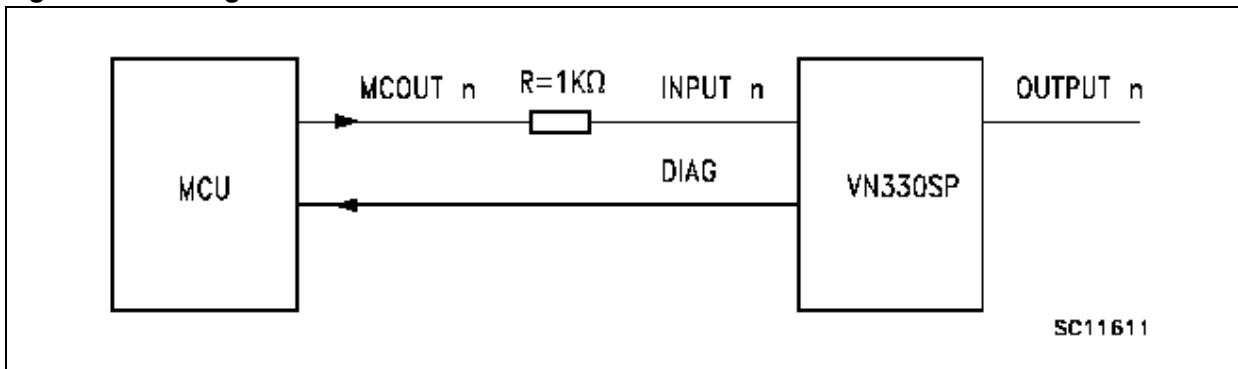


Figure 8. Driving circuit



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 8. PowerSO-10 Mechanical data

Dim	Mm			Inch		
	Min	Typ	Max	Min	Typ	Max
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.23		0.32	0.009		0.012
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
a	0°		8°			

Figure 9. Package dimension

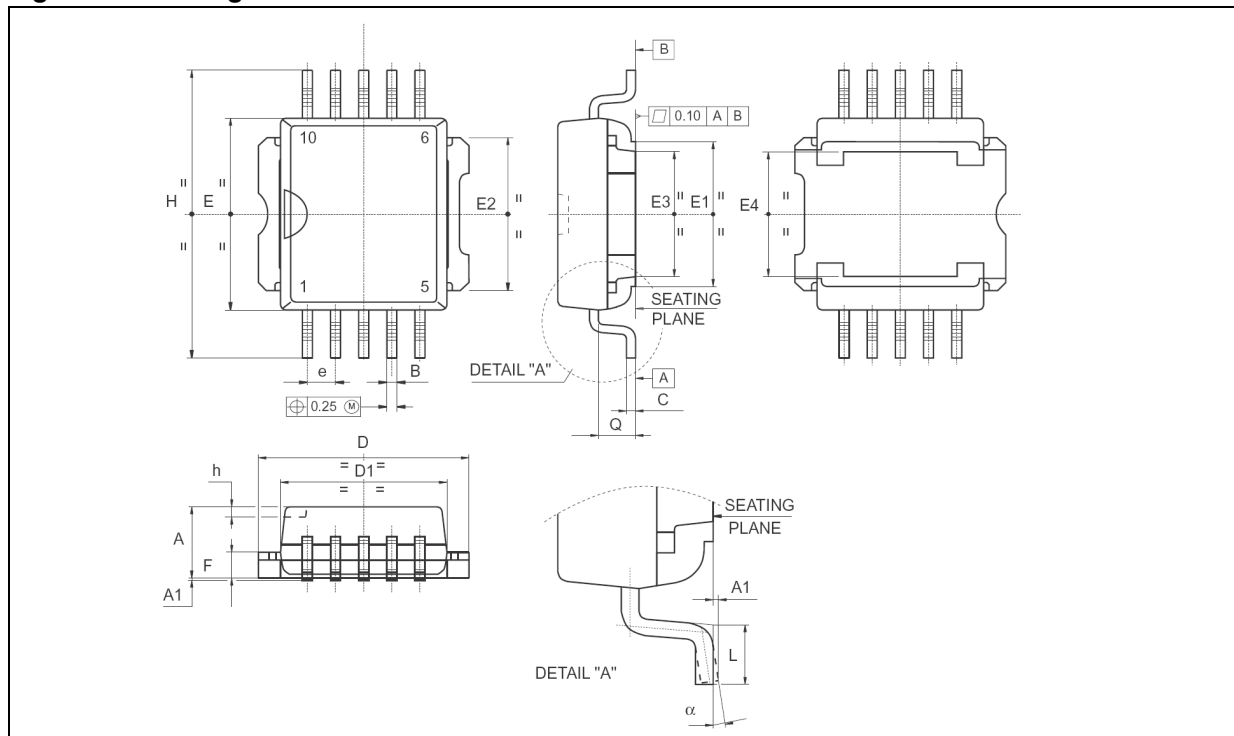


Figure 10. PowerSO-10™ Suggested Pad and Tube Shipment (No Suffix)

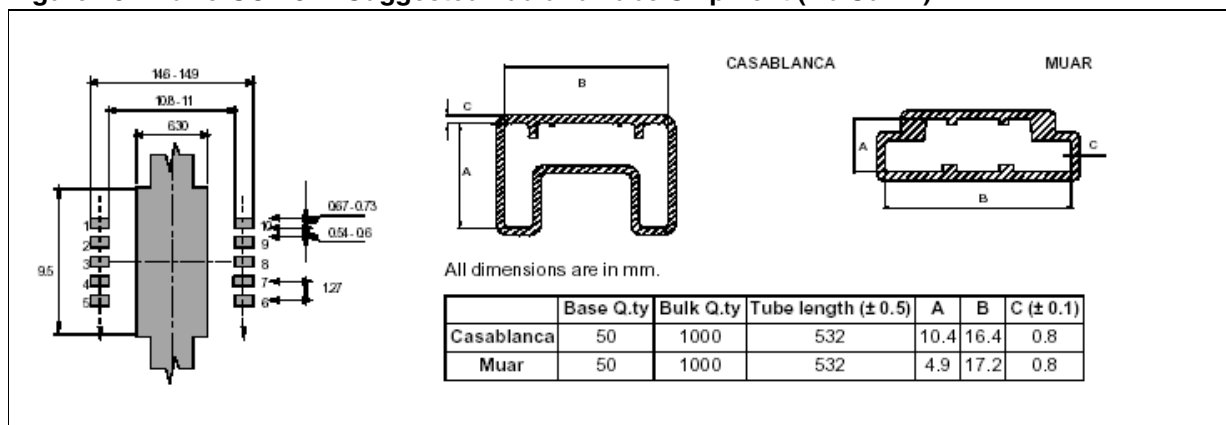
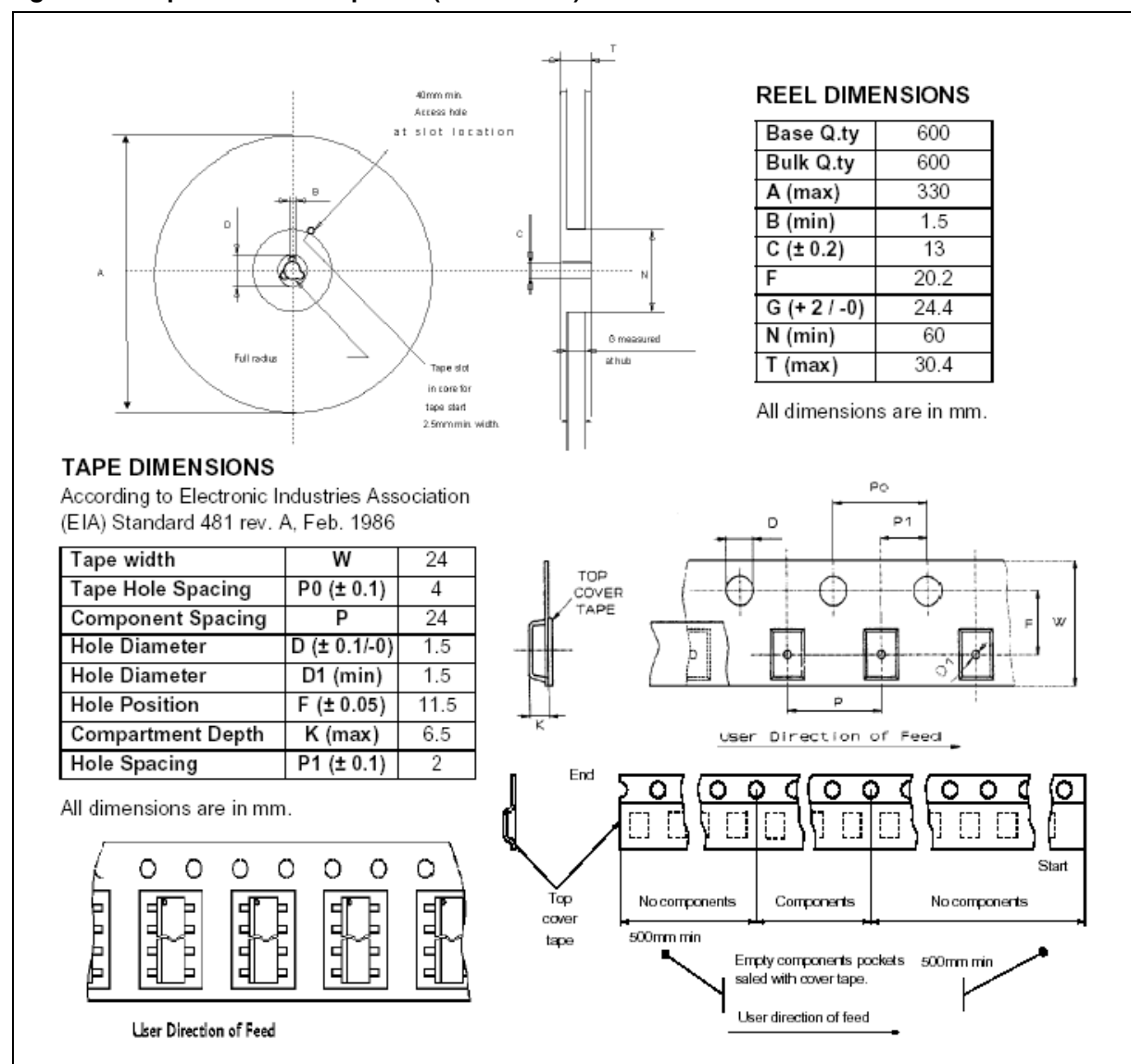


Figure 11. Tape and Reel Shipment (Suffix “TR”)



7 Order code

Table 9. Order code

Part number	Package	Packaging
VN330SP-E	PowerSO-10 TM	Tube
VN330SPTR-E	PowerSO-10 TM	Tape and reel

8 Revision history

Table 10. Revision history

Date	Revision	Changes
6-Sep-2005	1	Initial release
31-Oct-2006	2	Typo in Electrical characteristics temperature conditions updated on page 5
27-Mar-2007	3	Document reformatted, typo in Note 1 on page 6

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