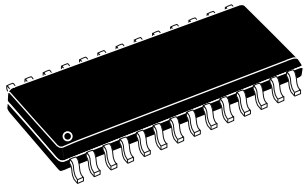
VN5772AK-E

Quad smart power solid-state relay for complete H-bridge configurations

Datasheet - production data



SO-28 (double island)

GAPG1102151005PS

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN5772AK-E	100 mΩ(1)	18 A(2)	36 V

1. Total resistance of one side in bridge configuration.
2. Typical current limitation value.

- General features
  - Inrush current management by active power limitation on the high-side switches
  - Very low standby current
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
- Protections
  - High-side drivers under voltage shutdown
  - Overvoltage clamp
  - Output current limitation
  - High and low-side overtemperature shutdown
  - Short-circuit protection
  - ESD protection
- Diagnostic functions
  - Proportional load current sense
  - Thermal shutdown indication on both the high and low-side switches

Applications

- DC motor driving in full or half-bridge configuration
- All types of resistive, inductive and capacitive loads

Description

The VN5772AK-E is a device formed by three monolithic chips housed in a standard SO-28 package: a double high-side and two low-side switches. The double high-side is made using STMicroelectronics® VIPower® M0-5 technology, while the low-side switches are fully protected VIPower M0-5 OMNIFET III. This device is suitable to drive a DC motor in a bridge configuration as well as to be used as a quad switch for any low-voltage application. The dual high-side switches integrate built-in non latching thermal shutdown with thermal hysteresis. An output current limiter protects the device in overload conditions. In the case of long overload duration, the device limits the dissipated power to a safe level-up to thermal shutdown intervention. An analog current sense pin delivers a current proportional to the load current (according to a known ratio) and indicates overtemperature shutdown of the relevant high-side switch through a voltage flag.The low-side switches have built-in non latching thermal shutdown with thermal hysteresis, linear current limitation and overvoltage clamping. In case of long overload duration, the low-side switches limit the dissipated power to a safe level up to the thermal shutdown intervention. Fault feedback for overtemperature shutdown of the low-side switch is indicated by the relevant status pin.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-28	VN5772AK-E	VN5772AKTR-E

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1 Block diagram and pin description

Figure 1. Block diagram

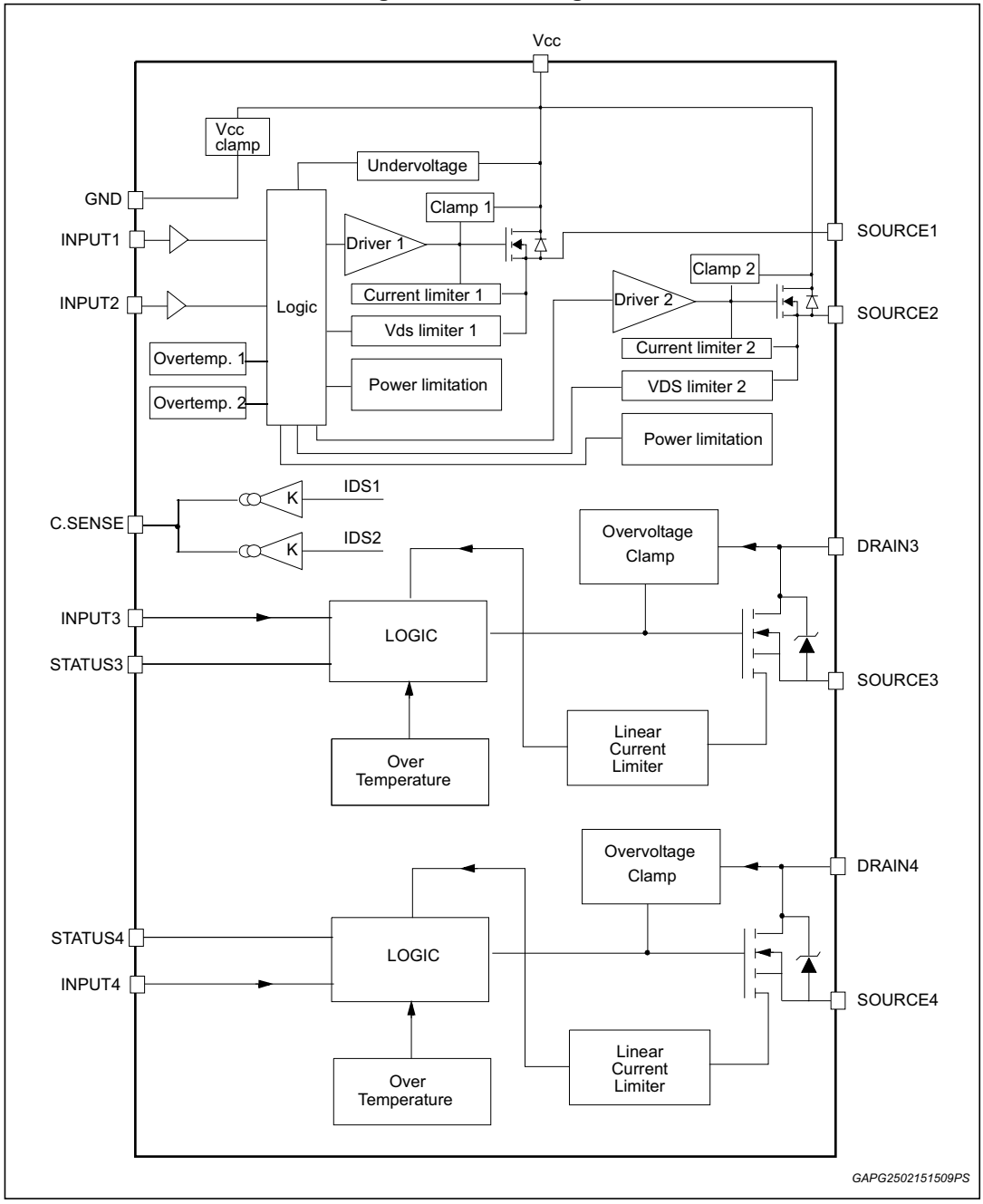
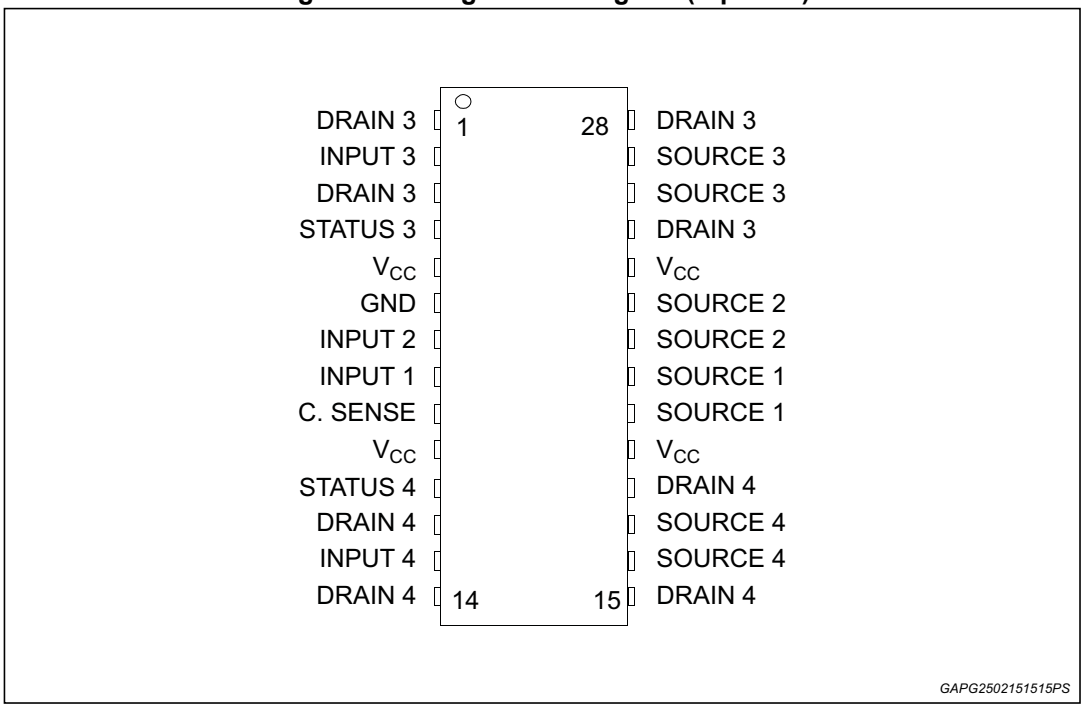


Table 2. Pin description

N° pin	Name	Function
1, 3, 25, 28	DRAIN 3	Drain of switch 3 (low-side switches)
2	INPUT 3	Input of switch 3 (low-side switch)
4	STATUS 3	Status of switch 3 (low-side switch)
11	STATUS 4	Status of switch 4 (low-side switch)
5, 10, 19, 24	V_{CC}	Drain of switches 1 and 2 (high-side switches) and power supply voltage
6	GND	Ground of switches 1 and 2 (high-side switches)
8	INPUT 1	Input of switch 1 (high-side switch)
7	INPUT 2	Input of switch 2 (high-side switch)
9	C.SENSE	Analog current sense pin, delivers a current proportional to the load current
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switches)
13	INPUT 4	Input of switch 4 (low-side switch)
16, 17	SOURCE 4	Source of switch 4 (low-side switches)
22, 23	SOURCE 2	Source of switch 2 (high-side switches)
20, 21	SOURCE 1	Source of switch 1 (high-side switches)
26, 27	SOURCE 3	Source of switch 3 (low-side switches)

Figure 2. Configuration diagram (top view)



2 Electrical specification

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the tables below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 3. Dual high-side switch

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$- I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$- I_{OUT}$	Reverse DC output current	-12	A
I_{IN}	DC input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse C.SENSE pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) (L = 3 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_{OUT} = I_{limL}*(Typ.)*)	104	mJ
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF) – Input – Current sense – $SOURCE_n/DRAIN_n$ – V_{CC}	 4000 2000 5000 5000	 V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

Table 4. Low side switch

Symbol	Parameter	Value	Unit
V_{DSn}	Drain-source voltage (V_{INn} = 0 V)	Internally clamped	V
I_{INn}	Input current	-1 to 10	mA
I_{Dn}	Drain current	Internally limited	A
$-I_{Dn}$	Reverse DC output current	-4	A
I_{STAT}	DC status current	-1 to 10	mA
V_{ESD1}	Electrostatic discharge (R = 1.5 KΩ, C = 100 pF): – Drain – Supply, status, input	 5000 4000	V
V_{ESD2}	Electrostatic discharge on output pins only (R = 330 Ω, C = 150 pF)	2000	V
T_j	Operating junction-temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}leadHS}$	Thermal resistance junction-case (high-side switch)	22	°C/W
$R_{thj\text{-}leadLS}$	Thermal resistance junction-case (low-side switch)	21	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (high-side switch)	47	°C/W
	Thermal resistance junction-ambient (low-side switch)	57	°C/W

2.3 Electrical characteristics

2.3.1 Electrical characteristics for dual high-side switches

Values specified in this section are for 8 V < V_{CC} < 36 V; -40 °C < T_j < 150 °C, unless otherwise specified (for each channel).

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	I_{OUT} = 3 A; T_j = 25 °C			50	mΩ
		I_{OUT} = 3 A; T_j = 150 °C			100	
		I_{OUT} = 3 A; V_{CC} = 5 V; T_j = 25 °C			65	
V_{clamp}	Voltage clamp	I_S = 20 mA	41	46	52	V
I_S	Supply current	Off-state: V_{CC} = 13 V; T_j = 25 °C, V_{IN} = V_{OUT} = V_{SENSE} = 0 V		2(1)	5(1)	µA
		On-state: V_{CC} = 13 V; V_{IN} = 5 V, I_{OUT} = 0 A		3	6	mA
$I_{L(off)}$	Off-state output current(2)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V, T_j = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V, T_j = 125 °C	0		5	
V_F	Output - V_{CC} diode voltage(2)	I_{OUT} = 3A, T_j = 150 °C			0.7	V

1. PowerMOS leakage included.
2. For each channel.

Table 7. Switching (V_{CC} = 13 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 6.5 Ω (see *Figure 4*)	—	25	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 6.5 Ω (see *Figure 4*)	—	20	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 6.5 Ω	—	See *Figure 15*	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 6.5 Ω	—	See *Figure 17*	—	V/µs

Table 7. Switching (V_{CC} = 13 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
W_{ON}	Switching energy losses during t_{won}	R_L = 6.5 Ω (see *Figure 4*)	—	0.24	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 6.5 Ω (see *Figure 4*)	—	0.2	—	mJ

Table 8. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input voltage hysteresis		0.25			V
V_{ICL}	Input voltage clamp	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		

Table 9. Protection and diagnostics

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	V_{CC} = 13 V	12	18	24	A
		5 V < V_{CC} < 36 V			24	A
I_{limL}	Short-circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		7		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.1 A, T_j = -40 °C to 150 °C (see *Figure 5*)		25		mV

1. To ensure long-term reliability under heavy overload or short-circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8 V < V_{CC} < 16 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT} / I_{SENSE}	I_{OUT} = 0.35 A; V_{SENSE} = 0.5 V; T_j = -40 °C to 50 °C	1430	2140	2890	
K_1	I_{OUT} / I_{SENSE}	I_{OUT} = 1 A; V_{SENSE} = 0.5 V; T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	1470 1570	2020 2020	2610 2470	
K_2	I_{OUT} / I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 4 V; T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	1740 1790	2020 2020	2320 2250	
K_3	I_{OUT} / I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	1890 1890	2010 2010	2140 2140	
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 4 A;	5			V
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{IN} = 0 V, T_j = -40 °C to 150 °C	0		1	µA
		I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{IN} = 5 V, T_j = -40 °C to 150 °C	0		2	
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC} = 13 V, R_{SENSE} = 10 KΩ		9		V
I_{SENSEH}	Analog sense output current in overtemperature condition	V_{CC} = 13 V, V_{SENSE} = 5 V		8		mA
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 4 A, I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 3*)		80	250	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 4 A, I_{SENSE} = 10% of $I_{SENSE\ max}$ (see *Figure 3*)		100	250	µs

Figure 3. Current sense delay characteristics

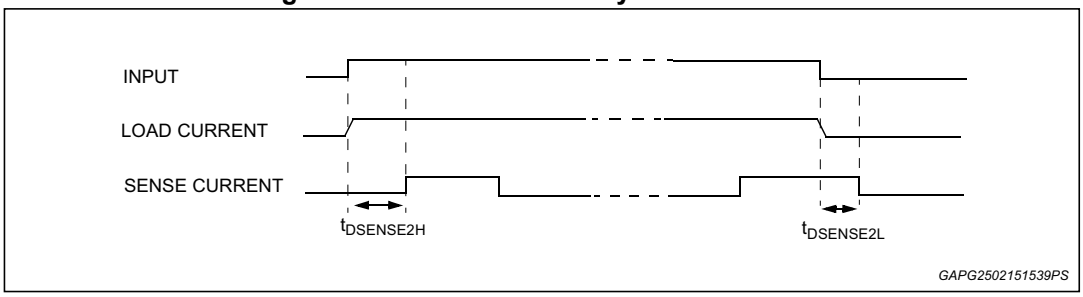


Figure 4. Switching time waveforms

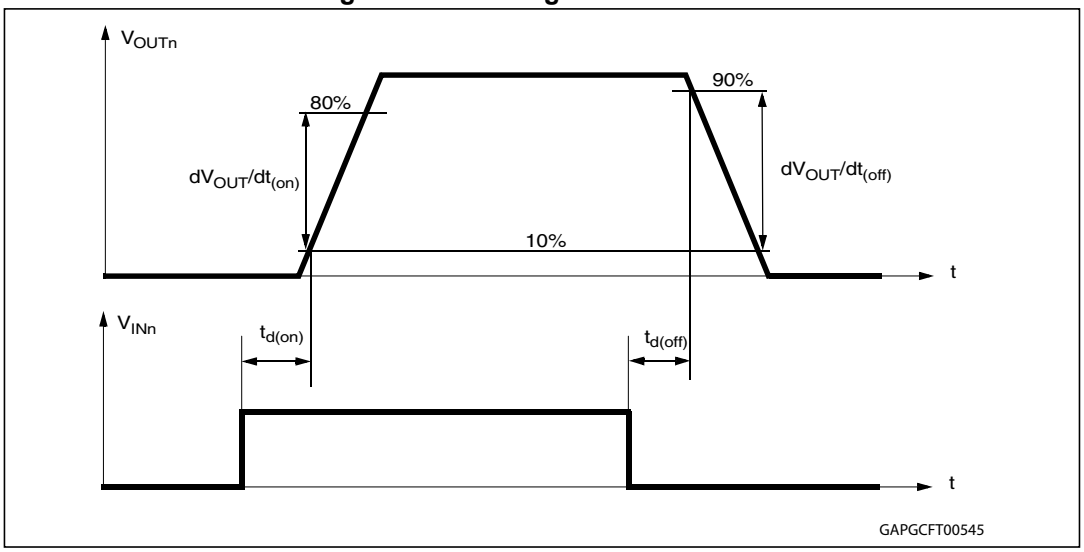


Figure 5. Output voltage drop limitation

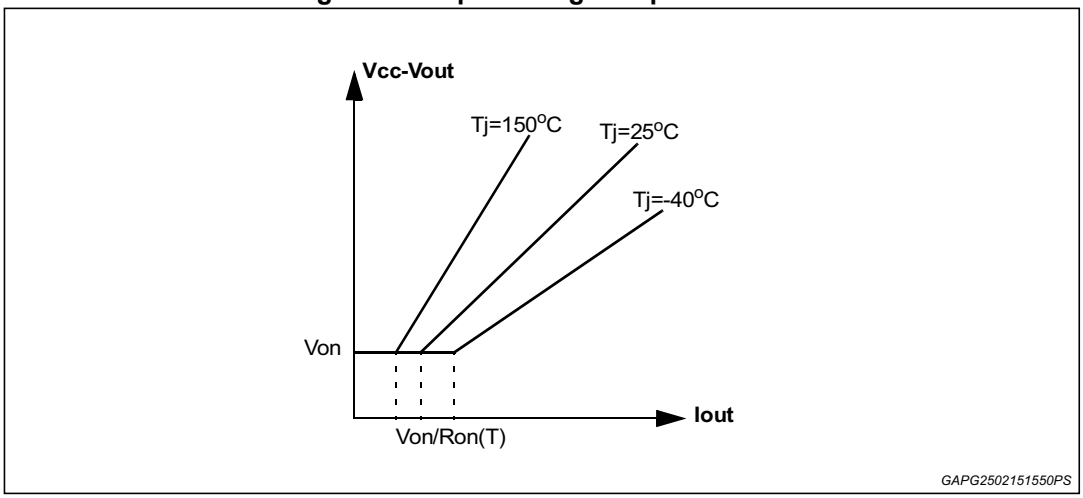


Table 11. Truth table high-side driver

Conditions	Input	Output	Sense
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Short-circuit to GND ($R_{SC} \leq 10$ mΩ)	L H H	L L L	0 0 if $T_j < T_{TSD}$ V_{SENSEH} if $T_j > T_{TSD}$
Short-circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) test pulse	Test levels (1)		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and Impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50µs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1µs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1µs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b(2)	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Note: Valid for HSD and H-bridge configuration.

Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004E test pulse	Test level results(1)	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Electrical characteristics curves for dual high-side switches

Figure 6. Off-state output current

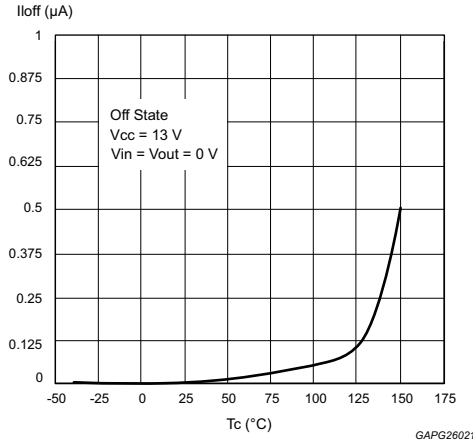


Figure 7. High-level input current

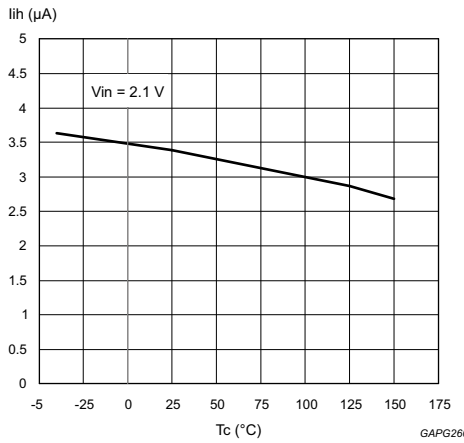


Figure 8. Input voltage clamp

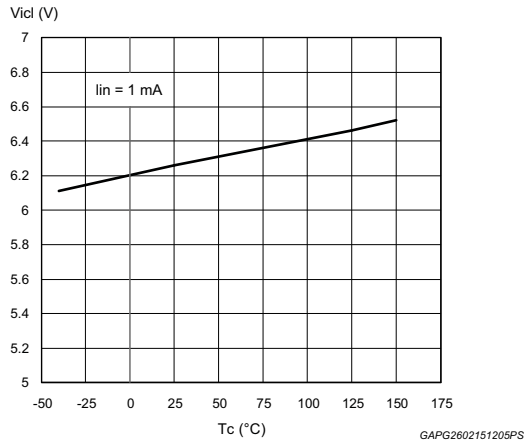


Figure 9. Low level input voltage

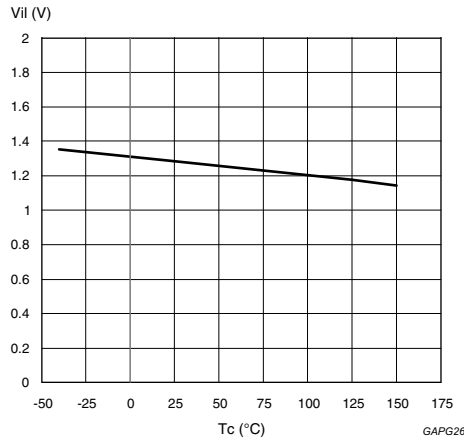


Figure 10. High-level input voltage

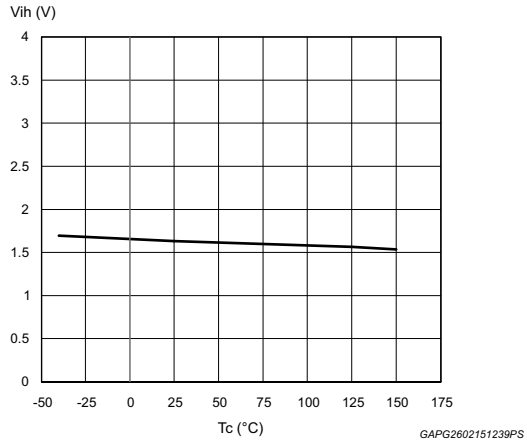


Figure 11. Input voltage hysteresis

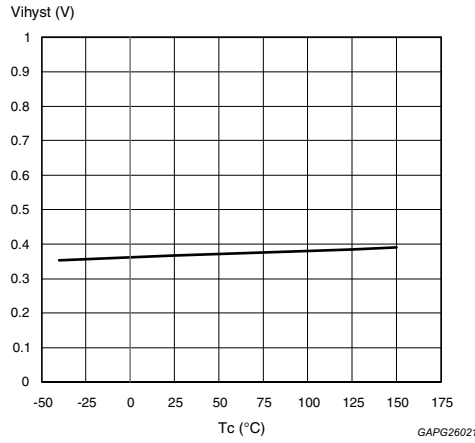


Figure 12. On-state resistance vs T_{case}

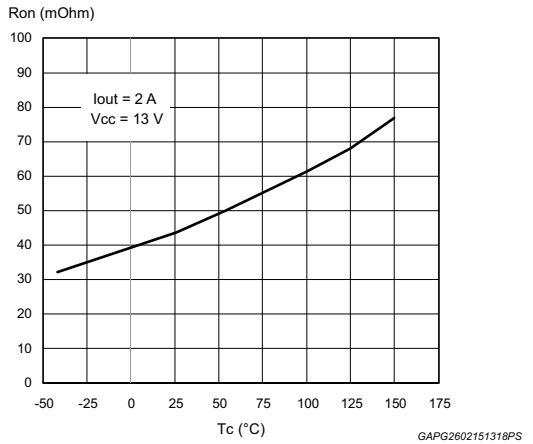


Figure 13. On-state resistance vs V_{CC}

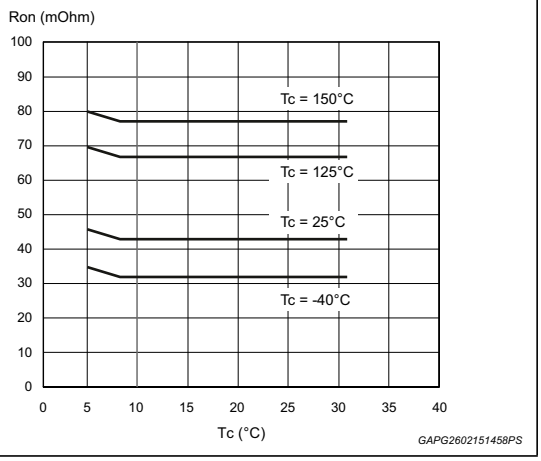


Figure 14. Undervoltage shutdown

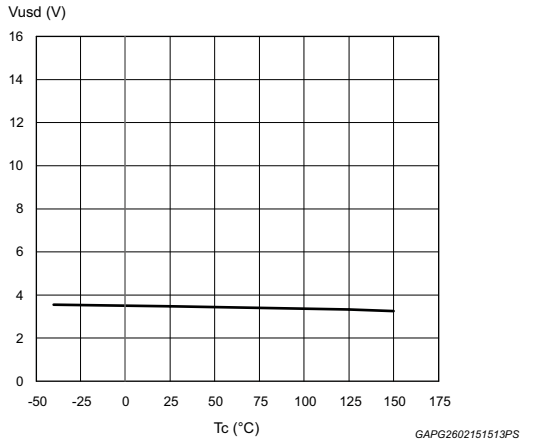


Figure 15. Turn-on voltage slope

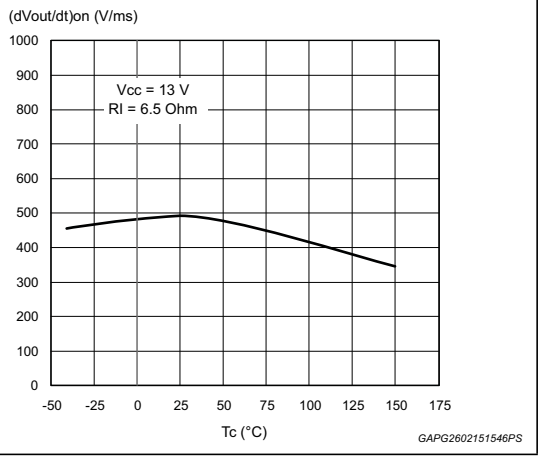


Figure 16. I_{LIMH} vs T_{case}

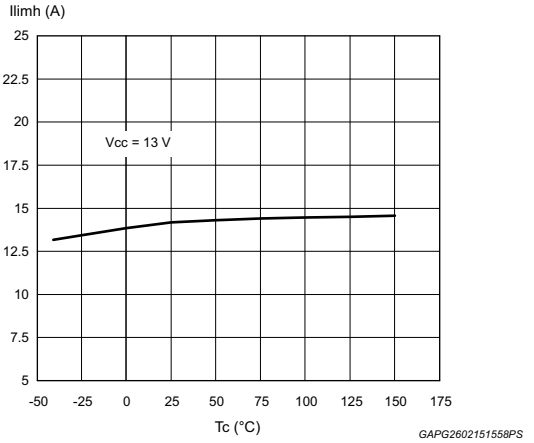
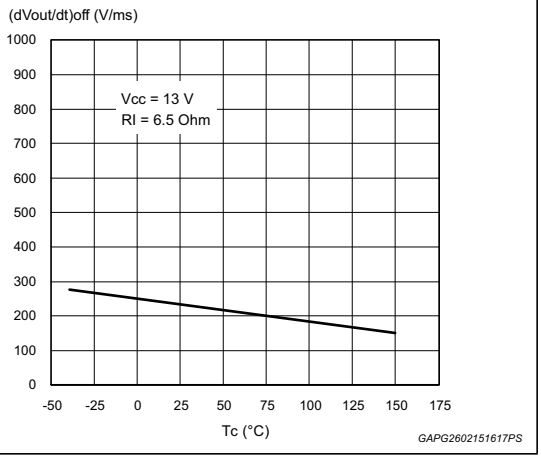


Figure 17. Turn-off voltage slope



2.5 Electrical characteristics for low-side switch

Values specified in this section are for -40 °C < T_j < 150 °C, unless otherwise specified

Table 15. PowerMOS section - off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Drain-source voltage clamp	V_{IN} = 0 V; I_D = 2 A	41	46	52	V
V_{CLTH}	Drain-source threshold voltage clamp	V_{IN} = 0 V; I_D = 2 mA	36			V
I_{DSS}	Zero input voltage Drain current (V_{IN} = 0 V)	V_{DS} = 13 V; V_{IN} = 0 V; T_j = 25°C	0		3	µA
		V_{DS} = 13 V; V_{IN} = 0 V; T_j = 125°C	0		5	

Table 16. PowerMOS section - on

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on-resistance	V_{IN} = 5 V; I_D = 2 A; T_j = 25 °C	—	—	50	mΩ
		V_{IN} = 5 V; I_D = 2 A; T_j = 150 °C	—	—	100	mΩ

Table 17. Switching (T_j = 25° C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 6.5 Ω; V_{CC} = 13 V	—	6	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 6.5 Ω; V_{CC} = 13 V	—	20	—	µs
t_r	Turn-on voltage slope	R_L = 6.5 Ω; V_{CC} = 13 V	—	10	—	µs
t_f	Turn-off voltage slope	R_L = 6.5 Ω; V_{CC} = 13 V	—	10	—	µs
W_{ON}	Switching energy losses during t_{won}	R_L = 6.5 Ω; V_{CC} = 13 V	—	0.04	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 6.5 Ω; V_{CC} = 13 V	—	0.06	—	mJ

Table 18. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 2 A; V_{IN} = 0 V	—	0.8	—	V

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 19. Input section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ISS}	Supply current from input pin	On-state: V_{IN} = 5 V; V_{DS} = 0 V		30	110	µA

Table 19. Input section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ICL}	Input voltage clamp	I_S = 1 mA	5.5		7	V
		I_S = -1 mA		-0.7		
V_{INTH}	Input voltage threshold	$V_{DS} = V_{IN}$; I_D = 1 mA	1		3.5	V

Table 20. STATUS pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation, V_{STAT} = 5 V			10	µA
C_{STAT}	STATUS pin input capacitance	Normal operation, V_{STAT} = 5 V			100	pF
V_{STCL}	Status voltage clamp	I_{STAT} = 1 mA	5.5		7	V
		I_{STAT} = -1 mA		-0.7		

Table 21. Protection and diagnostics (-40 °C < T_j < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	V_{DS} = 13 V, V_{IN} = 5 V	19	27	38	A
I_{limL}	Short-circuit current during thermal cycling	V_{DS} = 13 V, $T_R < T_j < T_{TSD}$		11		A
t_{dlim}	Step response current limit	V_{IN} = 5 V, V_{DS} = 13 V		20		µs
T_{TSD}	Overtemperature shutdown		150	175	200	°C
T_R	Overtemperature reset		135			°C

Table 22. Truth table low-side driver

Conditions	Input	Drain	Status
Normal operation	L	H	H
	H	L	H
Overtemperature	L	H	H
	H	H	L

2.6 Electrical characteristics curves for low-side switch

Figure 18. Source diode forward characteristics

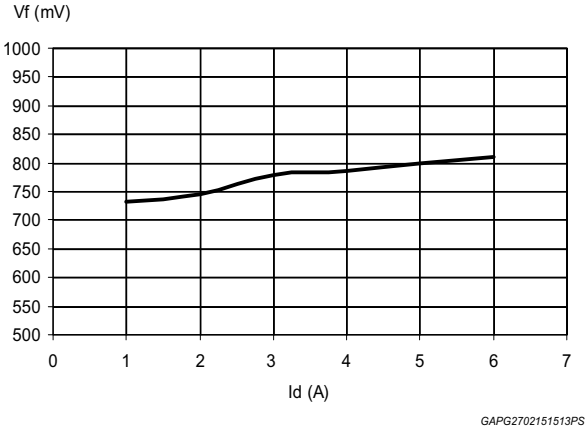


Figure 19. Static drain source on-resistance vs drain current (3 pin)

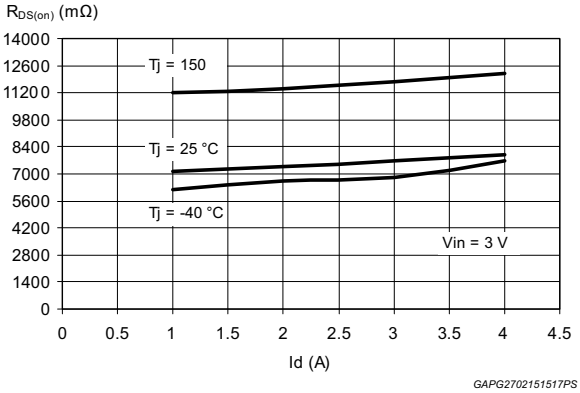


Figure 20. Static drain source on-resistance vs input voltage (3 pin)

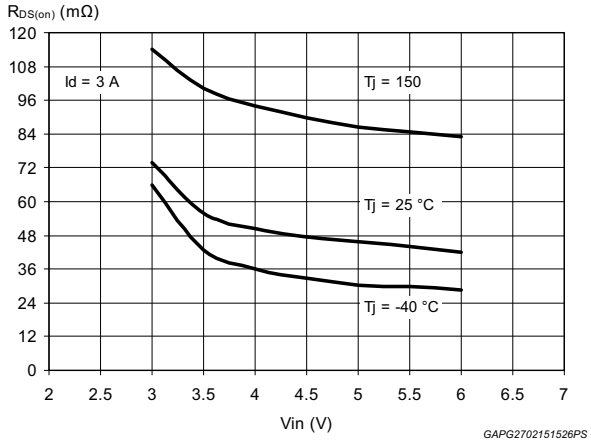
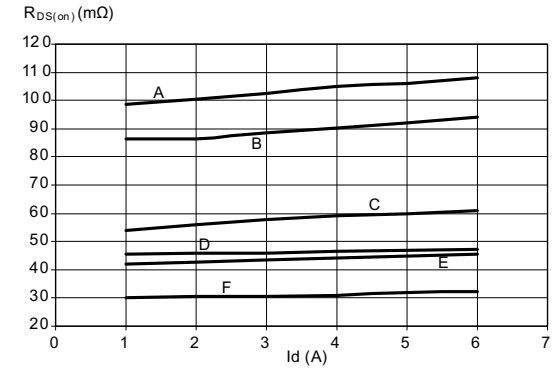
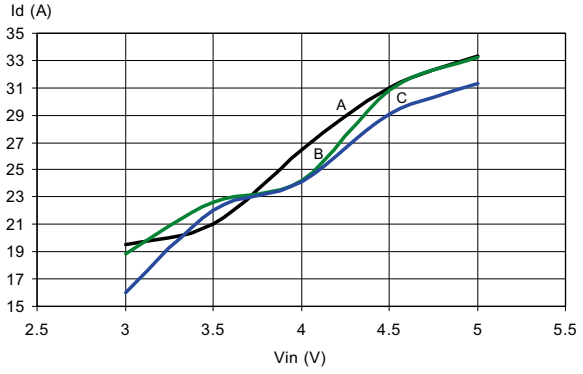


Figure 21. Static drain source on-resistance vs drain current



A : Vin = 3.5 V, Tj = 150 °C
B : Vin = 5 V, Tj = 150 °C
C : Vin = 3.5 V, Tj = 25 °C
D : Vin = 5 V, Tj = 25 °C
E : Vin = 3.5 V, Tj = -40 °C
F : Vin = 5 V, Tj = -40 °C

Figure 22. Transfer characteristics



A: Tj = -40 °C B: Tj = 25 °C C: Tj = 150 °C

Figure 23. Output characteristics

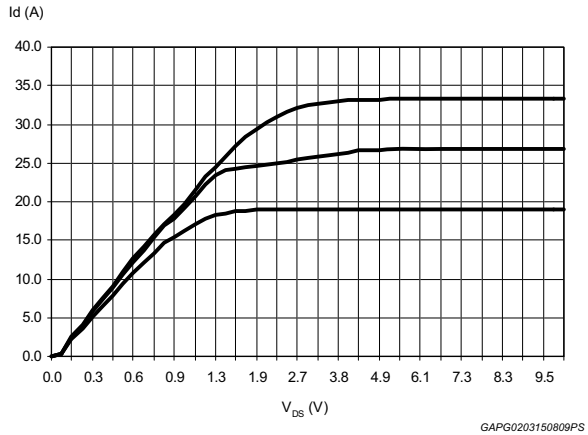


Figure 24. Normalized on-resistance vs temperature

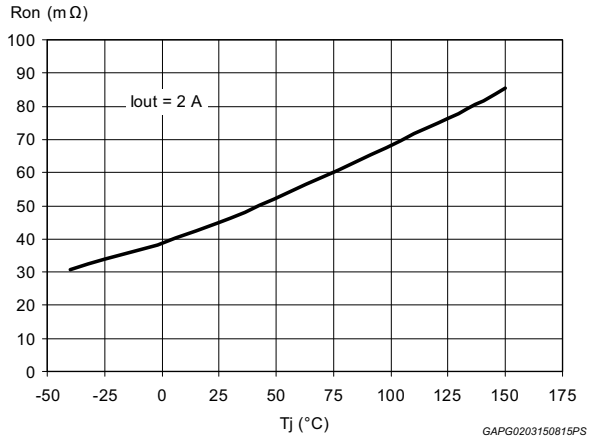
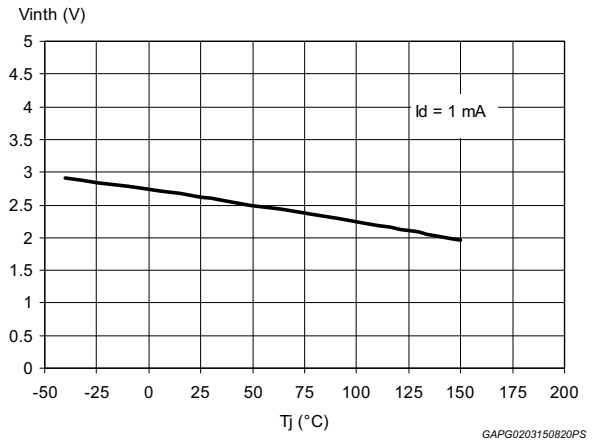
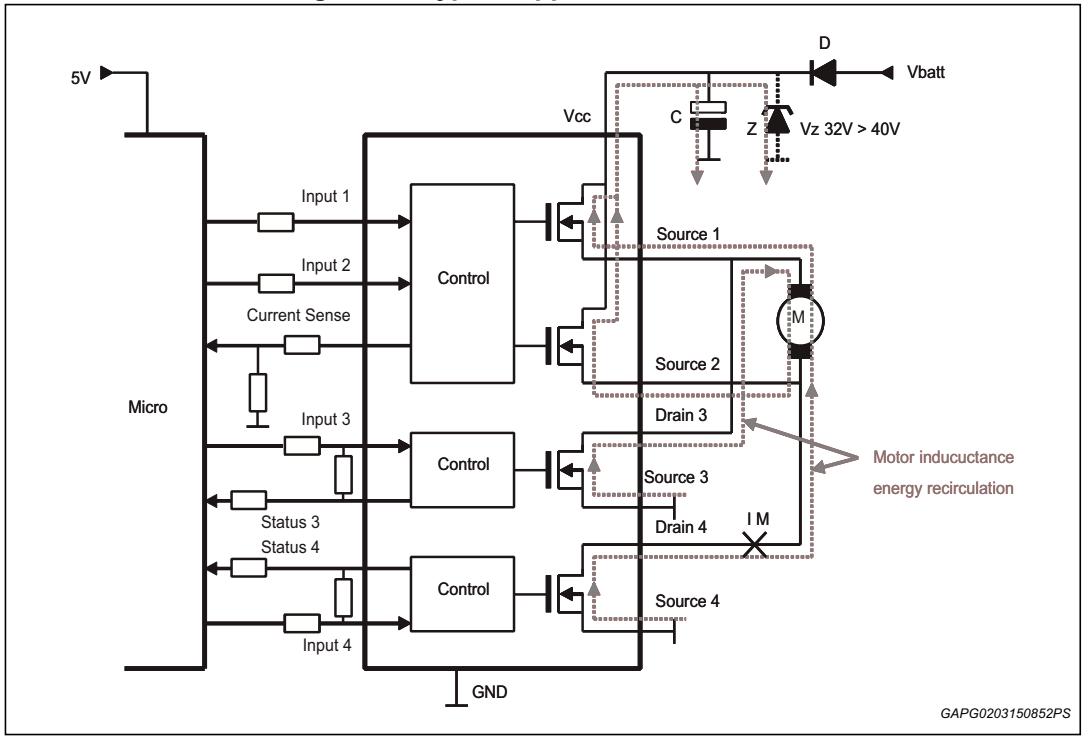


Figure 25. Normalized input threshold vs temperature



3 Application information

Figure 26. Typical application schematic



Mostly motor bridge drivers use a reverse battery protection diode (D) inside supply rail. This diode prevents a reverse current flow back to Vbatt in case the bridge gets disabled via the logic inputs while motor inductance still carries energy. In order to prevent a hazardous overvoltage at circuit supply terminal (V_{CC}), a blocking capacitor (C) is needed to limit the voltage overshoot. As basic orientation, 50 µF per 1 A load current is recommended. In alternative, also a Zener protection (Z) is suitable.

Even if a reverse polarity diode is not present, it is recommended to use a capacitor or zener at V_{CC} because a similar problem appears in case supply terminal of the module has intermittent electrical contact to the battery or gets disconnected while motor is operating.

Figure 27. Recommended motor operation

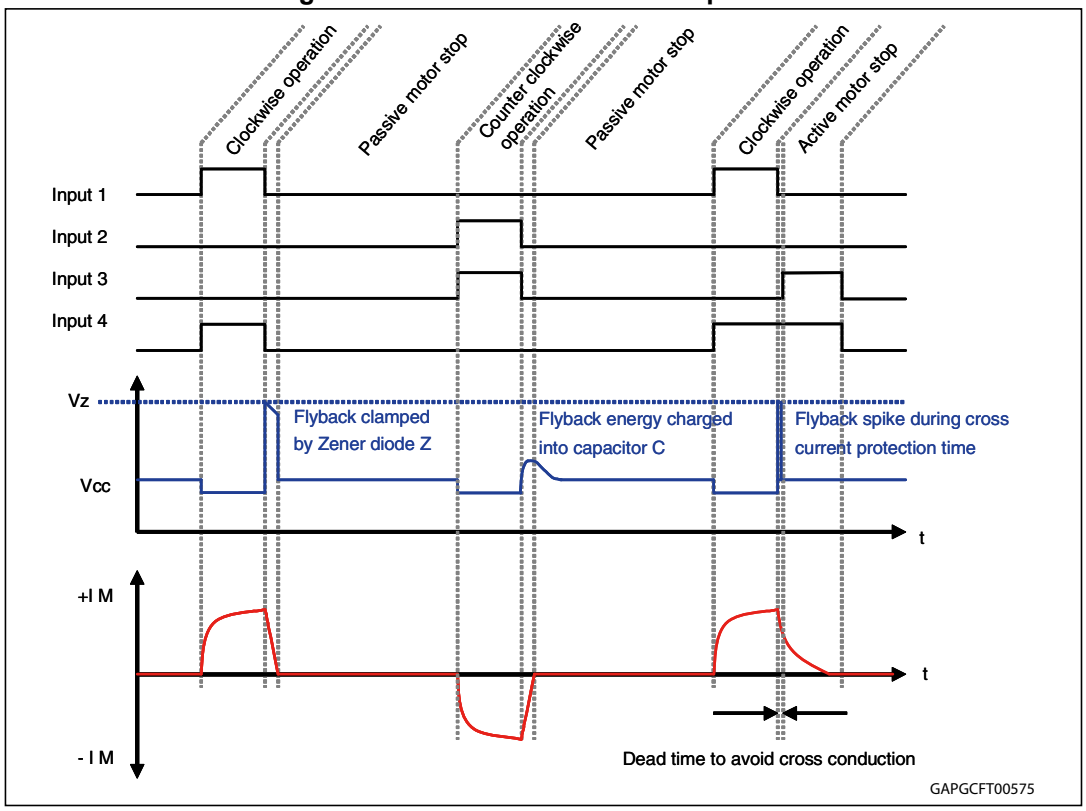
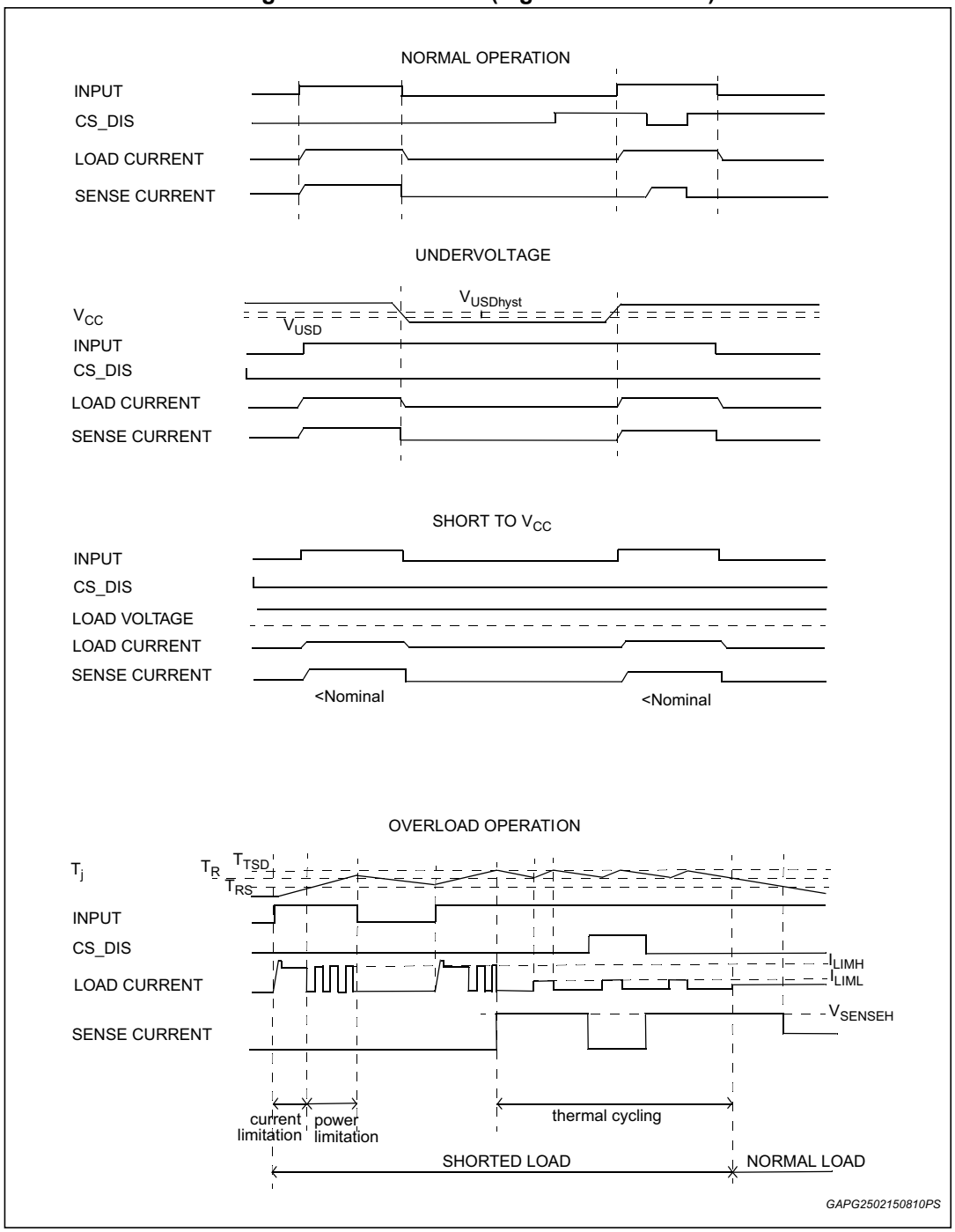
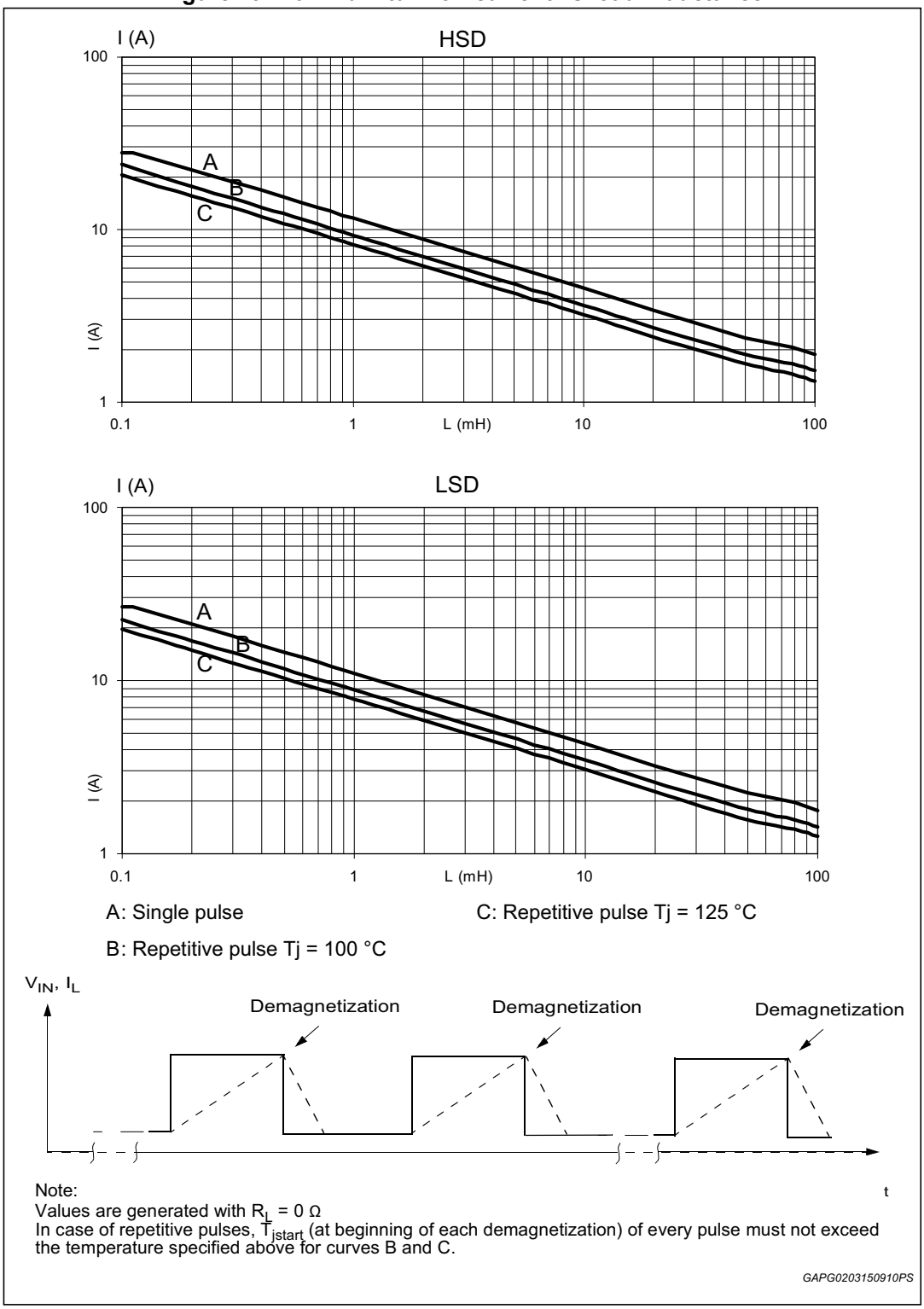


Figure 28. Waveforms (high-side switches)



3.1 Maximum demagnetization energy (V_{CC} = 13.5 V)

Figure 29. Maximum turn-off current vs load inductance



Note:
Values are generated with R_L = 0 Ω
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

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4 Package and PC board thermal data

4.1 SO-28 thermal data

Figure 30. SO-28 PC board

Note:
Layout condition of Rth and Zth measurements (Board finish thickness 1.6 mm +/- 10%; Board double layers; Board dimension 77x86; Board Material FR4; Cu thickness 0.070mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm).

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Figure 31. Chipset configuration

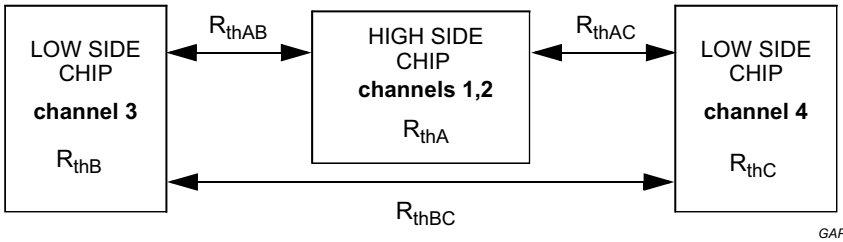

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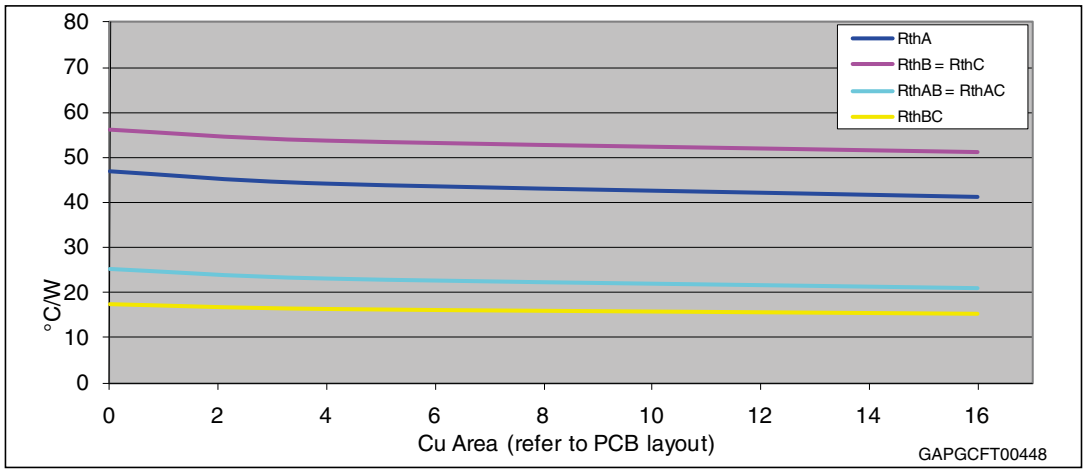
Figure 32. Auto and mutual Rthj-amb vs PCB copper area in open box free air condition



Note: See Figure 31. For more detailed information see Table 24 and Table 25.

Table 23. Thermal calculations in clockwise and anti-clockwise operation in steady-state mode

HS_1	HS_2	LS_3	LS_4	T_{jHS12}	T_{jLS3}	T_{jLS4}
On	Off	Off	On	$P_{dHS1} \times R_{thHS} + P_{dLS4} \times R_{thHSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLS} + T_{amb}$
Off	On	On	Off	$P_{dHS2} \times R_{thHS} + P_{dLS3} \times R_{thHSLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLSLS} + T_{amb}$

Table 24. Thermal resistances definitions

Parameter	Definition[1]
$\mathbf{R_{thHS}} = R_{thHS1} = R_{thHS2}$	High-side chip thermal resistance junction-to-ambient (HS_1 or HS_2 in on-state)
$\mathbf{R_{thLS}} = R_{thLS3} = R_{thLS4}$	Low-side chip thermal resistance junction-to-ambient
$\mathbf{R_{thHSLS}} = R_{thHS1LS4} = R_{thHS2LS3}$	Mutual thermal resistance junction-to-ambient between high-side and low-side chips
$\mathbf{R_{thLSLS}} = R_{thLS3LS4}$	Mutual thermal resistance junction-to-ambient between low-side chips

1. Values dependent on PCB heatsink area.

Table 25. Single pulse thermal impedance definitions

Parameter	Definition [1]
Z_{thHS}	High-side chip thermal impedance junction-to-ambient
$Z_{thLS} = Z_{thLS3} = Z_{thLS4}$	Low-side chip thermal impedance junction-to-ambient
$Z_{thHSLS} = Z_{thHS12LS3} = Z_{thHS12LS4}$	Mutual thermal impedance junction-to-ambient between high-side and low-side chips
$Z_{thLSLS} = Z_{thLS3LS4}$	Mutual thermal impedance junction-to-ambient between low-side chips

1. Values dependent on PCB heatsink area.

Table 26. Thermal calculations in transient mode

Parameter	Definition(1)
T_{jHS12}	$Z_{thHS} \times P_{dHS12} + Z_{thHSLS} \times (P_{dLS3} + P_{dLS4}) + T_{amb}$
T_{jLS3}	$Z_{thHSLS} \times P_{dHS12} + Z_{thLS} \times P_{dLS3} + Z_{thLSLS} \times P_{dLS4} + T_{amb}$
T_{jLS4}	$Z_{thHSLS} \times P_{dHS12} + Z_{thLSLS} \times P_{dLS3} + Z_{thLS} \times P_{dLS4} + T_{amb}$

1. Calculation is valid in any dynamic operating condition. Pd values set by user.

Figure 33. SO-28 HSD thermal impedance junction-ambient single pulse

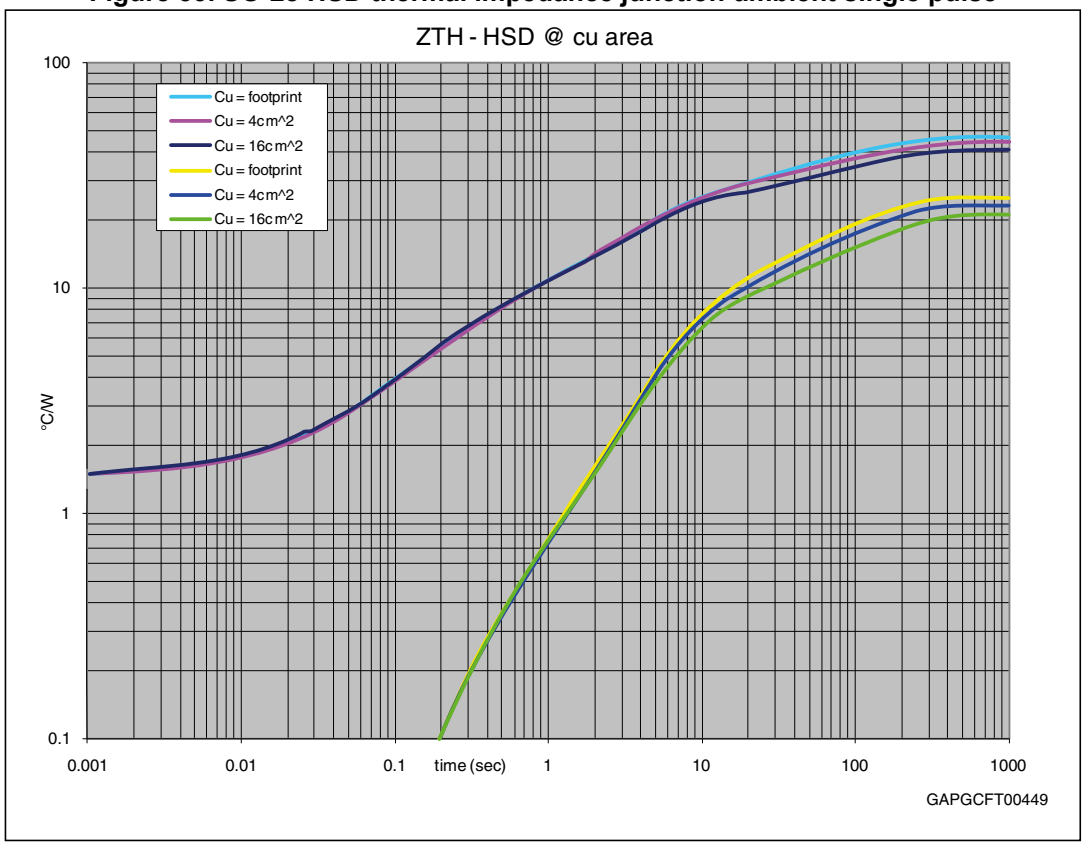
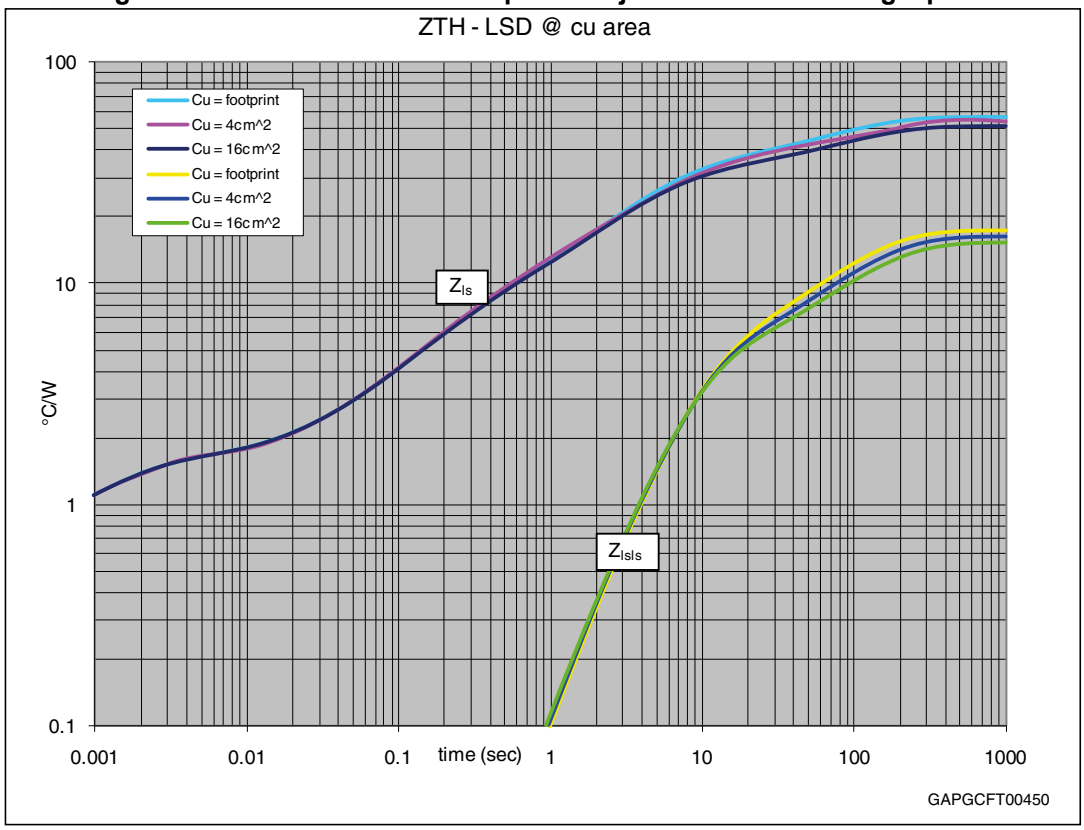


Figure 34. SO-28 LSD thermal impedance junction-ambient single pulse



Equation 1: Pulse Calculation Formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 35. Thermal fitting model of an H-bridge in SO-28

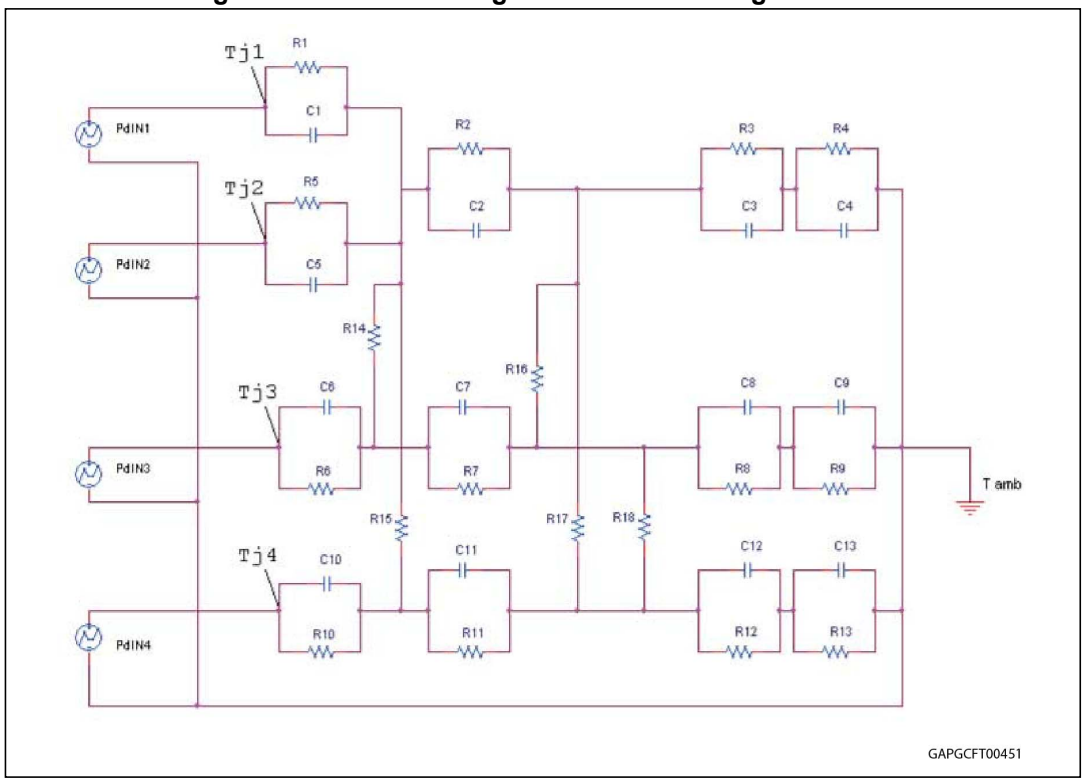


Table 27. Thermal parameters

Area/island (cm^2)	FP	4(1)	16(1)
R1 = R5 = R6 = R10 (°C/W)	1.5		
R2 = R7 = R11 (°C/W)	5.5		
R3 (°C/W)	36	34	32
R4 (°C/W)	50	43	36
R8 = R12 (°C/W)	40	38	36
R9 = R13 (°C/W)	54	52	50
R14 = R15 (°C/W)	120		
R16 = R17 (°C/W)	200		
R18 (°C/W)	400	350	300
C1 = C5 (W·s/°C)	0.00025		
C2 = C7 = C11 (W·s/°C)	0.04		
C3 (W·s/°C)	0.2		
C4 (W·s/°C)	2.2	3	4
C6 = C10 (W·s/°C)	0.00075		
C8 = C12 (W·s/°C)	0.15		
C9 = C13 (W·s/°C)	1.6	1.8	2

1. A blank space means that the value is the same as the previous one

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 SO-28 package mechanical data

Figure 36. SO-28 package outline

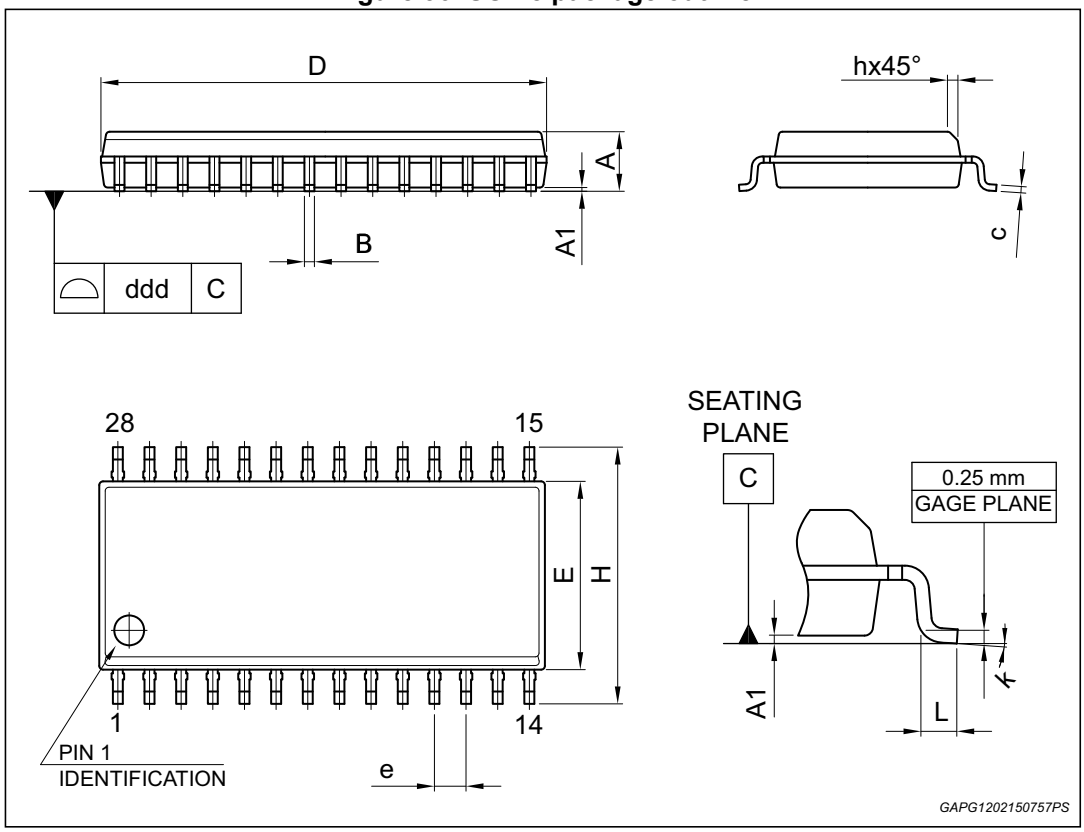


Table 28. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D(1)	17.70		18.10

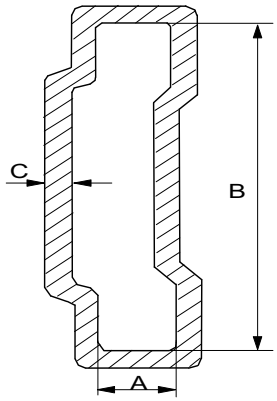
Table 28. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

1. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

5.2 Packing information

Figure 37. SO-28 tube shipment (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

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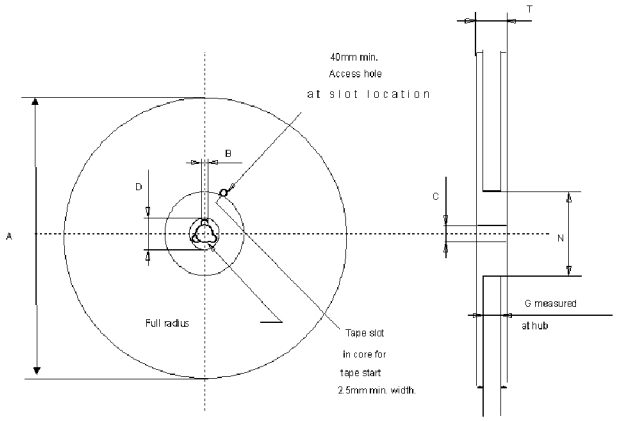
Figure 38. SO-28 tape and reel shipment (suffix "TR")



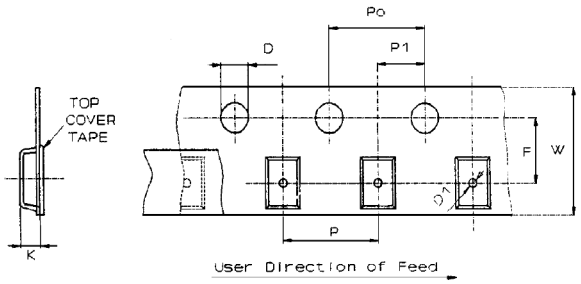
Reel dimensions

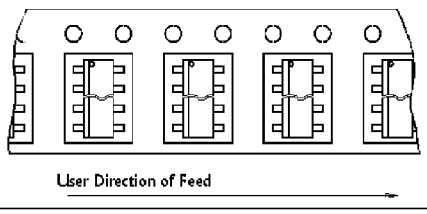
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

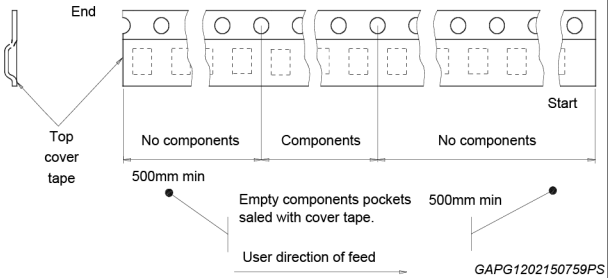
Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Description	Dimensions	mm
Tape width	W (± 0.3)	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	12
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	3.1
Hole Spacing	P1 (± 0.1)	2







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6 Revision history

Table 29. Document revision history

Date	Revision	Changes
30-Jul-2009	1	Initial release.
10-Sep-2009	2	Updated following figures: – *Figure 29: Maximum turn-off current vs load inductance* – *Figure 32: Auto and mutual Rthj-amb vs PCB copper area in open box free air condition* – *Figure 33: SO-28 HSD thermal impedance junction-ambient single pulse* – *Figure 34: SO-28 LSD thermal impedance junction-ambient single pulse* Updated *Table 27: Thermal parameters*.
14-Jan-2010	3	Updated *Figure 26: Typical application schematic*.
13-Jul-2011	4	Updated *Features* list Updated *Figure 35: Thermal fitting model of an H-bridge in SO-28* Updated *Table 27: Thermal parameters*
02-Nov-2011	5	*Table 17: Switching (Tj = 25° C, unless otherwise specified)*: – Changed $(dV_{OUT}/dt)_{on}$ to t_r – Changed $(dV_{OUT}/dt)_{off}$ to t_f Added following tables: – *Table 12: Electrical transient requirements (part 1/3)* – *Table 13: Electrical transient requirements (part 2/3)* – *Table 14: Electrical transient requirements (part 3/3)*
19-Sep-2013	6	Updated Disclaimer.
02-Mar-2015	7	Updated: – *Section 5.1: SO-28 package mechanical data*; – Tape dimensions in *Figure 38: SO-28 tape and reel shipment (suffix “TR”) on page 32*.

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