



# VNQ690SP-E

## QUAD CHANNEL HIGH SIDE DRIVER

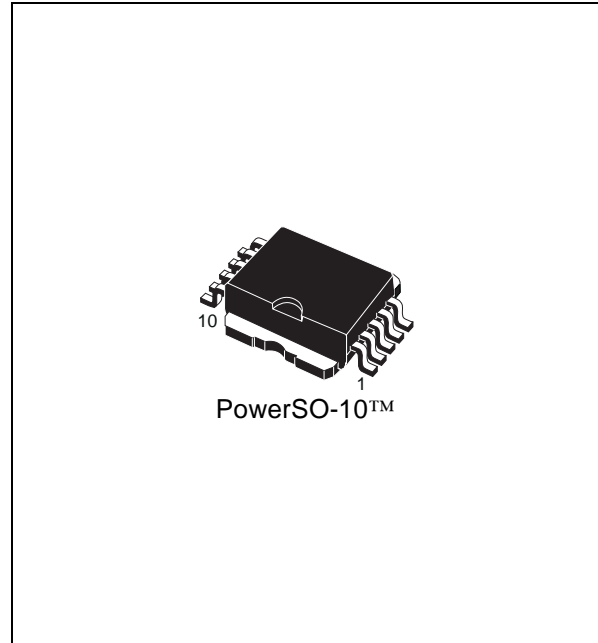
**Table 1. General Features**

Type	$R_{DS(on)}$	$I_{out}$	$V_{CC}$
VNQ690SP-E	90m $\Omega$ (*)	10A	36V

(\*) Per each channel

- OUTPUT CURRENT PER CHANNEL: 10A
- CMOS COMPATIBLE INPUTS
- OPEN LOAD DETECTION (OFF STATE)
- UNDERVOLTAGE & OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT-DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST:
  - LOSS OF GROUND & LOSS OF  $V_{CC}$
- REVERSE BATTERY PROTECTION (\*\*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

**Figure 1. Package**



### DESCRIPTION

The VNQ690SP-E is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving resistive or inductive loads with one side connected to ground. This device has four independent channels.

Built-in thermal shut down and output current limitation protect the chip from over temperature and short circuit.

**Table 2. Order Codes**

Package	Tube	Tape and Reel
PowerSO-10™	VNQ690SP-E	VNQ690SPTR-E

Note: (\*\*) See application schematic at page 9

Figure 2. Block Diagram

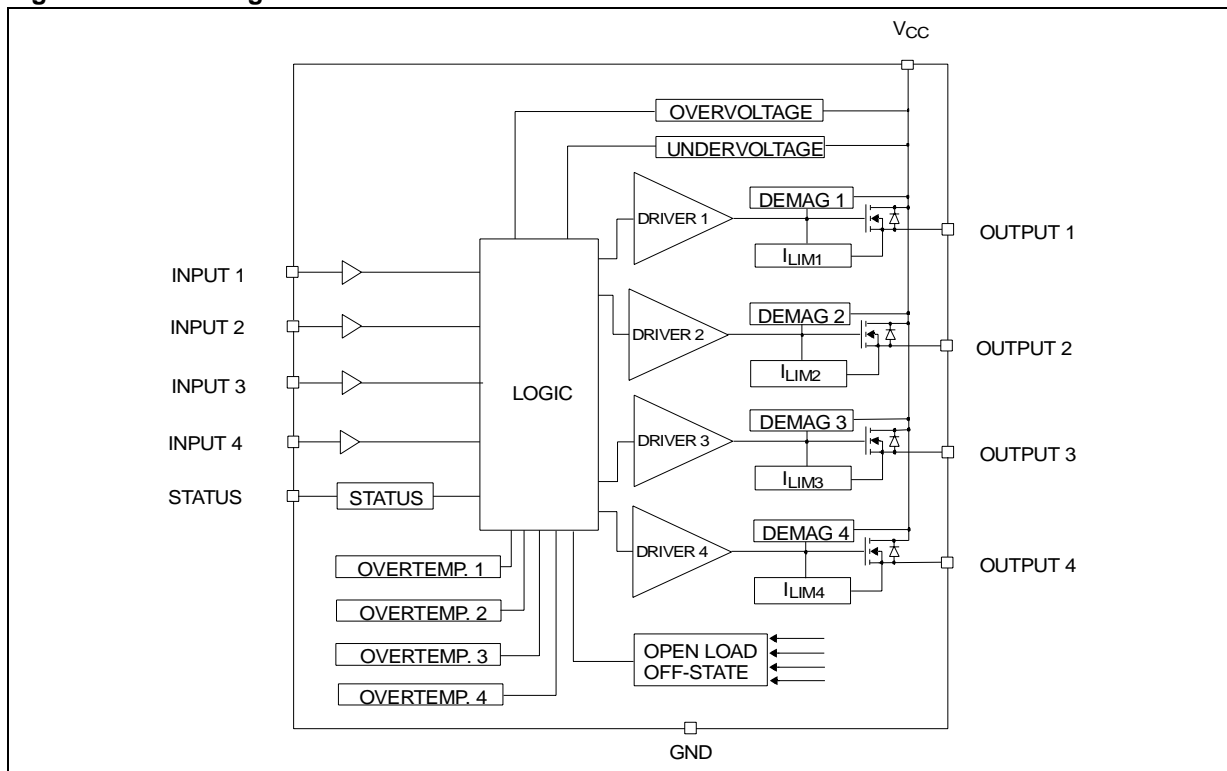


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage (continuous)	41	V
-V <sub>CC</sub>	Reverse supply voltage (continuous)	-0.3	V
I <sub>OUT</sub>	Output current (continuous), per each channel	Internally limited	A
I <sub>R</sub>	Reverse output current (continuous), per each channel	-15	A
I <sub>IN</sub>	Input current	+/- 10	mA
I <sub>STAT</sub>	Status current	+/- 10	mA
I <sub>GND</sub>	Ground current at T <sub>C</sub> ≤25°C (continuous)	-200	mA
V <sub>ESD</sub>	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- V <sub>CC</sub>	5000	V
P <sub>tot</sub>	Power dissipation at T <sub>C</sub> =25°C	78	W
E <sub>MAX</sub>	Maximum Switching Energy (L=0.38mH; R <sub>L</sub> =0Ω; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150°C; I <sub>L</sub> =14A)	53	mJ
T <sub>j</sub>	Junction operating temperature	-40 to 150	°C
T <sub>stg</sub>	Storage temperature	-65 to 150	°C

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins

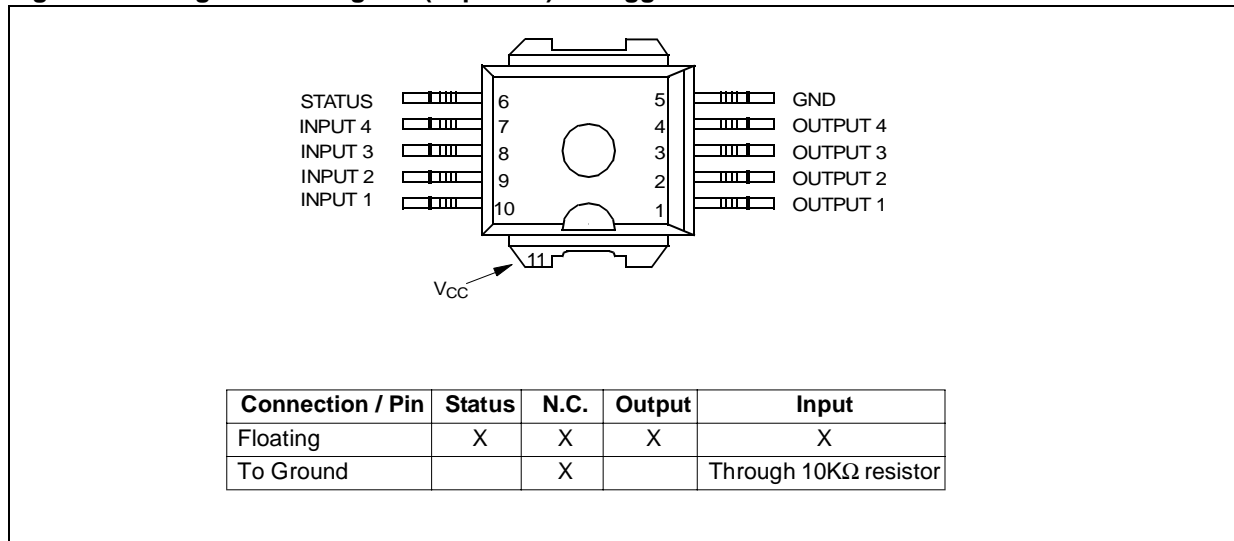


Figure 4. Current and Voltage Conventions

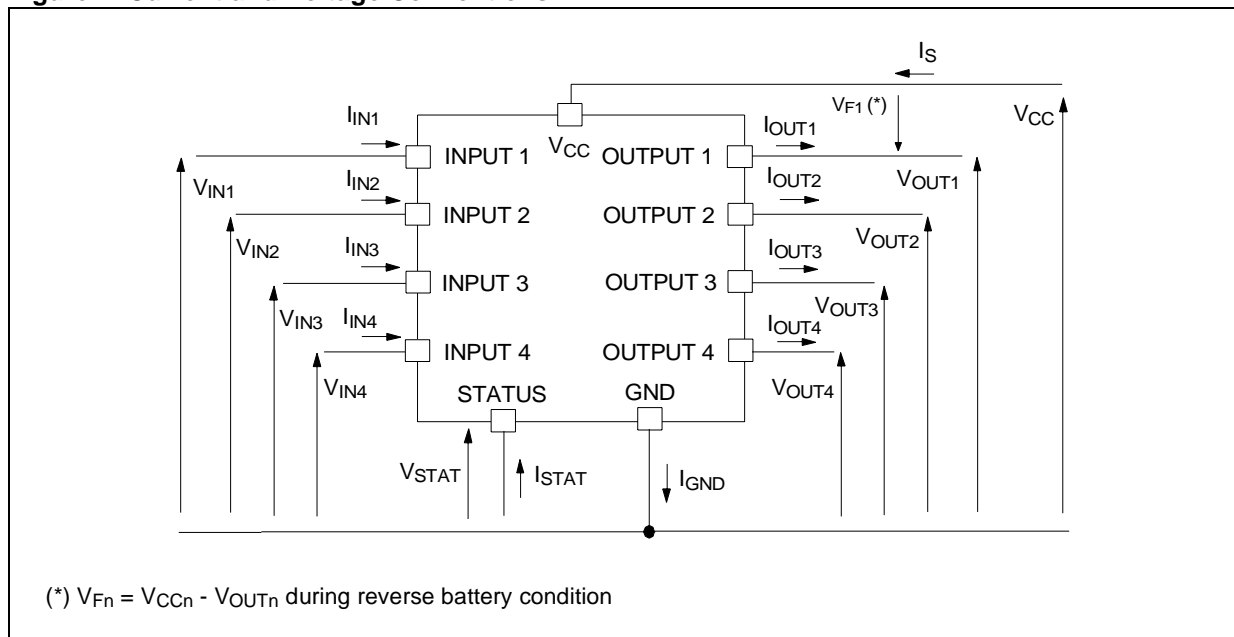


Table 4. Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX) per channel	2	°C/W
$R_{tj-amb}$	Thermal resistance junction-ambient (MAX)	52 <sup>(1)</sup>   37 <sup>(2)</sup>	°C/W

Note: 1. When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35 μm thick)

Note: 2. When mounted on a standard single-sided FR-4 board with 6cm<sup>2</sup> of Cu (at least 35 μm thick).

**ELECTRICAL CHARACTERISTICS**

 ( $V_{CC}=6V$  up to  $24V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$  unless otherwise specified)

**Table 5. Power** (Per each channel)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CC}$ (#)	Operating supply voltage		6	13	36	V
$V_{USD}$ (#)	Undervoltage shutdown		3.5	4.6	6	V
$V_{UVhyst}$ (#)	Undervoltage hysteresis		0.2		1	V
$V_{OV}$ (#)	Overvoltage shutdown		36			V
$V_{OVhyst}$ (#)	Overvoltage hysteresis		0.25			V
$I_S$ (#)	Supply current	Off state; $V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13.5V$		12	40	$\mu A$
		Off state; $V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13.5V$		12	25	$\mu A$
		$T_j=25^{\circ}C$ On state; $V_{IN}=3.25V$ ; $9V < V_{CC} < 18V$		6	12	$mA$
$R_{ON}$	On state resistance	$I_{OUT}=1A$ ; $T_j=25^{\circ}C$ ; $9V < V_{CC} < 18V$			90	$m\Omega$
		$I_{OUT}=1A$ ; $T_j=150^{\circ}C$ ; $9V < V_{CC} < 18V$			180	$m\Omega$
$I_{L(off1)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$	0		50	$\mu A$
$I_{L(off2)}$	Off State Output Current	$V_{IN}=0V$ ; $V_{OUT}=3.5V$	-75		0	$\mu A$
$I_{L(off3)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ; $T_j=125^{\circ}C$			5	$\mu A$
$I_{L(off4)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ; $T_j=25^{\circ}C$			3	$\mu A$

Note: (#) Per device.

**Table 6. Protection** (see note 1)

(per each channel)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$T_{TSD}$	Shutdown temperature		150	170	200	$^{\circ}C$
$T_R$	Reset temperature		135			$^{\circ}C$
$T_{hyst}$	Thermal hysteresis		7	15	25	$^{\circ}C$
$I_{LIM}$	DC Short circuit current	$9V < V_{CC} < 36V$	10	14	20	A
		$6V < V_{CC} < 36V$			20	A
$V_{demag}$	Turn-off output voltage clamp	$I_{OUT}=2A$ ; $V_{IN}=0V$ ; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V
$V_{STAT}$	Status low output voltage	$I_{STAT}=1.6mA$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT}=5V$			10	$\mu A$
$C_{STAT}$	Status pin input capacitance	Normal operation; $V_{STAT}=5V$			25	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT}=1mA$	6	6.8	8	V
		$I_{STAT}=-1mA$		-0.7		V

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

**ELECTRICAL CHARACTERISTICS** (continued)

**Table 7. V<sub>CC</sub> - Output Diode**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>F</sub>	Forward on Voltage	-I <sub>OUT</sub> =0.9A; T <sub>J</sub> =150°C			0.6	V

**Table 8. Switching** (V<sub>CC</sub>=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t <sub>d(on)</sub>	Turn-on delay time	R <sub>L</sub> =13Ω channels 1,2,3,4		30		μs
t <sub>d(off)</sub>	Turn-off delay time	R <sub>L</sub> =13Ω channels 1,2,3,4		30		μs
dV <sub>OUT</sub> /dt <sub>(on)</sub>	Turn-on voltage slope	R <sub>L</sub> =13Ω channels 1,2,3,4		See relative diagram		V/μs
dV <sub>OUT</sub> /dt <sub>(off)</sub>	Turn-off voltage slope	R <sub>L</sub> =13Ω channels 1,2,3,4		See relative diagram		V/μs

**Table 9. Openload Detection** (off state) per each channel

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t <sub>SDL</sub>	Status Delay	See Figure 1 (Openload detection reading must be performed after T <sub>DOL</sub> ).			20	μs
V <sub>OL</sub>	Openload Voltage Detection Threshold	V <sub>IN</sub> =0V	1.5	2.5	3.5	V
T <sub>DOL</sub>	Openload Detection Delay at Turn Off	V <sub>CC</sub> =18V			300	μs

**Table 10. Logic Input**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Input Low Level Voltage				1.25	V
V <sub>IH</sub>	Input High Level Voltage		3.25			V
V <sub>HYST</sub>	Input Hysteresis Voltage		0.5			V
I <sub>IH</sub>	Input high level voltage	V <sub>IN</sub> =3.25V			10	μA
I <sub>IL</sub>	Input Current	V <sub>IN</sub> =1.25V	1			μA
V <sub>ICL</sub>	Input Clamp Voltage	I <sub>IN</sub> =1mA	6	6.8	8	V
		I <sub>IN</sub> =-1mA		-0.7		V

**Figure 5. Status Timing Waveforms**

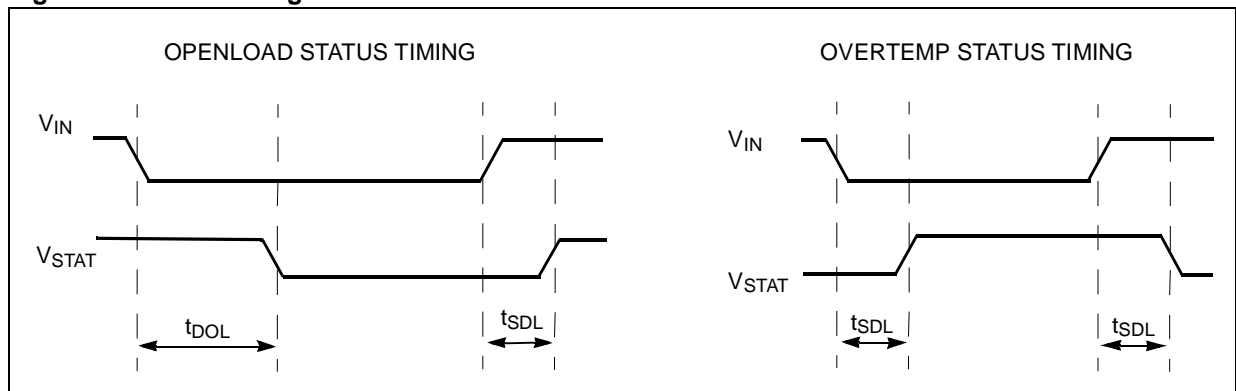


Table 11. Truth Table (Per each channel)

CONDITIONS	INPUT	OUTPUT	SENSE
Normal Operation	L	L	H
	H	H	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Current Limitation	L	L	H
	H	X	H
Output Voltage > $V_{OL}$	L	H	L
	H	H	H

Figure 6. Switching Characteristics

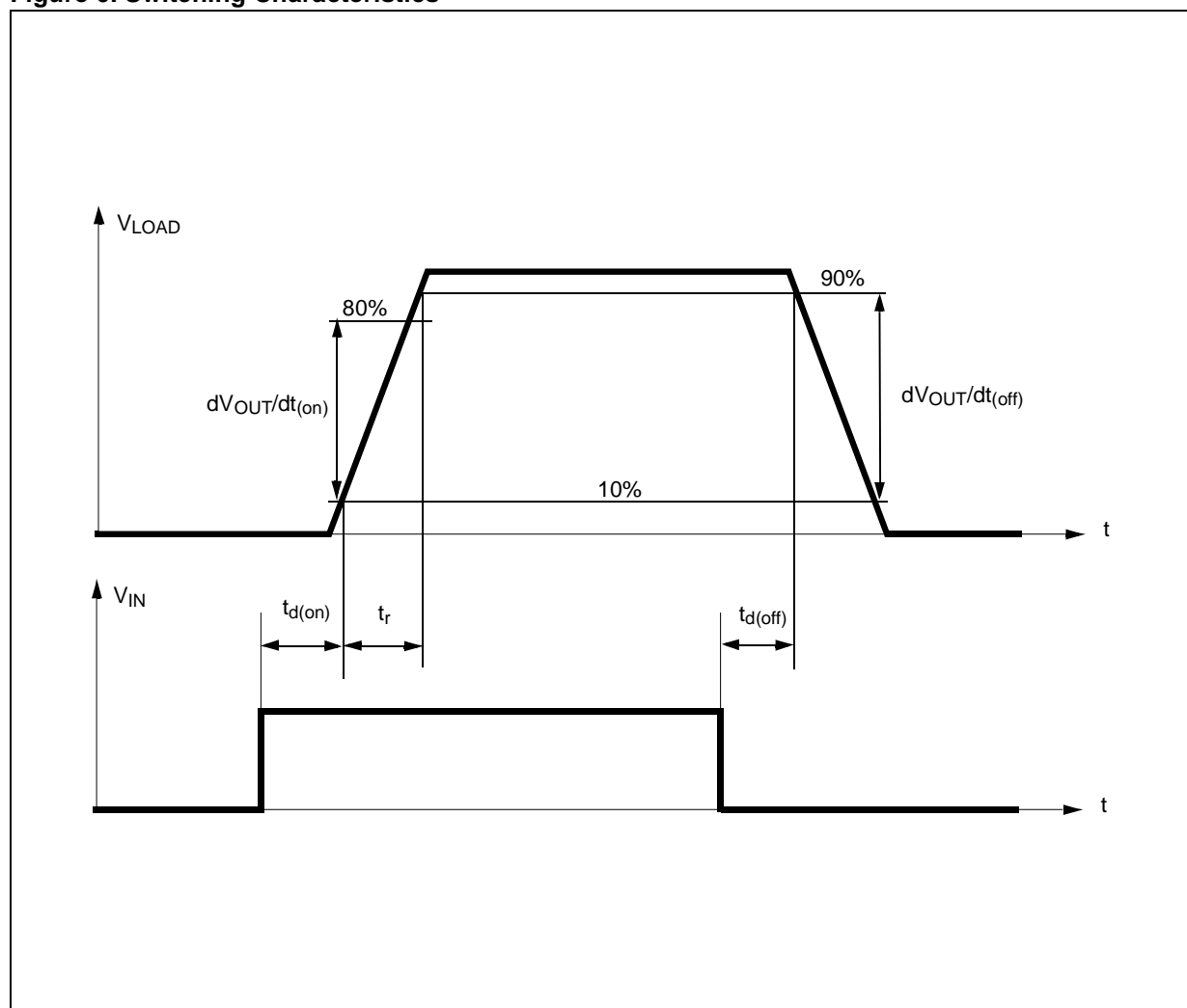


Table 12. Electrical Transient Requirements

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 $\Omega$
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 $\Omega$
3a	-25 V	-50 V	-100 V	-150 V	0.1 $\mu$ s 50 $\Omega$
3b	+25 V	+50 V	+75 V	+100 V	0.1 $\mu$ s 50 $\Omega$
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 $\Omega$

ISO T/R 7637/1 Test Pulse	Test Levels Result			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

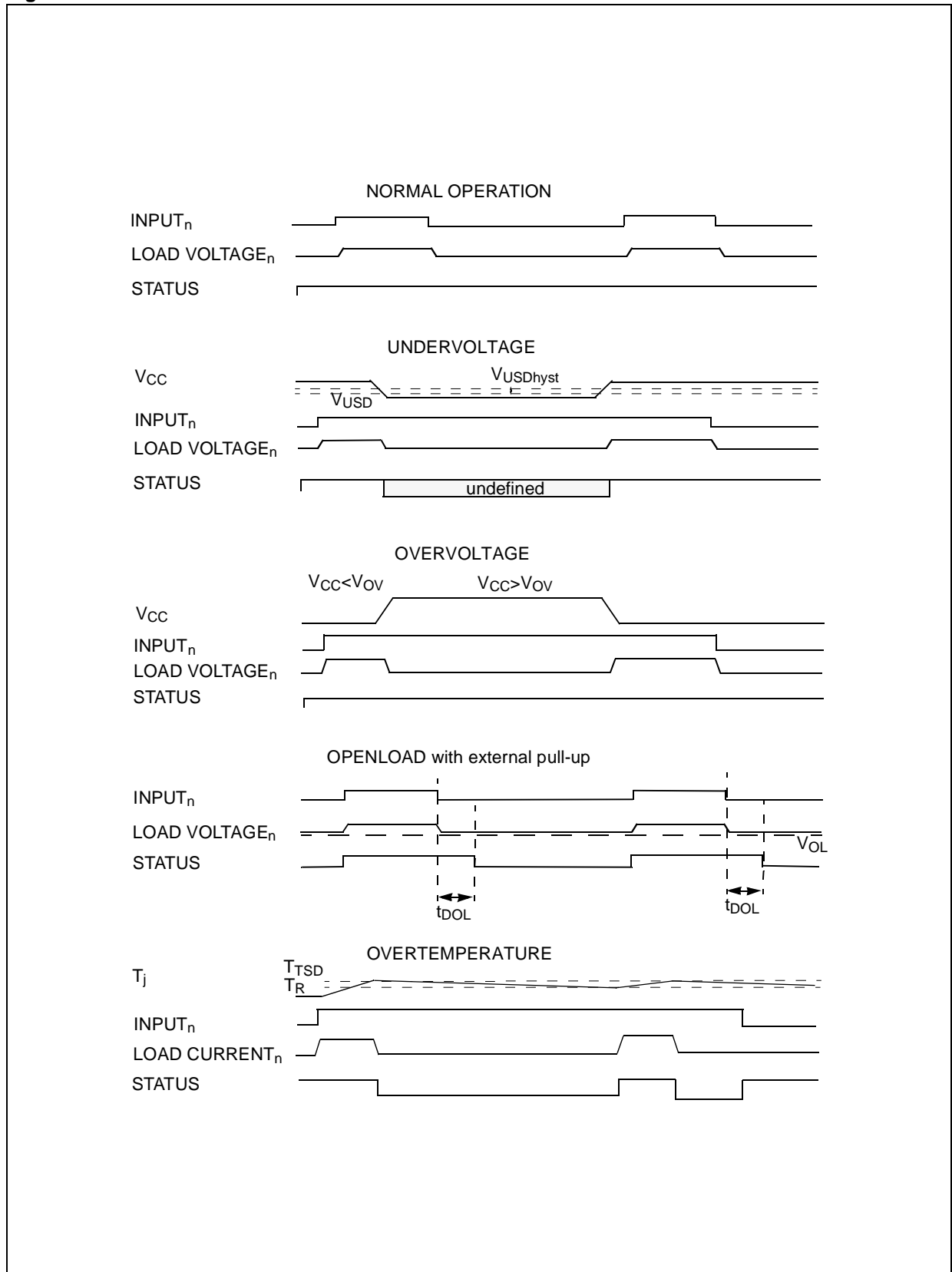
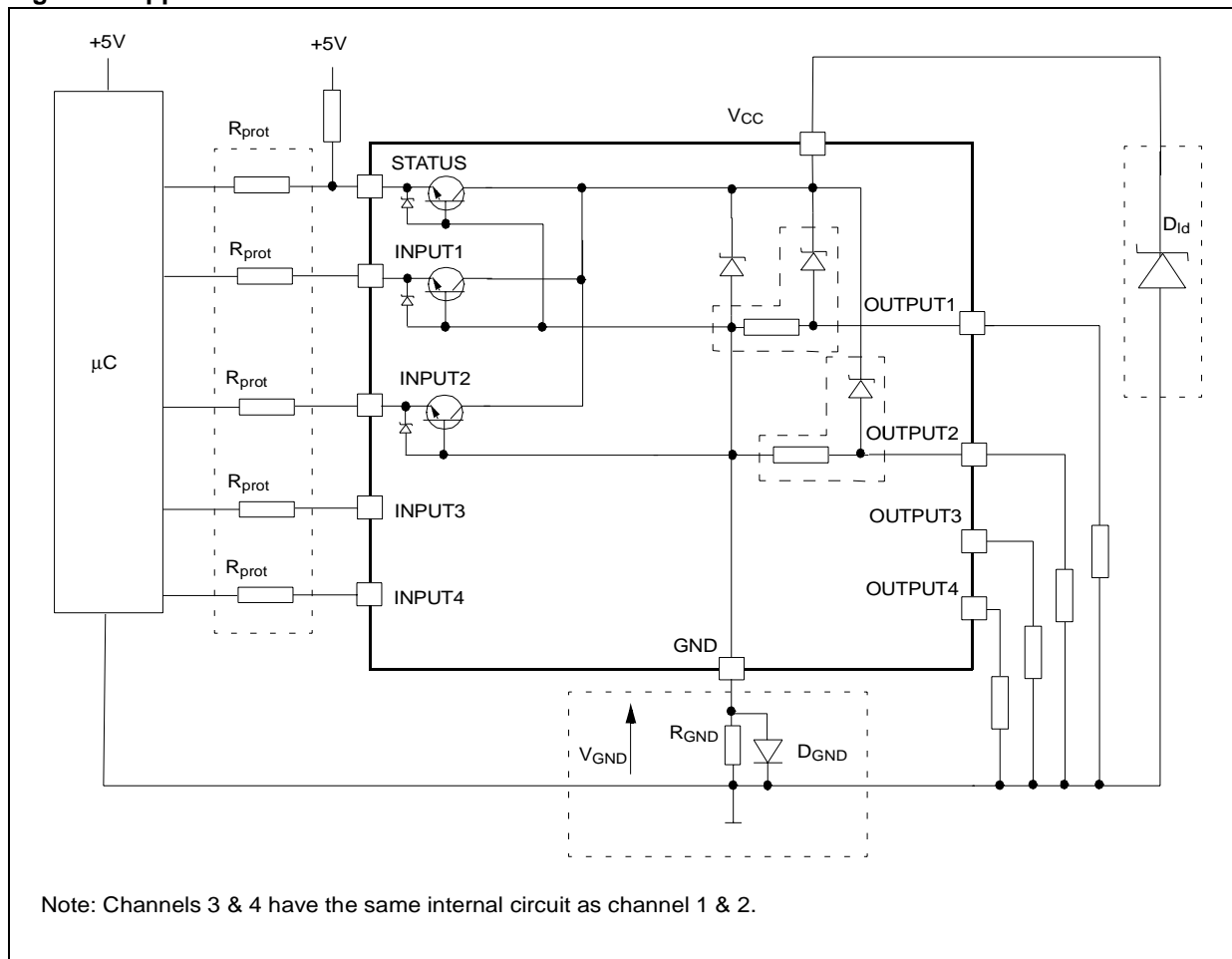




Figure 8. Application Schematic



## GND PROTECTION NETWORK AGAINST REVERSE BATTERY

**Solution 1:** Resistor in the ground line ( $R_{GND}$  only). This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

- 1)  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

**Solution 2:** A diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND} = 1\text{k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\approx 600\text{mV}$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## LOAD DUMP PROTECTION

$D_{id}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds  $V_{CC}$  max DC rating. The same applies if the device will be subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

### **μC I/Os PROTECTION:**

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

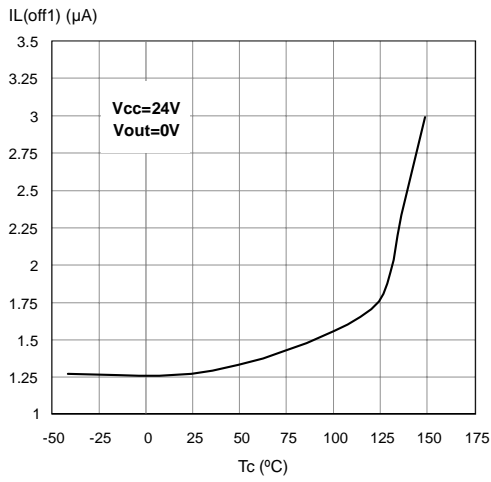
Calculation example:

For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$

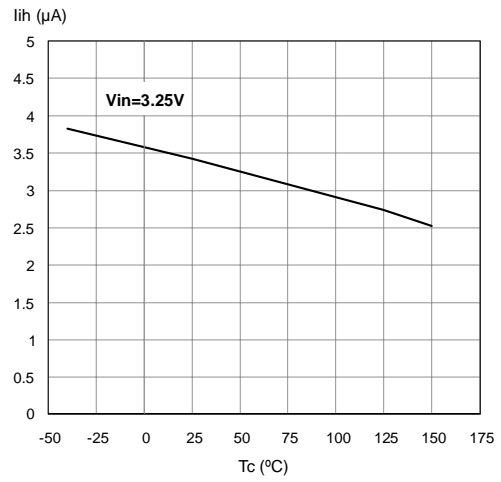
$$5k\Omega \leq R_{prot} \leq 65k\Omega.$$

Recommended  $R_{prot}$  value is 10kΩ.

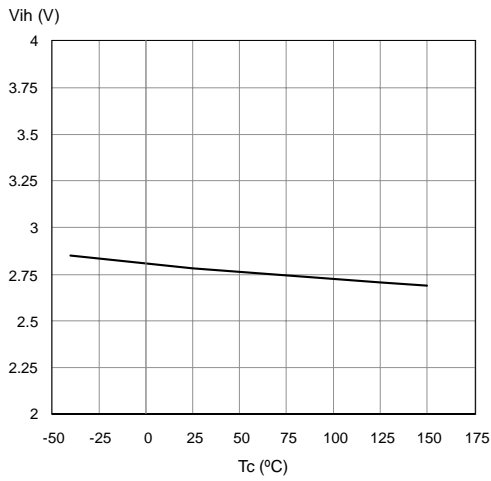
**Figure 9. Off State Output Current**



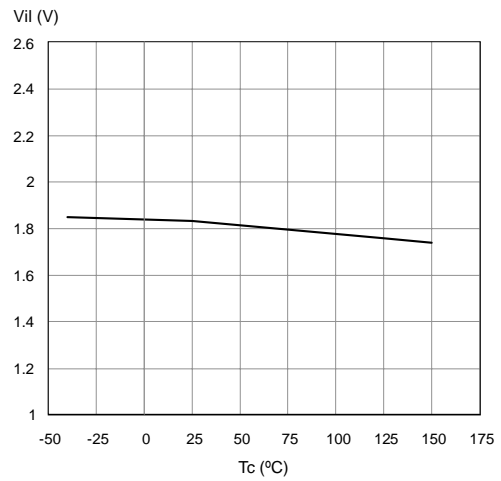
**Figure 12. High Level Input Current**



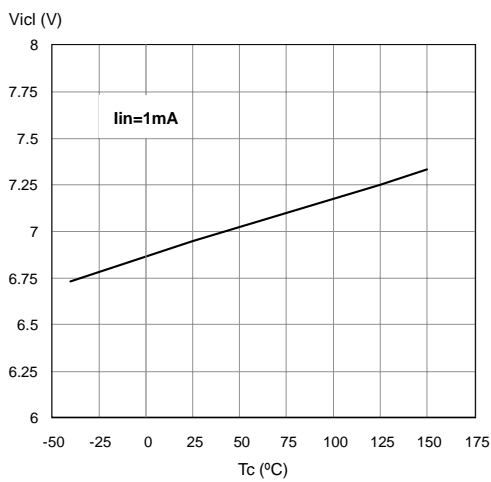
**Figure 10. Input High Level**



**Figure 13. Input Low Level**



**Figure 11. Input Clamp Voltage**



**Figure 14. Input Hysteresis Voltage**

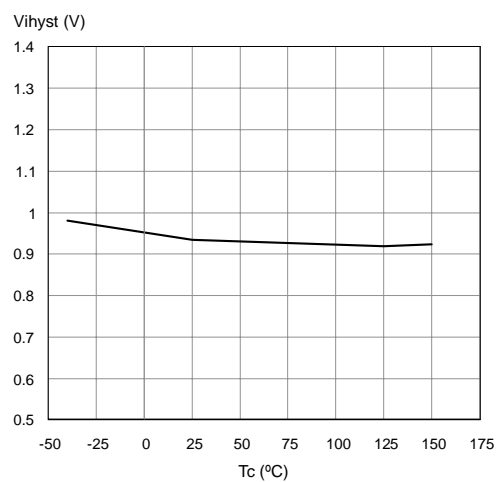


Figure 15. Overvoltage Shutdown

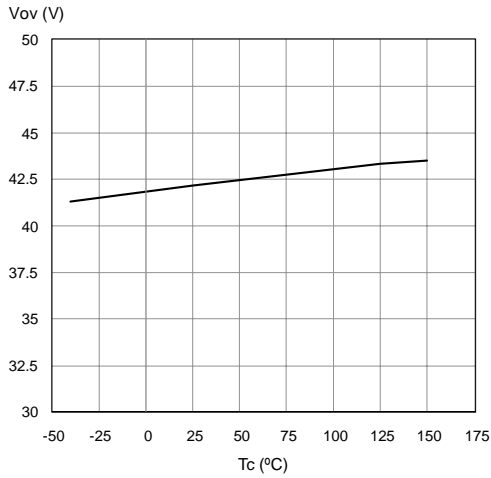


Figure 18. Openload Off State Detection Threshold

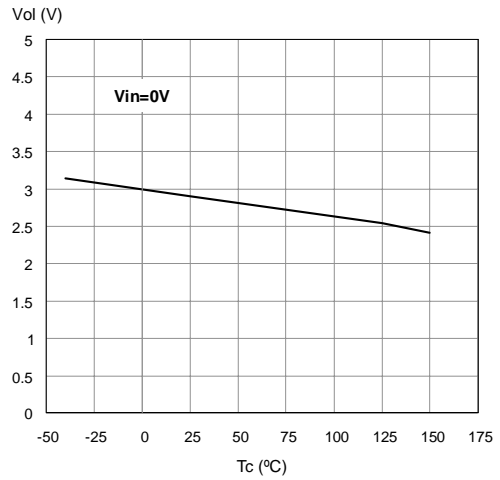


Figure 16. Turn-on Voltage Slope

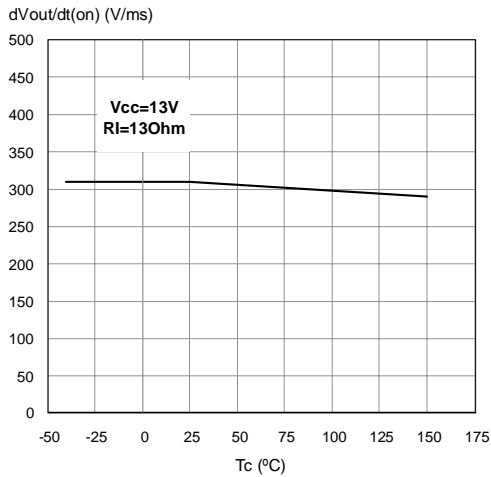


Figure 19. Turn-off Voltage Slope

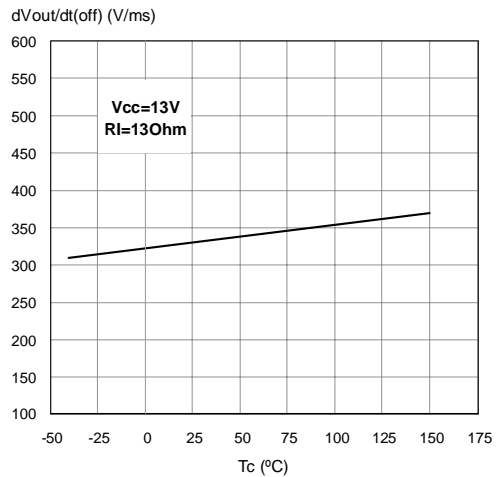


Figure 17. I<sub>LIM</sub> Vs T<sub>case</sub>

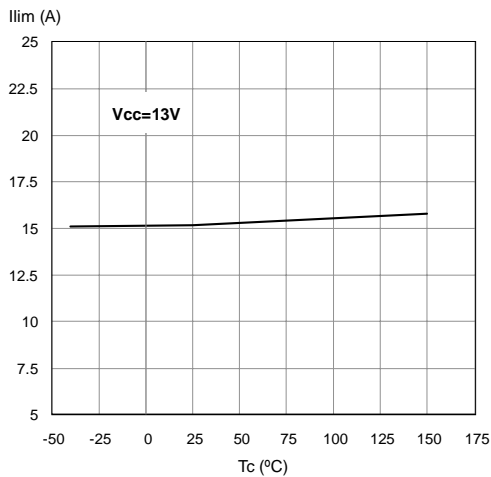
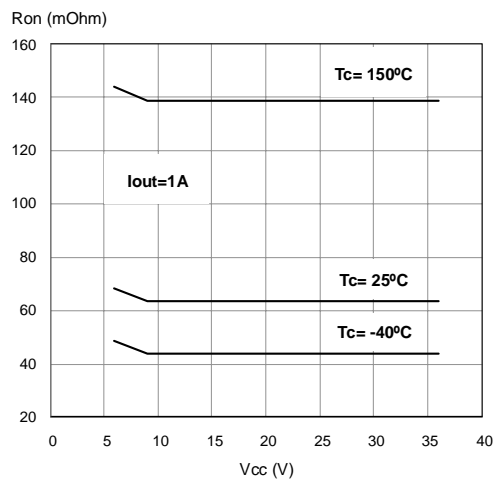
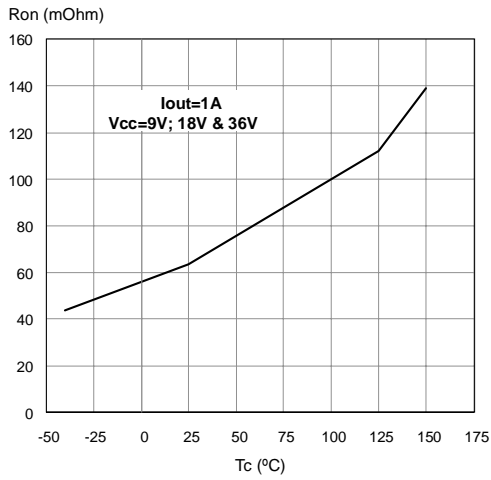


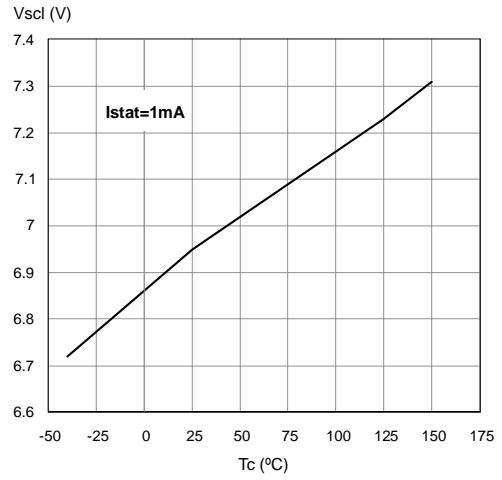
Figure 20. On State Resistance Vs V<sub>CC</sub>



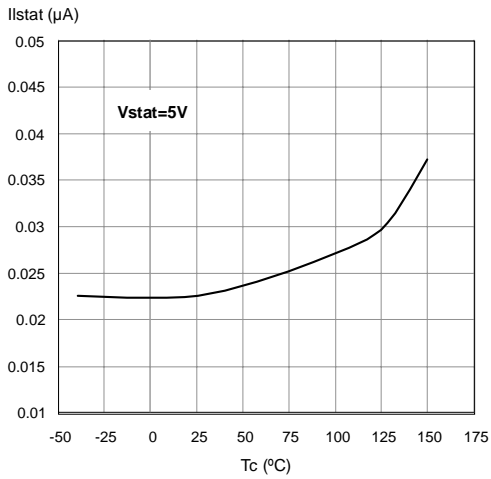
**Figure 21. On State Resistance Vs  $T_{case}$**



**Figure 23. Status Clamp Voltage**



**Figure 22. Status Leakage Current**



**Figure 24. Status Low Output Voltage**

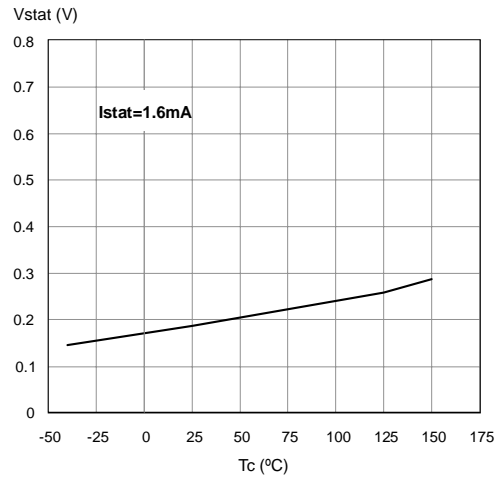
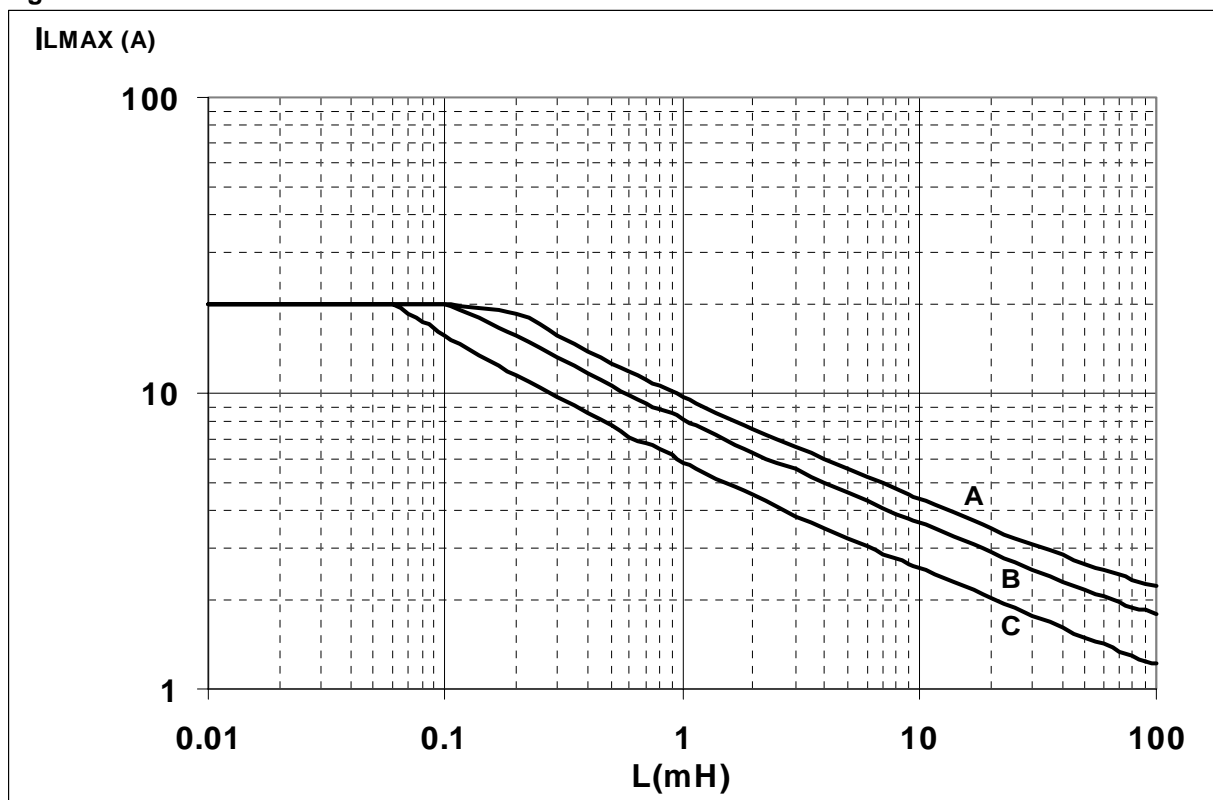


Figure 25. Maximum turn off current versus load inductance



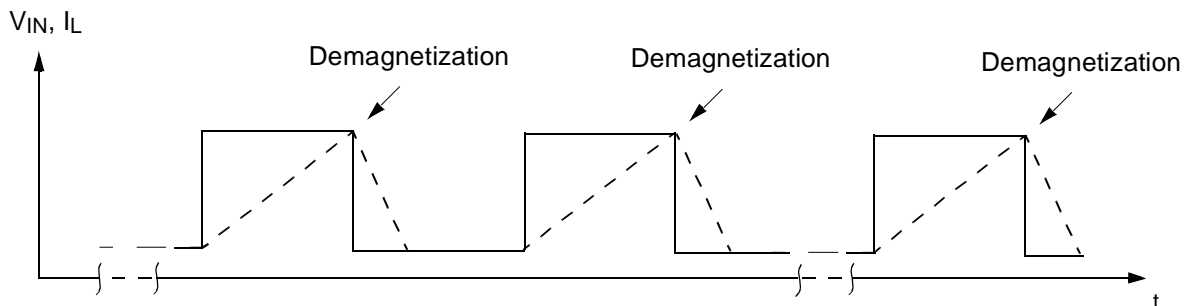
- A = Single Pulse at  $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at  $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at  $T_{Jstart}=125^{\circ}C$

Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5V$



PowerSO-10™ Thermal Data

Figure 26. PowerSO-10™ PC Board

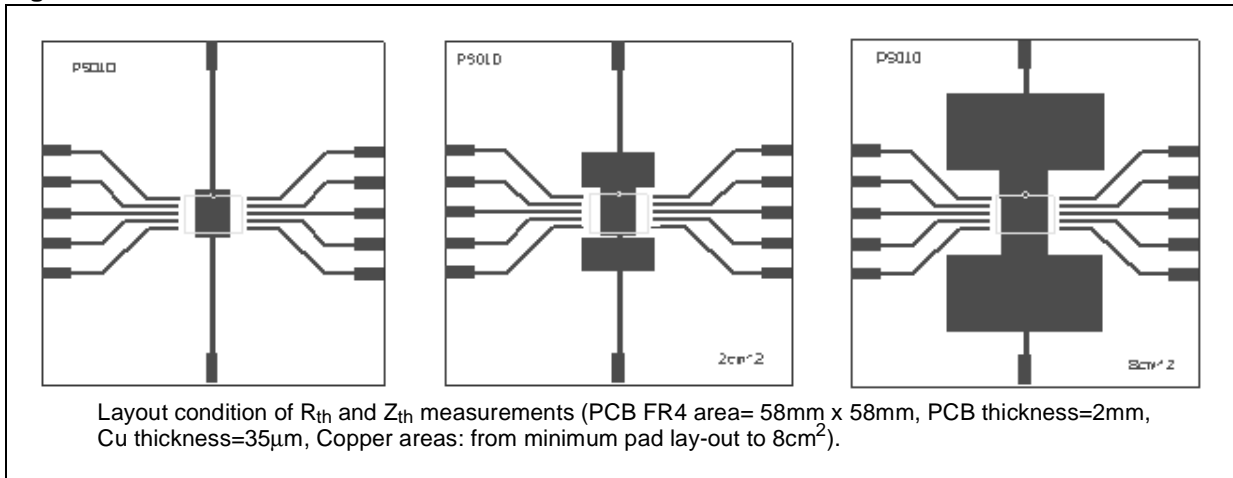


Figure 27.  $R_{thj-amb}$  Vs PCB copper area in open box free air condition

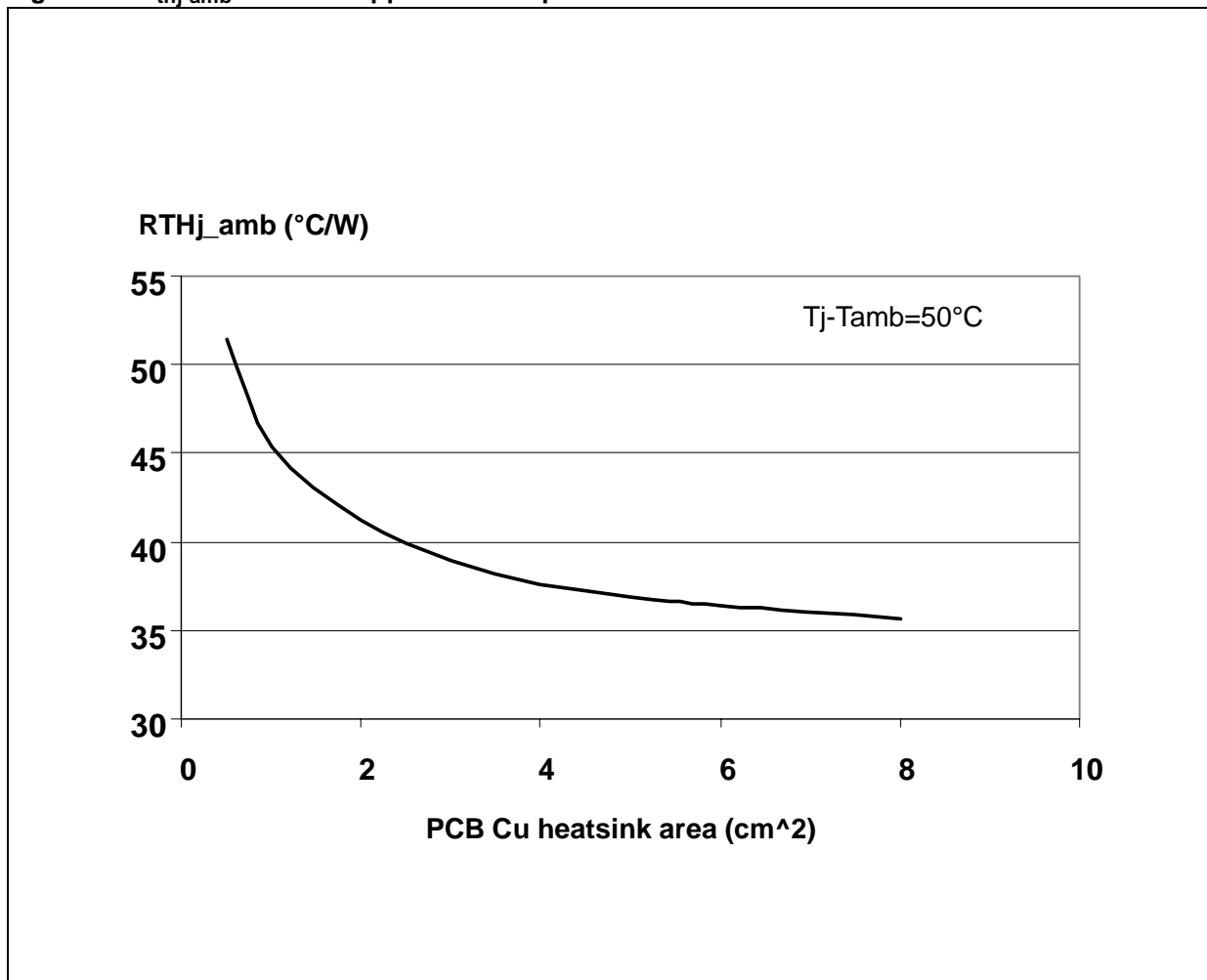


Figure 28. PowerSO-10 Thermal Impedance Junction Ambient Single Pulse

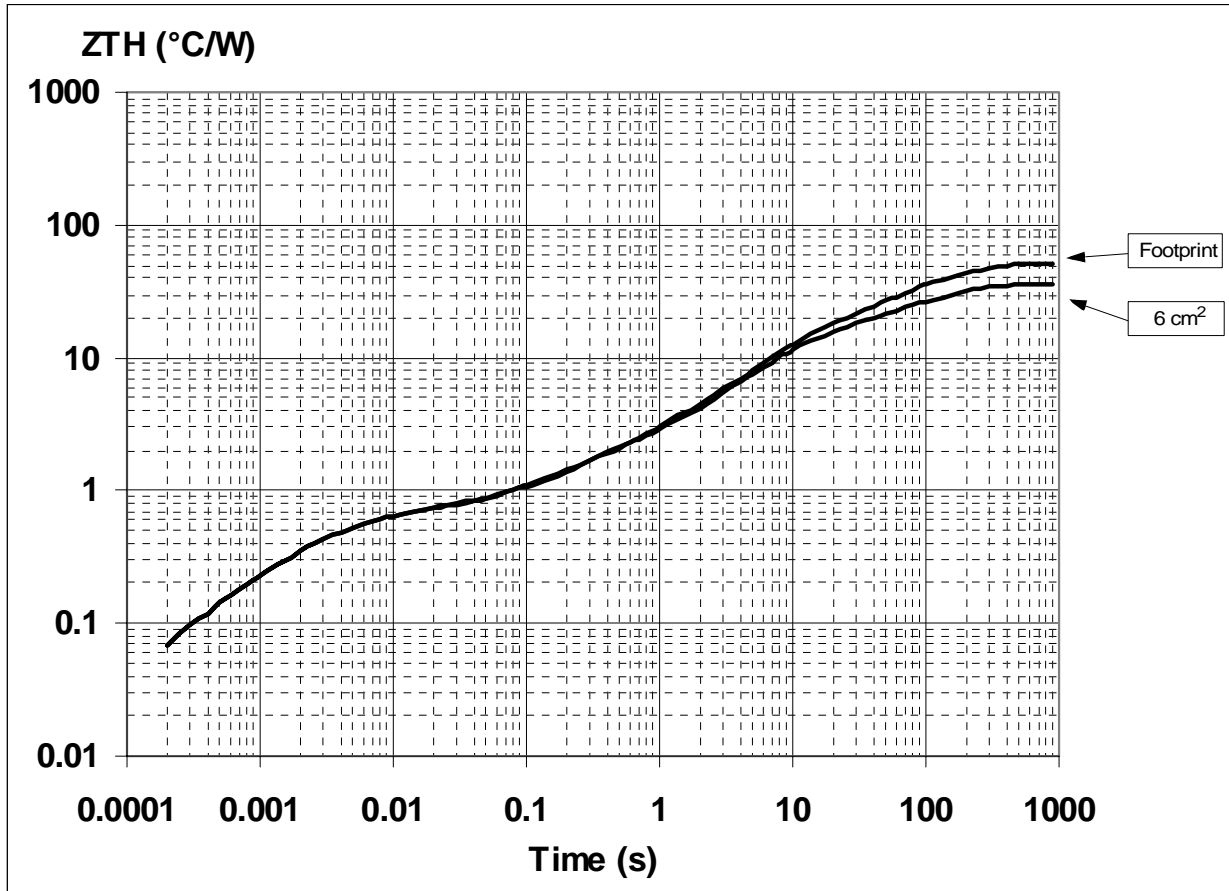
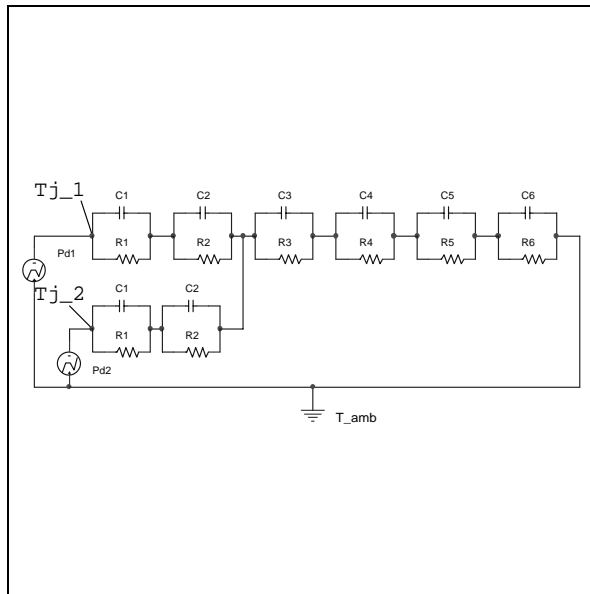


Figure 29. Thermal fitting model of a double channel HSD in PowerSO-10



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Table 13. Thermal Parameter

Area/island (cm <sup>2</sup> )	Footprint	6
R1 (°C/W)	0.05	
R2 (°C/W)	0.3	
R3 (°C/W)	0.3	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.001	
C2 (W.s/°C)	5.00E-03	
C3 (W.s/°C)	0.02	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5



PACKAGE MECHANICAL

Table 14. PowerSO-10™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	3.35		3.65
A (*)	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B (*)	0.37		0.53
C	0.35		0.55
C (*)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 (*)	7.30		7.50
E4	5.90		6.10
E4 (*)	5.90		6.30
e		1.27	
F	1.25		1.35
F (*)	1.20		1.40
H	13.80		14.40
H (*)	13.85		14.35
h		0.50	
L	1.20		1.80
L (*)	0.80		1.10
a	0°		8°
α (*)	2°		8°

Note: (\*) Muar only POA P013P

Figure 30. PowerSO-10™ Package Dimensions

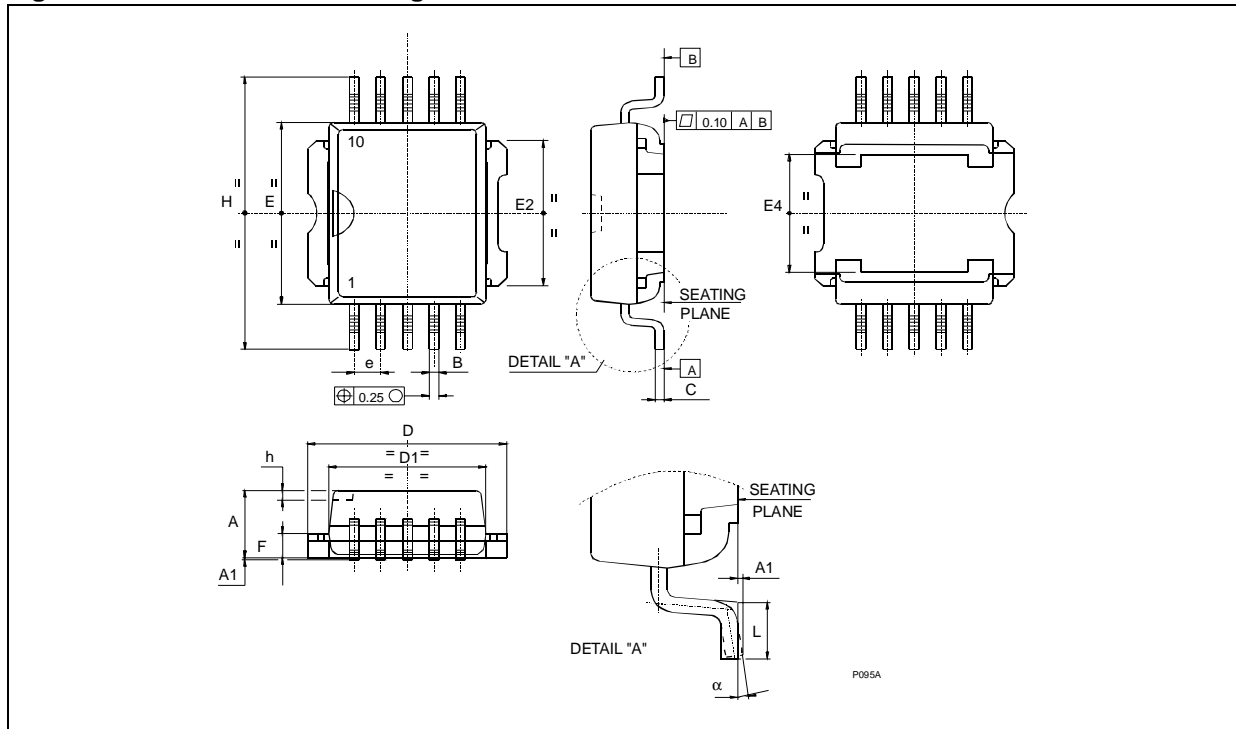


Figure 31. PowerSO-10™ Suggested Pad Layout And Tube Shipment (No Suffix)

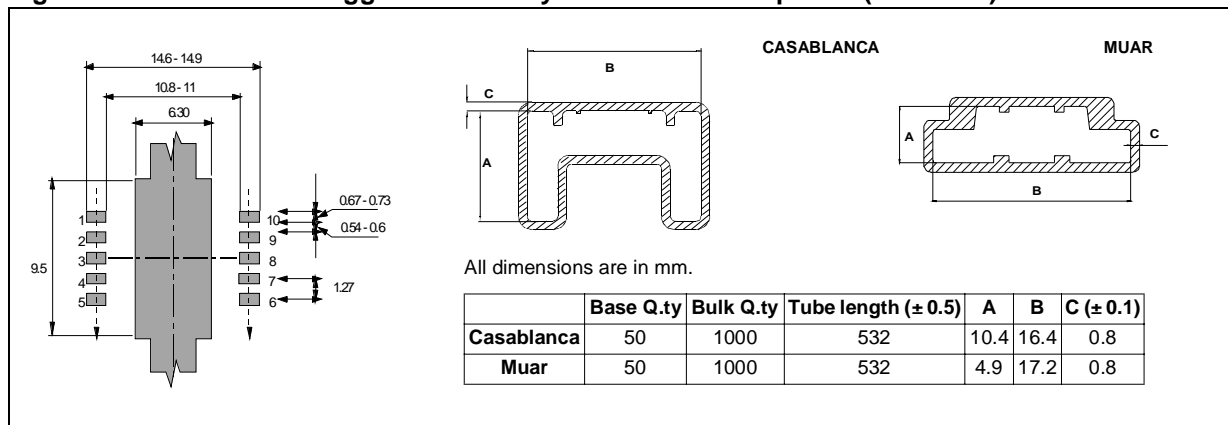
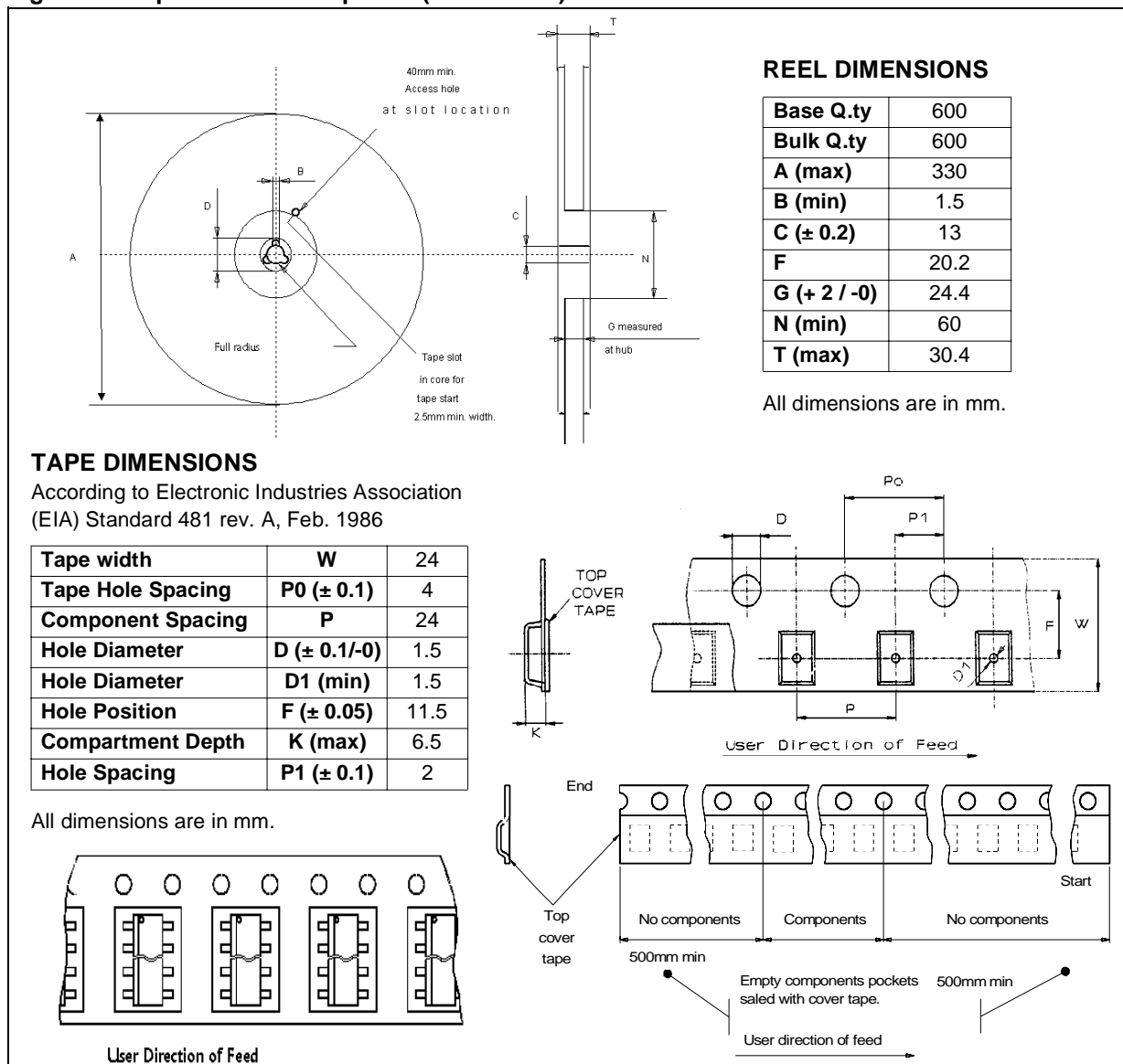


Figure 32. Tape And Reel Shipment (suffix “TR”)



**REVISION HISTORY**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
Oct. 2004	1	- First Issue.
September 2013	2	- Updated Disclaimer.

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