

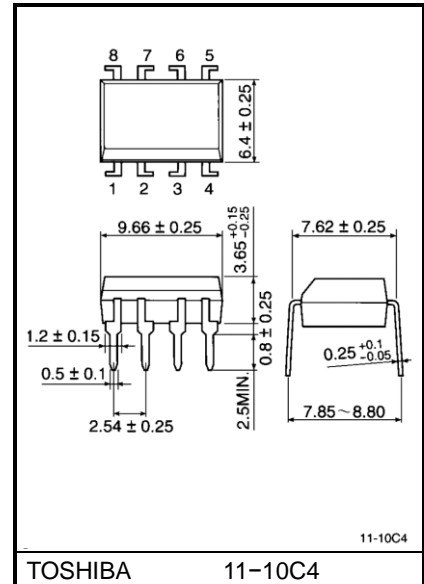
# TLP759

Digital Logic Ground Isolation  
 Line Receiver  
 Microprocessor System Interfaces  
 Switching Power Supply Feedback Control  
 Industrial Inverter

The TOSHIBA TLP759 consists of a GaAlAs high-output light emitting diode and a high speed detector of one chip photo diode-transistor. This unit is 8-lead DIP.  
 TLP759 has no internal base connection, and a Faraday shield integrated on the photodetector chip provides an effective common mode noise transient immunity.  
 So this is suitable for application in noisy environmental condition.

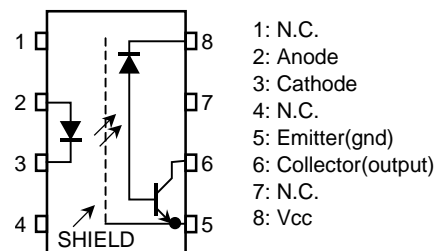
- Isolation voltage: 5000 Vrms (min)
  - Switching speed:  $t_{pHL} = 0.2\mu s$  (typ.)  
 $t_{pLH} = 0.3\mu s$  (typ.) ( $R_L=1.9 k\Omega$ )
  - TTL compatible
  - UL Approved: UL1577, file No. E67349
  - c-UL approved :CSA Component Acceptance Service No. 5A, File No.E67349
  - Option (D4) type  
 VDE Approved: DIN EN 60747-5-5 (Note 1)
- Note 1: When a EN 60747-5-5 approved type is needed, please designate the "Option (D4)"**
- Mechanical Parameters  
 Creepage distance: 7.0 mm (min)  
 Clearance: 7.0 mm (min)  
 Insulation thickness: 0.4 mm (min)

Unit: mm

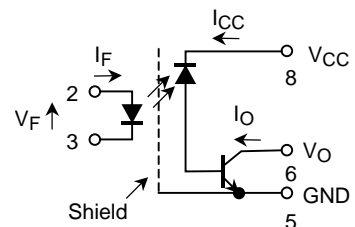


Weight: 0.54 g (typ.)

### Pin Configuration (top view)



### Schematic



Start of commercial production  
 1993-01

## Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current	I <sub>F</sub>	25	mA
	Forward current derating (Ta ≥70°C)	I <sub>F</sub> / Ta	-0.8	mA / °C
	Pulse forward current (Note 1)	I <sub>FP</sub>	50	mA
	Peak transient forward current (Note 2)	I <sub>FPT</sub>	1	A
	Reverse voltage	V <sub>R</sub>	5	V
	Diode power dissipation (Note 3)	P <sub>D</sub>	45	mW
Detector	Output current	I <sub>O</sub>	8	mA
	Peak output current	I <sub>OP</sub>	16	mA
	Output voltage	V <sub>O</sub>	-0.5 to 20	V
	Supply voltage	V <sub>CC</sub>	-0.5 to 30	V
	Output power dissipation	P <sub>O</sub>	100	mW
	Output power dissipation derating (Ta ≥70°C)	P <sub>O</sub> / Ta	-2	mW / °C
Operating temperature range		T <sub>opr</sub>	-55 to 100	°C
Storage temperature range		T <sub>stg</sub>	-55 to 125	°C
Lead solder temperature (10 s) (Note 4)		T <sub>sol</sub>	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60%) (Note 5)		BV <sub>S</sub>	5000	V <sub>rms</sub>

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) 50% duty cycle, 1 ms pulse width. Derate 1.6mA / °C above 70°C.

(Note 2) Pulse width ≤ 1μs, 300pps.

(Note 3) Derate 0.9mW / °C above 70°C.

(Note 4) Soldering portion of lead: Up to 2mm from the body of the device.

(Note 5) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

## Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
LDE	Forward voltage	V <sub>F</sub>	I <sub>F</sub> = 16mA	—	1.65	1.85	V
	Forward voltage temperature coefficient	ΔV <sub>F</sub> / ΔT <sub>a</sub>	I <sub>F</sub> = 16mA	—	-2	—	mV / °C
	Reverse current	I <sub>R</sub>	V <sub>R</sub> = 5V	—	—	10	μA
	Capacitance between terminals	C <sub>T</sub>	V = 0 V, f = 1MHz	—	45	—	pF
Detector	High level output current	I <sub>OH</sub> (1)	I <sub>F</sub> = 0mA, V <sub>CC</sub> = V <sub>O</sub> = 5.5V	—	3	500	nA
		I <sub>OH</sub> (2)	I <sub>F</sub> = 0mA, V <sub>CC</sub> = 30V, V <sub>O</sub> = 20V	—	—	5	μA
		I <sub>OH</sub>	I <sub>F</sub> = 0mA, V <sub>CC</sub> = 30V, V <sub>O</sub> = 20V T <sub>a</sub> = 70°C	—	—	50	
	High level supply voltage	I <sub>CC</sub> H	I <sub>F</sub> = 0mA, V <sub>CC</sub> = 30V	—	0.01	1	μA
Coupled	Current transfer ratio	I <sub>O</sub> / I <sub>F</sub>	I <sub>F</sub> = 16mA, V <sub>CC</sub> = 4.5V V <sub>O</sub> = 0.4V	20	40	—	%
	Low level output voltage	V <sub>OL</sub>	I <sub>F</sub> = 16mA, V <sub>CC</sub> = 4.5V I <sub>O</sub> = 2.4 mA	—	—	0.4	V
	Resistance (input-output)	R <sub>S</sub>	R.H. ≤ 60%, V <sub>S</sub> = 500V (Note 1)	1×10 <sup>12</sup>	10 <sup>14</sup>	—	Ω
	Capacitance (input-output)	C <sub>S</sub>	V <sub>S</sub> = 0 V, f = 1MHz (Note 1)	—	0.8	—	pF
	Isolation voltage	BV <sub>S</sub>	AC, 60 s	5000	—	—	V <sub>rms</sub>
AC, 1 s, in oil			—	10000	—		
DC, 60 s, in oil			—	10000	—	V <sub>dc</sub>	

(Note 1) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

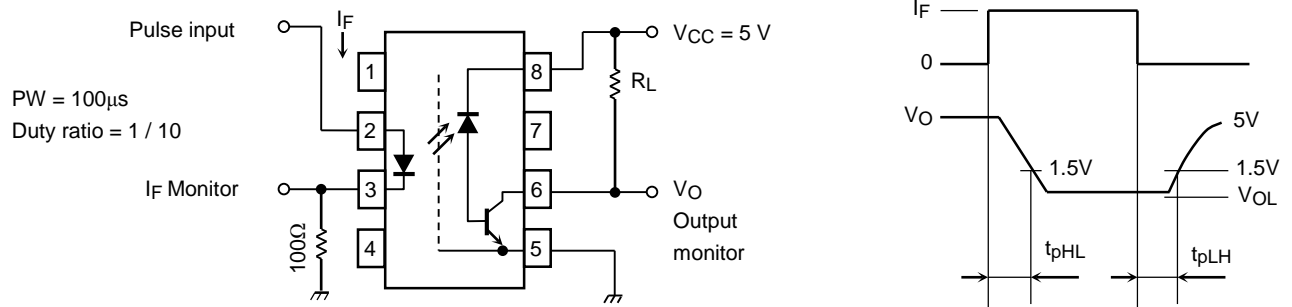
## Switching Characteristics (Ta = 25°C, VCC = 5V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H → L)	t <sub>pHL</sub>	1	I <sub>F</sub> = 0 → 16mA, R <sub>L</sub> = 1.9kΩ	—	0.2	0.8	μs
Propagation delay time (L → H)	t <sub>pLH</sub>						
Common mode transient immunity at logic high output (Note 1)	CM <sub>H</sub>	2	I <sub>F</sub> = 0mA, V <sub>CM</sub> = 400V <sub>p-p</sub> R <sub>L</sub> = 4.1kΩ	5000	10000	—	V / μs
Common mode transient immunity at logic low output (Note 1)	CM <sub>L</sub>						

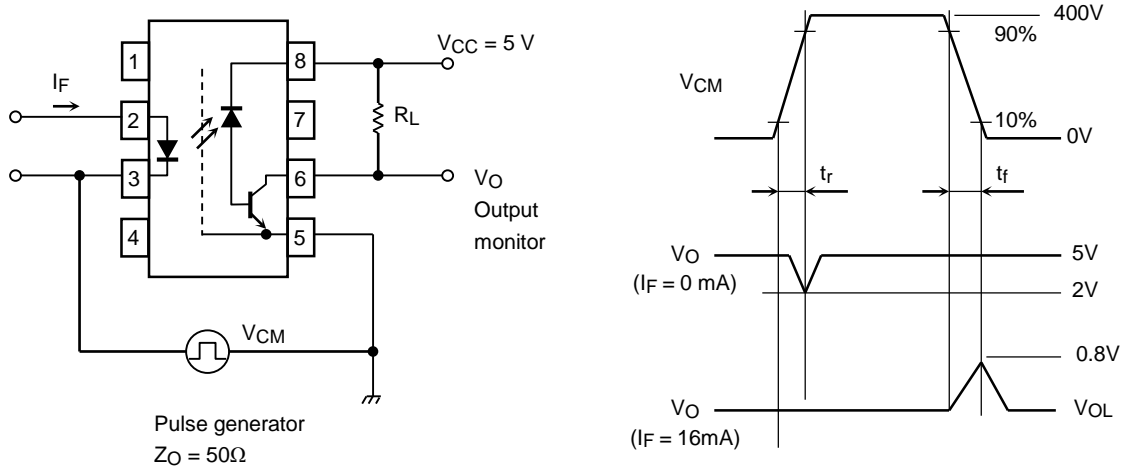
(Note 1) CML is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V<sub>O</sub> < 0.8V).

CMH is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V<sub>O</sub> > 2.0V).

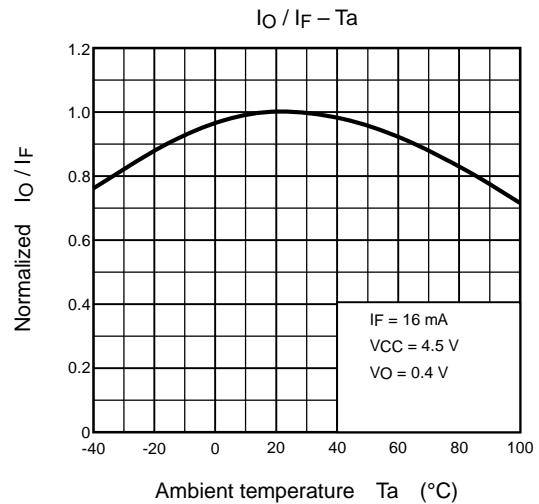
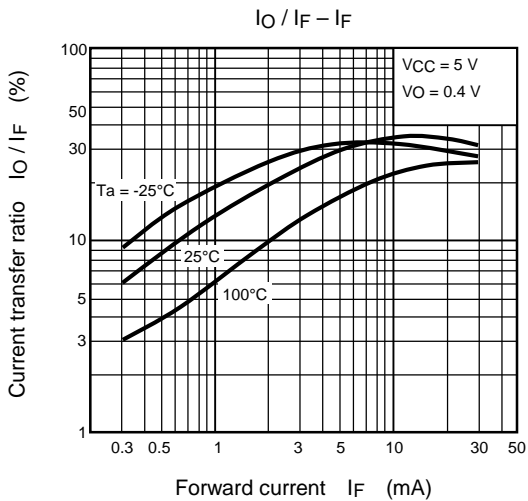
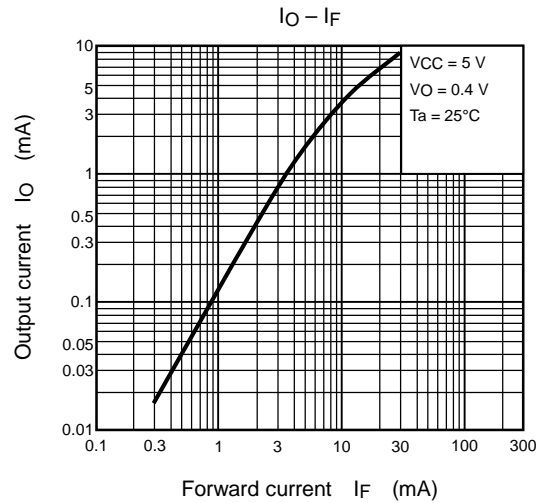
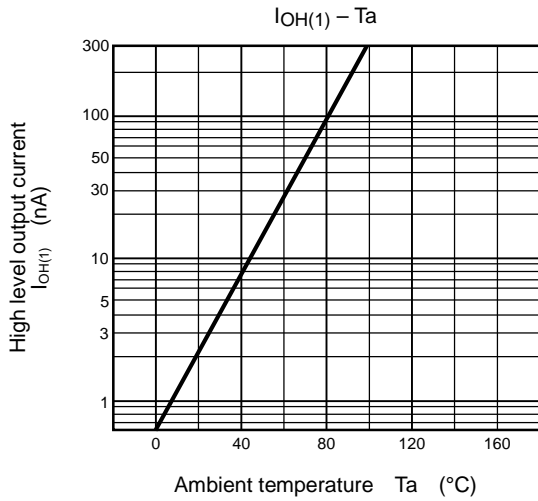
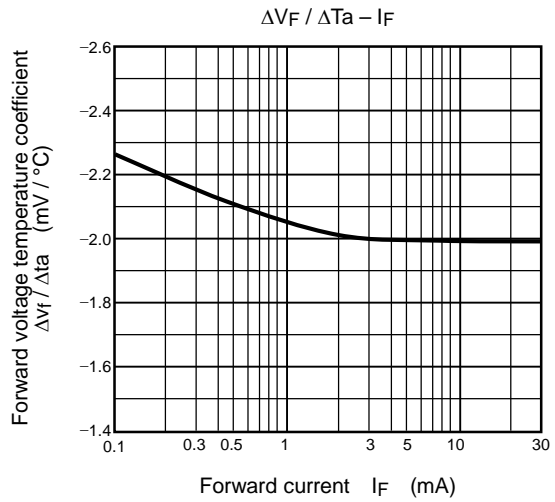
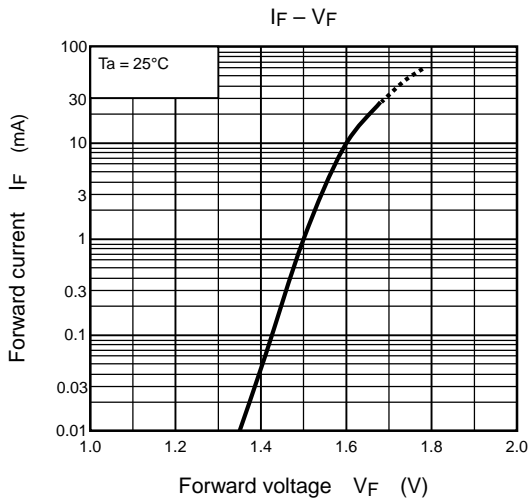
## Test Circuit 1: Switching Time Test Circuit

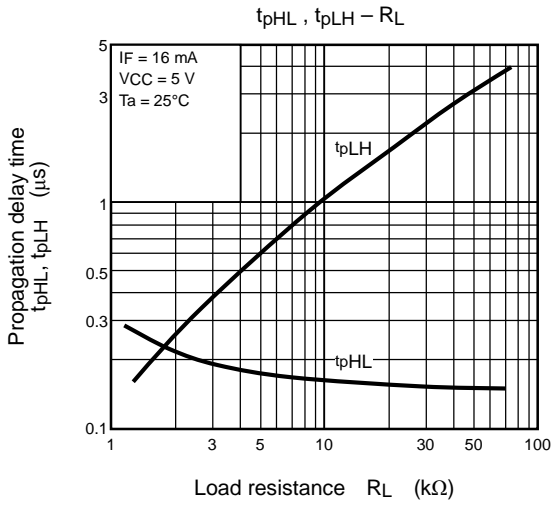
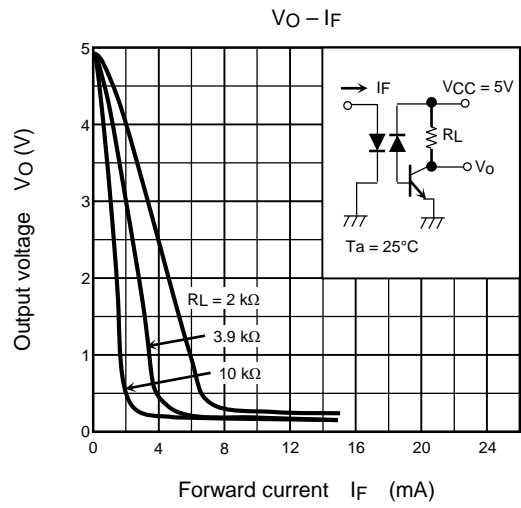
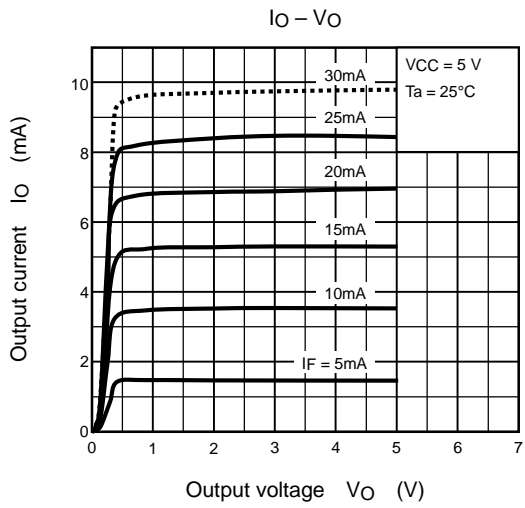


## Test Circuit 2: Common Mode Noise Immunity Test Circuit



$$CM_H = \frac{320\text{ (V)}}{t_r\text{ (\mu s)}}, CM_L = \frac{320\text{ (V)}}{t_f\text{ (\mu s)}}$$





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