



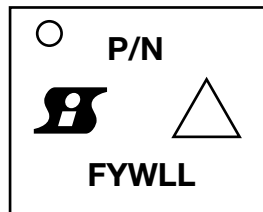


ORDERING INFORMATION		
PART NUMBER	PACKAGE	MARKING (LINE 2: P/N)
SiP12109DMP-T1-GE4	QFN16 3x3	2109
SiP12109DB	N/A	-

Note

- “DB” means demo board

MARKING



Format:

- Line 1: Dot
- Line 2: P/N
- Line 3: Siliconix Logo + ESD Symbol
- Line 4: Factory Code + Year Code + Work Week Code + LOT Code

ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	CONDITIONS	LIMIT	UNIT
V <sub>IN</sub>	Reference to P <sub>GND</sub>	-0.3 to 16	V
V <sub>CC</sub>	Reference to A <sub>GND</sub>	-0.3 to 6	
LX	Reference to P <sub>GND</sub>	-0.3 to 16	
LX (AC)	100 ns	17	
Boot		-0.3 to V <sub>IN</sub> + V <sub>CC</sub>	
A <sub>GND</sub> to P <sub>GND</sub>		-0.3 to +0.3	
All Logic Inputs	Reference to A <sub>GND</sub>	-0.3 to V <sub>CC</sub> + 0.3	
TEMPERATURE			
Max. Operating Junction Temperature		-40 to 150	°C
Storage Temperature		-65 to 150	
POWER DISSIPATION			
Junction to Ambient Thermal Impedance (R <sub>thJA</sub> )		36.3	°C/W
Maximum Power Dissipation	Ambient Temperature = 25 °C	3.4	W
	Ambient Temperature = 100 °C	1.3	
ESD PROTECTION			
	HBM	2	kV

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

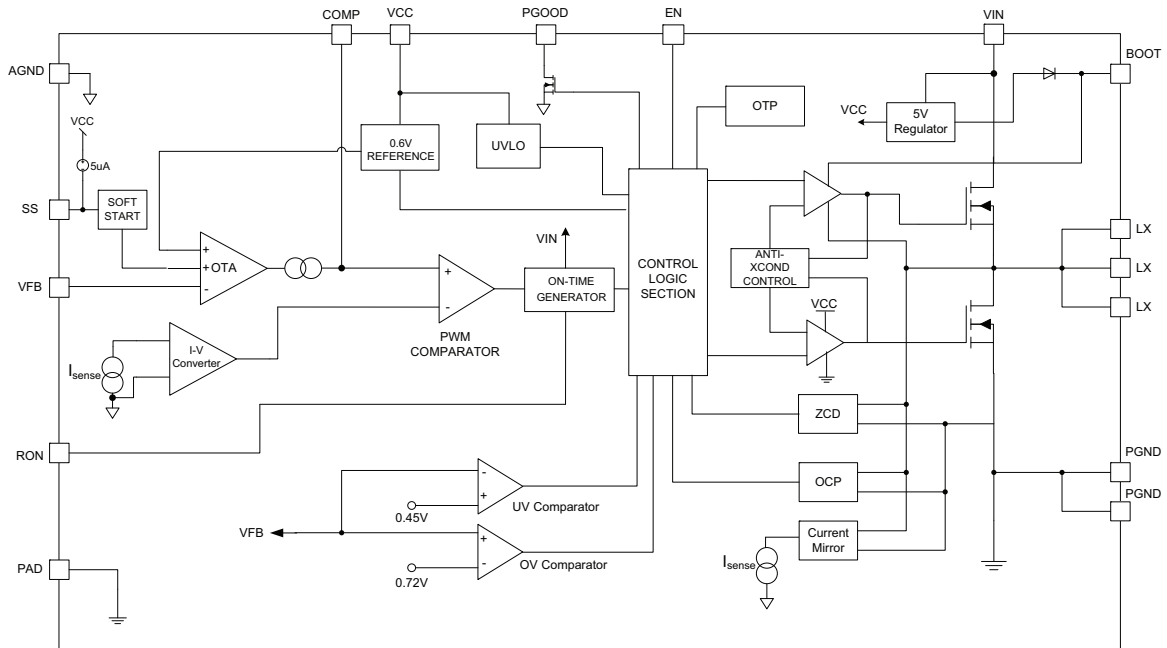


<b>RECOMMENDED OPERATING RANGE</b> (all voltages referenced to GND = 0 V)				
ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
V <sub>IN</sub>	4.5	-	15	V
V <sub>CC</sub>	4.5	-	5.5	
LX	-1	-	15	
V <sub>OUT</sub>	0.6	-	5.5	
<b>TEMPERATURE</b>				
Recommended Ambient Temperature	-40 to 85			°C
Operating Junction Temperature	-40 to 125			

<b>ELECTRICAL SPECIFICATIONS</b> (test condition unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITION V <sub>IN</sub> = 12 V, T <sub>A</sub> = -40 °C to 85 °C	LIMITS			UNIT
			MIN.	TYP.	MAX.	
<b>POWER SUPPLY</b>						
Power Input Voltage Range	V <sub>IN</sub>	Note 1	4.5	-	15	V
V <sub>CC</sub> Regulator Voltage	V <sub>CC</sub>		4.5	5	5.5	
Input Current	I <sub>IN_NOLOAD</sub>	T <sub>A</sub> = 25 °C, R <sub>on</sub> = 75 kΩ, Non-switching, I <sub>O</sub> = 0 A	-	1.2	-	mA
Shutdown Current	I <sub>IN_SHDN</sub>	EN = 0 V	-	5	8	μA
V <sub>CC</sub> UVLO Threshold	V <sub>CC_UVLO</sub>	V <sub>CC</sub> rising	2.3	2.55	2.8	V
V <sub>CC</sub> UVLO Hysteresis	V <sub>CC_UVLO_HYS</sub>		-	300	-	mV
<b>CONTROLLER AND TIMING</b>						
Feedback Reference	V <sub>FB</sub>	T <sub>A</sub> = 25 °C	0.596	0.600	0.604	V
		T <sub>A</sub> = -40 °C to +85 °C	0.594	0.600	0.606	
V <sub>FB</sub> Input Bias Current	I <sub>FB</sub>		-	2	200	nA
Transconductance	g <sub>m</sub>		-	1	-	mS
COMP Source Current	I <sub>COMP_SOURCE</sub>		-	50	-	μA
COMP Sink Current	I <sub>COMP_SINK</sub>		-	50	-	
On-Time	t <sub>ON</sub>	R <sub>on</sub> = 75 kΩ	100	135	170	ns
Minimum Off-Time	t <sub>OFF_MIN.</sub>		145	200	255	
Soft Start Current	I <sub>SS</sub>		3	5	7	μA
<b>POWER MOSFETS</b>						
High-Side On Resistance	R <sub>ON_HS</sub>	V <sub>GS</sub> = 5 V	-	45	67	mΩ
Low-Side On Resistance	R <sub>ON_LS</sub>		-	27	41	
<b>FAULT PROTECTIONS</b>						
Over Current Limit	I <sub>OCP</sub>	Inductor valley current	4	5	6	A
Output OVP Threshold	V <sub>FB_OVP</sub>	V <sub>FB</sub> with respect to 0.6 V reference	-	21	-	%
Output UVP Threshold	V <sub>FB_UVP</sub>		-	-65	-	
Over Temperature Protection		Rising temperature	-	160	-	°C
		Hysteresis	-	35	-	
<b>POWER GOOD</b>						
Power Good Output Threshold	V <sub>FB_RISING_VTH_OV</sub>	V <sub>FB</sub> rising above 0.6 V reference	-	21	-	%
	V <sub>FB_FALLING_VTH_UV</sub>	V <sub>FB</sub> falling below 0.6 V reference	-	-12.5	-	
Power Good On Resistance	R <sub>ON_PGOOD</sub>		-	30	60	Ω
Power Good Delay Time	t <sub>DLY_PGOOD</sub>		-	5	-	μs
<b>ENABLE THRESHOLD</b>						
Logic High Level	V <sub>EN_H</sub>		1.5	-	-	V
Logic Low Level	V <sub>EN_L</sub>		-	-	0.4	

**Note**(1) Tie V<sub>CC</sub> to V<sub>IN</sub> when V<sub>IN</sub> is < 5.5 V.

**FUNCTIONAL BLOCK DIAGRAM**



**Fig. 2 - SiP12109 Functional Block Diagram**

## PIN CONFIGURATION

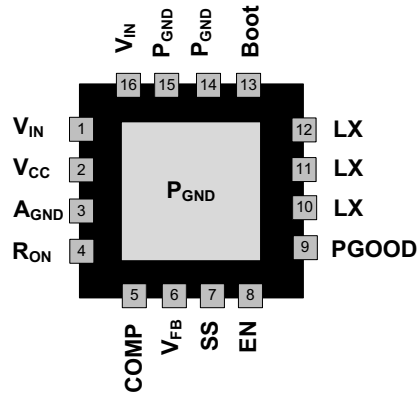
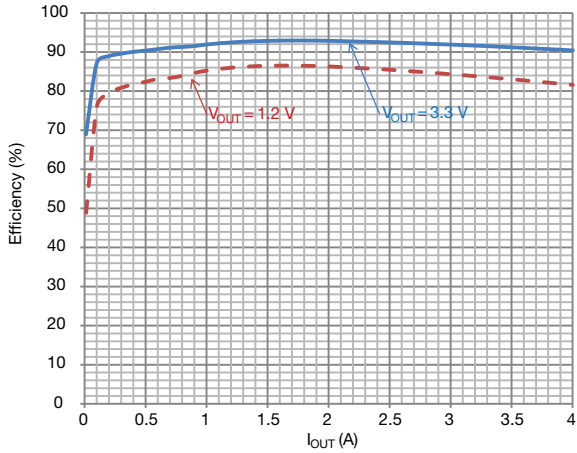


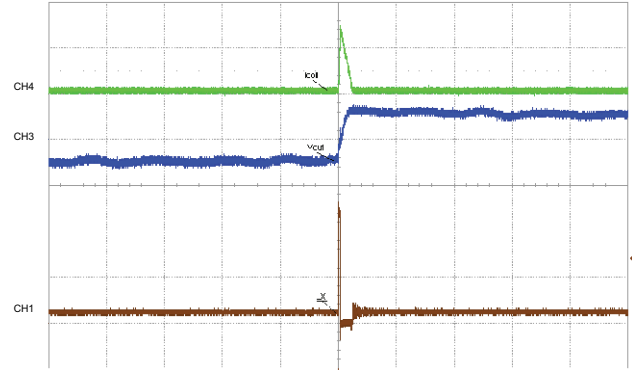
Fig. 3 - SiP12109 Pin Configuration (Top View)

PIN CONFIGURATION		
PIN NUMBER	NAME	FUNCTION
1, 16	$V_{IN}$	Input supply voltage for power MOS. $V_{IN} = 4.5\text{ V to }15\text{ V}$
2	$V_{CC}$	Internal regulator output, tie $V_{CC}$ to $V_{IN}$ when $V_{IN}$ is $< 5.5\text{ V}$
3	$A_{GND}$	Analog ground
4	$R_{ON}$	An external resistor between $R_{ON}$ and $A_{GND}$ sets the switching on time.
5	COMP	Connect to an external RC network for loop compensation and droop function.
6	$V_{FB}$	Feedback voltage. $0.6\text{ V (typ.)}$ . Use a resistor divider between $V_{OUT}$ and $A_{GND}$ to set the output voltage.
7	SS	An external capacitor between SS and $A_{GND}$ sets the soft start time.
8	EN	Enable pin. Pull enable above $1.5\text{ V}$ to enable and below $0.4\text{ V}$ to disable the part. Do not float this pin.
9	$P_{GOOD}$	Power good output. Open drain.
10, 11, 12	LX	Switching node, inductor connection point
13	BOOT	Bootstrap pin - connect a capacitor of at least $100\text{ nF}$ from BOOT to LX to develop the floating supply for the high-side gate drive.
14, 15, PAD	$P_{GND}$	Power ground

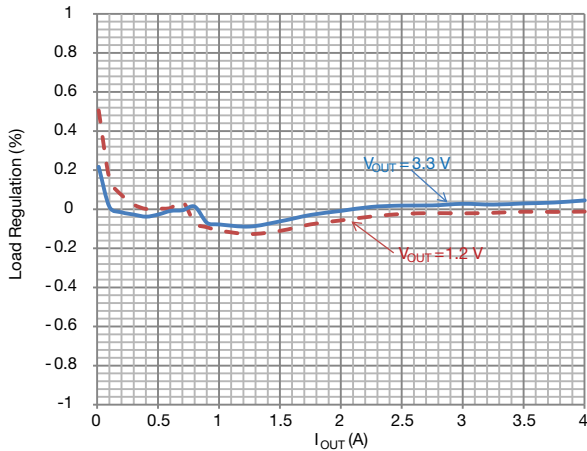
**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $F_{SW} = 1\text{ MHz}$ ,  $L_0 = 1\ \mu\text{H}$ ,  $C_0 = 3 \times 22\ \mu\text{F}$ , unless noted otherwise)



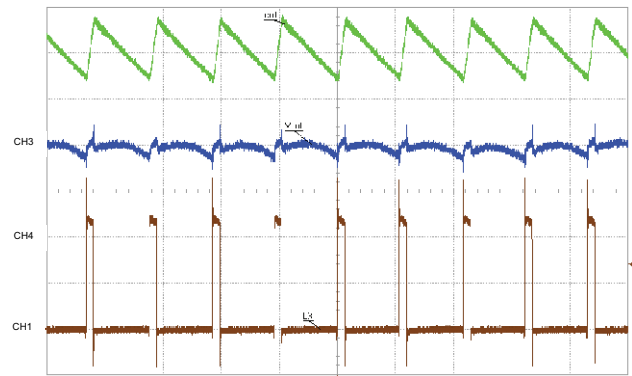
**Fig. 4 - Efficiency vs.  $I_{OUT}$**



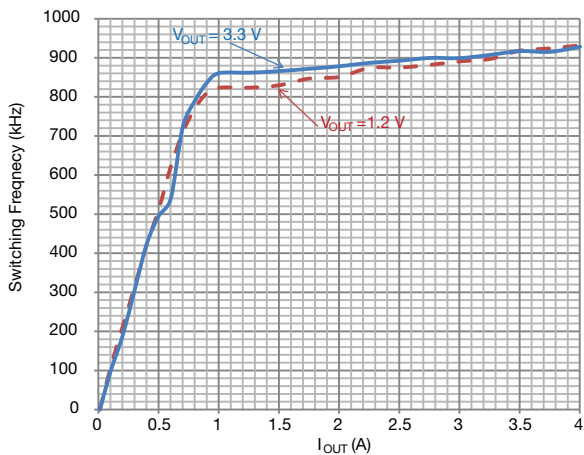
**Fig. 7 - Steady-State,  $I_{OUT} = 0\text{ A}$   
CH1 (BRN) = LX (5 V/div), CH3 (BLU) =  $V_{OUT}$  (20 mV/div),  
CH4 (GRN) =  $I_{COIL}$  (1 A/div), Time = 5  $\mu\text{s}/\text{div}$**



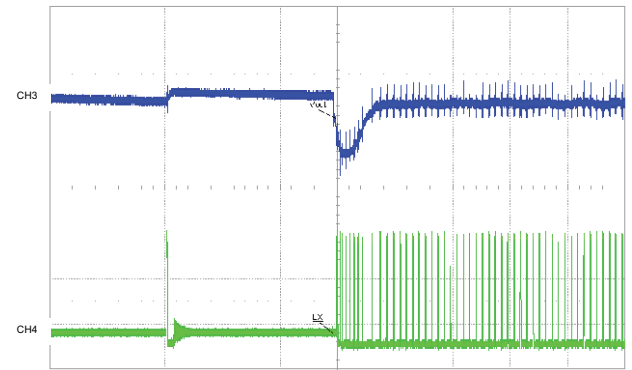
**Fig. 5 - Load Regulation vs.  $I_{OUT}$**



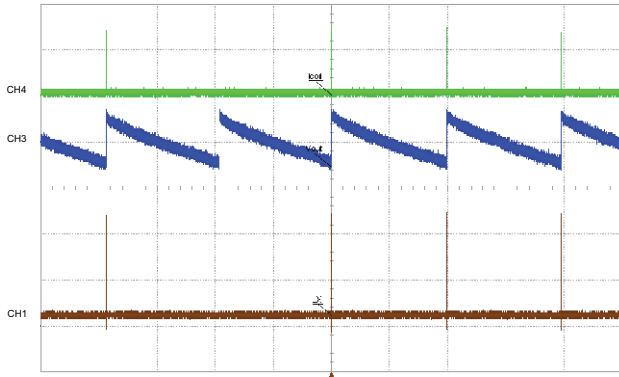
**Fig. 8 - Steady-State,  $I_{OUT} = 4\text{ A}$   
CH1 (BRN) = LX (5 V/div), CH3 (BLU) =  $V_{OUT}$  (20 mV/div),  
CH4 (GRN) =  $I_{COIL}$  (1 A/div), Time = 1  $\mu\text{s}/\text{div}$**



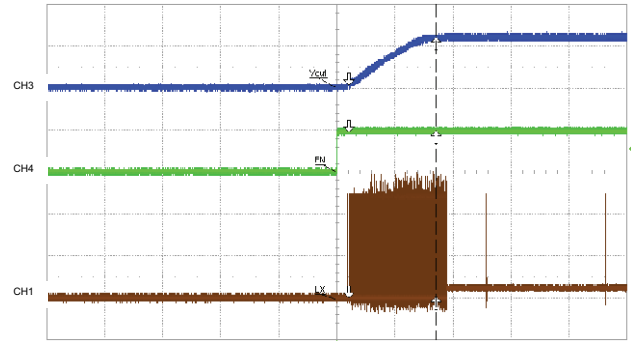
**Fig. 6 - Frequency Variation vs.  $I_{OUT}$**



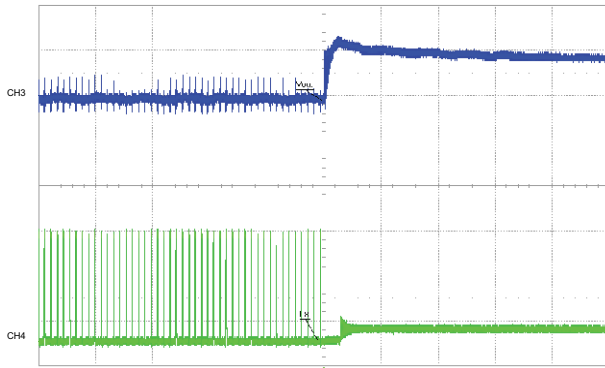
**Fig. 9 - Load Step Undershoot Response,  $I_{OUT} = 0\text{ A}$  to 4 A  
CH3 (BLU) =  $V_{OUT}$  (100 mV/div),  
CH4 (GRN) = LX (5 V/div), Time = 10  $\mu\text{s}/\text{div}$**



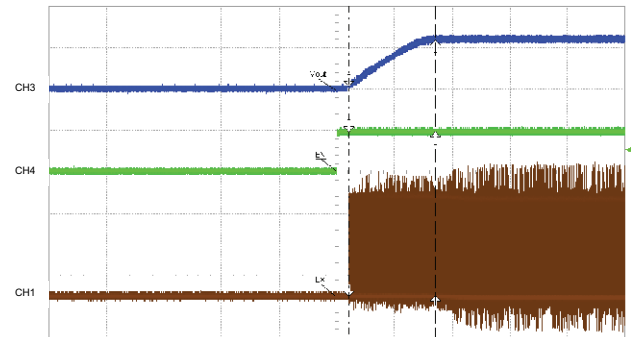
**Fig. 10 - Steady-State,  $I_{OUT} = 0$  A**  
 CH1 (BRN) = LX (5 V/div), CH3 (BLU) =  $V_{OUT}$  (20 mV/div),  
 CH4 (GRN) =  $I_{COIL}$  (1 A/div), Time = 5 ms/div



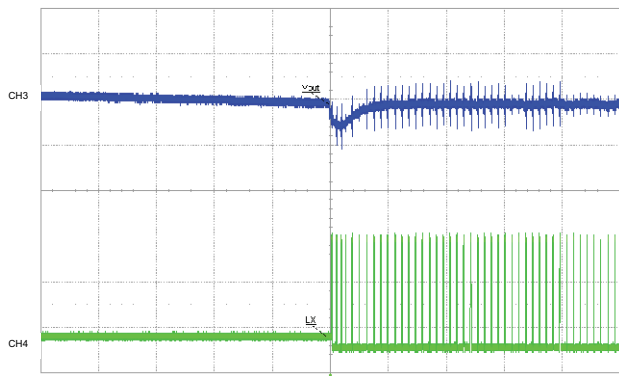
**Fig. 13 - Start-Up,  $I_{OUT} = 0$  A**  
 CH1 (BRN) = LX (5 V/div), CH3 (BLU) =  $V_{OUT}$  (1 V/div),  
 CH4 (GRN) = EN (5 V/div), Time = 1 ms/div



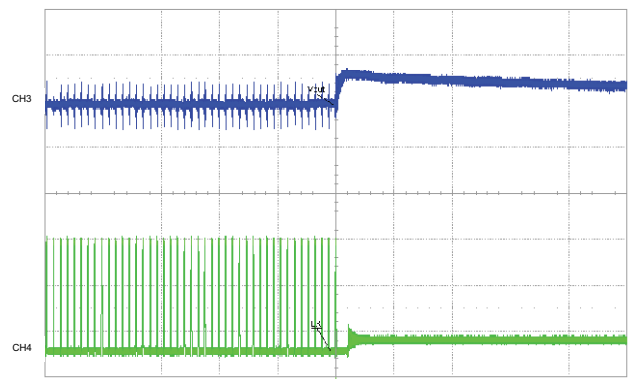
**Fig. 11 - Load Step Overshoot Response,  $I_{OUT} = 4$  A to 0 A**  
 CH3 (BLU) =  $V_{OUT}$  (100 mV/div),  
 CH4 (GRN) = LX (5 V/div), Time = 10  $\mu$ s/div



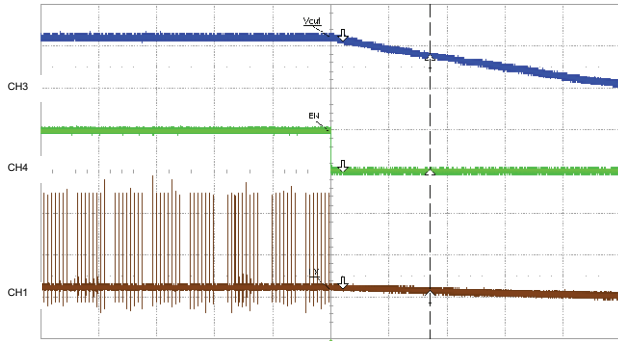
**Fig. 14 - Start-Up,  $I_{OUT} = 4$  A**  
 CH1 (BRN) = LX (5 V/div), CH3 (BLU) =  $V_{OUT}$  (1 V/div),  
 CH4 (GRN) = EN (5 V/div), Time = 1 ms/div



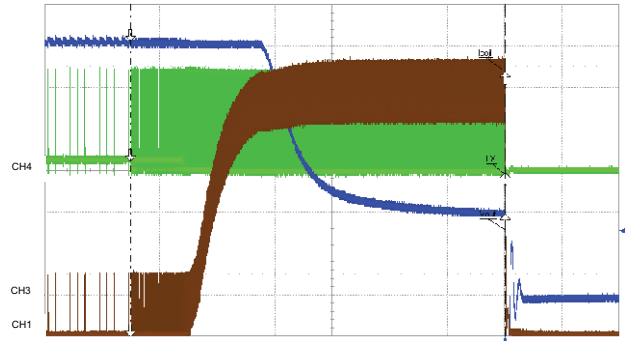
**Fig. 12 - Load Step Undershoot Response,  $I_{OUT} = 0$  A to 2 A**  
 CH3 (BLU) =  $V_{OUT}$  (100 mV/div),  
 CH4 (GRN) = LX (5 V/div), Time = 10  $\mu$ s/div



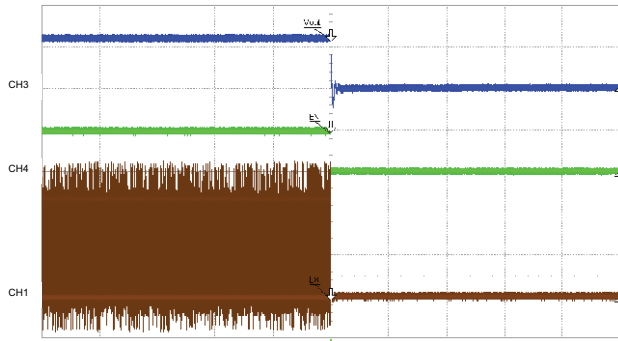
**Fig. 15 - Load Step Overshoot Response,  $I_{OUT} = 2$  A to 0 A**  
 CH3 (BLU) =  $V_{OUT}$  (100 mV/div),  
 CH4 (GRN) = LX (5 V/div), Time = 10  $\mu$ s/div



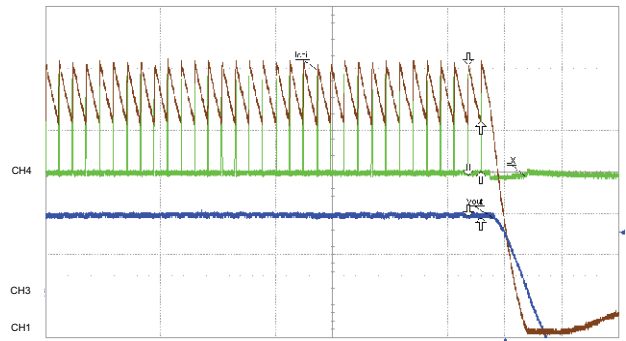
**Fig. 16 - Shut-Down,  $I_{OUT} = 0$  A**  
CH1 (BRN) = LX (5 V/div), CH3 (BLU) =  $V_{OUT}$  (1 V/div),  
CH4 (GRN) = EN (5 V/div), Time = 1 ms/div



**Fig. 18 - Over Current Protection,  $I_{OUT} = 5.9$  A;  $I_{VALLEY} = 5.2$  A**  
CH1 (BRN) =  $I_{COIL}$  (1 A/div), CH3 (BLU) =  $V_{OUT}$  (200 mV/div),  
CH4 (GRN) = LX (5 V/div), Time = 500  $\mu$ s/div



**Fig. 17 - Shut-Down,  $I_{OUT} = 4$  A**  
CH1 (BRN) = LX (5 V/div), CH3 (BLU) =  $V_{OUT}$  (1 V/div),  
CH4 (GRN) = EN (5 V/div), Time = 1 ms/div



**Fig. 19 - Over Current Protection,  $I_{OUT} = 5.9$  A;  $I_{VALLEY} = 5.2$  A**  
CH1 (BRN) =  $I_{COIL}$  (1 A/div), CH3 (BLU) =  $V_{OUT}$  (200 mV/div),  
CH4 (GRN) = LX (5 V/div), Time = 10  $\mu$ s/div



## OPERATIONAL DESCRIPTION

### Device Overview

SiP12109 is a high-efficiency monolithic synchronous buck regulator capable of delivering up to 4 A continuous current. The device has programmable switching frequency up to 1.5 MHz. The control scheme is based on current-mode constant-on-time architecture, which delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high-ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature by enabling diode emulation mode and frequency foldback as load decreases.

SiP12109 has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output

This device is available in QFN16 3x3 package to deliver high power density and minimize PCB area.

### Power Stage

SiP12109 integrates a high-performance power stage with a  $\sim 45 \text{ m}\Omega$  high side n-channel MOSFET and a  $\sim 27 \text{ m}\Omega$  low side n-channel MOSFET. The MOSFETs are optimized to achieve 95 % efficiency at up to 1.5 MHz switching frequency.

The power input voltage ( $V_{IN}$ ) can go up to 15 V and down as low as 4.5 V for the power conversion. The logic bias voltage ( $V_{CC}$ ) ranges from 4.5 V to 5.5 V.

### PWM Control Mechanism

SiP12109 employs a state-of-the-art current-mode COT control mechanism. During steady-state operation, output voltage is compared with internal reference (0.6 V typ.) and the amplified error signal ( $V_{COMP}$ ) is generated on the COMP pin. In the meantime, inductor valley current is sensed, and its slope ( $I_{sense}$ ) is converted into a voltage signal ( $V_{current}$ ) to be compared with  $V_{COMP}$ . Once  $V_{current}$  is lower than  $V_{COMP}$ , a single shot on-time is generated for a fixed time programmed by the external  $R_{ON}$ . Figure 20 illustrates the basic block diagram for CM-COT architecture and figure 21 demonstrates the basic operational principle:

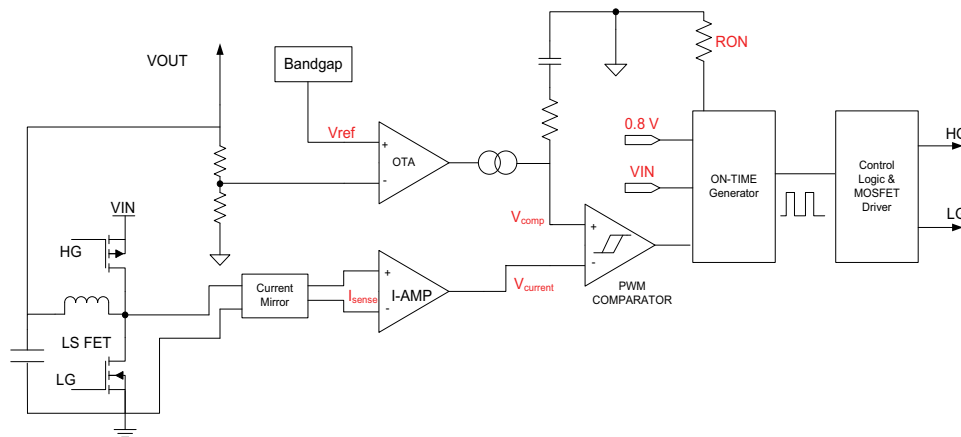
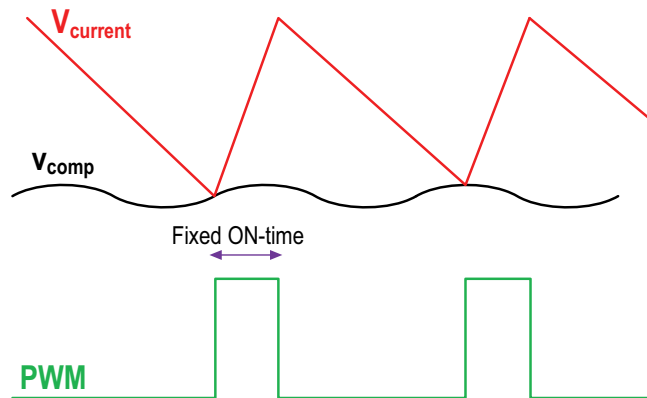


Fig. 20 - CM-COT Block Diagram


**Fig. 21 - CM-COT Operational Principle**

The following equation illustrates the relationship between on-time,  $V_{IN}$ ,  $V_{OUT}$  and  $R_{ON}$  value:

$$T_{ON} = R_{ON} \times K \times \frac{1}{V_{IN}}, \text{ where } K = 17.5 \times 10^{-12} \text{ is a constant set internally}$$

Once on-time is set, the pseudo constant frequency is then determined by the following equation:

$$f_{SW} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{\frac{1}{V_{IN}} \times R_{ON} \times K} = \frac{V_{OUT}}{R_{ON} \times K}$$

### Loop Stability and Compensator Design

Due to the nature of current mode control, a simple RC network (type II compensator) is required between COMP and  $A_{GND}$  for loop stability and transient response purpose. The general concept of this loop design is to introduce a single zero through the compensator to determine the crossover frequency of overall close loop system.

The overall loop can be broken down into following segments.

Output feedback divider transfer function  $H_{fbZ}$ :

$$H_{fb} = \frac{R_{fb2}}{R_{fb1} \times R_{fb2}}$$

Voltage compensator transfer function  $G_{COMP}$  (s):

$$G_{COMP}(s) = \frac{R_O \times (1 + sC_{COMP}R_{COMP})}{(1 + sR_OC_{COMP})} gm$$

Modulator transfer function  $H_{mod}$  (s):

$$H_{mod}(s) = \frac{1}{AV_1 \times R_{DS(on)}} \times \frac{R_{load} \times (1 + sC_O R_{ESR})}{(1 + sC_O R_{load})}$$

The complete loop transfer function is given by:

$$H_{mod}(s) = \frac{R_{fb2}}{R_{fb1} \times R_{fb2}} \times \frac{R_O \times (1 + sC_{COMP}R_{COMP})}{(1 + sR_OC_{COMP})} gm \times \frac{1}{AV_1 \times R_{DS(on)}} \times \frac{R_{load} \times (1 + sC_O R_{ESR})}{(1 + sC_O R_{load})}$$

#### When:

$C_{COMP}$  = Compensation capacitor

$R_{COMP}$  = Compensation resistor

$gm$  = Error amplifier transconductance

$R_{load}$  = Load resistance

$C_O$  = Output capacitor

$R_{DS(on)}$  = LS switch resistance

$R_{fb1}$  = Feedback resistor connect to LX

$R_{fb2}$  = Feedback resistor connect to ground

$R_O$  = Output impedance of error amplifier = 20 M $\Omega$

$AV_1$  = Voltage to current gain = 3

**Light Load Operation**

To further improve efficiency at light-load condition, SiP12109 provides a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal Zero Crossing Detector (ZCD) monitors LX node voltage to determine when inductor current starts to flow negatively. In light load operation as soon as inductor valley current crosses zero, the device first deploys diode

emulation mode by turning off LS FET. If load further decreases, switching frequency is further reduced proportional to load condition to save switching losses while keeping output ripple within tolerance. The switching frequency is set by the controller to maintain regulation. At zero load this frequency can go as low as hundreds of Hz.

**OUTPUT MONITORING AND PROTECTION FEATURES**

**Output Over-Current Protection (OCP)**

SiP12109 has pulse-by-pulse over-current limit control. The inductor valley current is monitored during LS FET turn-on period through  $R_{DS(on)}$  sensing. After a pre-defined time, the valley current is compared with internal threshold (5 A typ.) to determine the threshold for OCP. If monitored current is higher than threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

In the severe over-current condition, pulse-by-pulse current limit eventually triggers output under-voltage protection (UVP), which latches the device off to prevent catastrophic thermal-related failure. UVP is described in the next section.

OCP is enabled immediately after  $V_{CC}$  passes UVLO level.

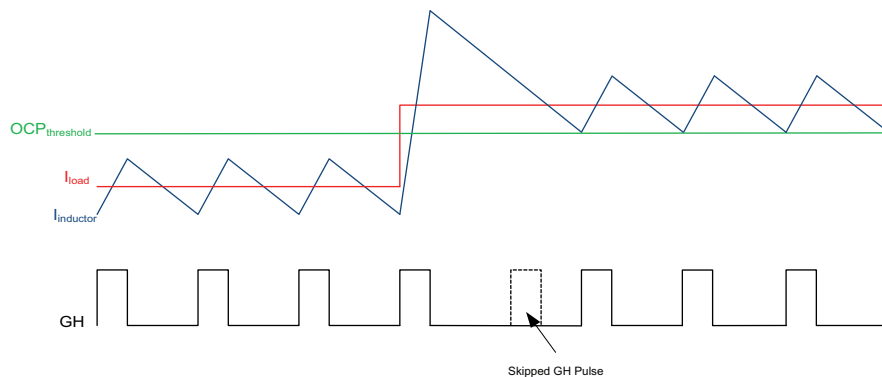


Fig. 22 - Over-Current Protection Illustration

**Output Under-Voltage Protection (UVP)**

UVP is implemented by monitoring output through  $V_{FB}$  pin. Once the voltage level at  $V_{FB}$  is below 0.2 V for more than 20  $\mu$ s, then UVP event is recognized and both HS and LS MOSFETs are turned off. UVP latches the device off until either  $V_{CC}$  or EN is recycled.

UVP is only active after the completion of soft-start sequence.

**Output Over-Voltage Protection (OVP)**

For OVP implementation, output is monitored through  $V_{FB}$  pin. After soft-start, if the voltage level at  $V_{FB}$  is above 21 % (typ.), OVP is triggered with HS FET turning off and LS FET turning on immediately to discharge the output. Normal operation is resumed once  $V_{FB}$  drops back to 0.675 V.

OVP is active immediately after  $V_{CC}$  passes UVLO level.

**Over-Temperature Protection (OTP)**

SiP12109 has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 160  $^{\circ}$ C (typ.). A hysteresis of 30  $^{\circ}$ C is implemented, so when junction temperature drops below 130  $^{\circ}$ C, the device restarts by initiating the soft-start sequence again.

**Soft Start up**

SiP12109 soft-start time is adjustable by selecting a capacitor value from the following equation. Once  $V_{CC}$  is above UVLO level (2.55 V typ.),  $V_{OUT}$  will ramp up slowly, rising monotonically to the programmed output voltage. There is an internal 5  $\mu$ A current source tied to the soft start pin which charges the external soft start cap

$$SS \text{ time} = \frac{C_{ext} \times 0.8 \text{ V}}{5 \mu\text{A}}$$

During soft-start period, OCP is activated. OVP and short-circuit protection are not active until soft-start is complete.

**Pre-bias Startup**

In case of pre-bias startup, output is monitored through  $V_{FB}$  pin. If the sensed voltage on  $V_{FB}$  is higher than the internal reference ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.

**Power Good (PGOOD)**

SiP12109's Power Good is an open-drain output. Pull PGOOD pin high up to 5 V through a 10K resistor to use this signal. Power good window is shown in the below diagram. If voltage level on  $V_{FB}$  pin is out of this window, PGOOD signal is de-asserted by pulling down to GND.

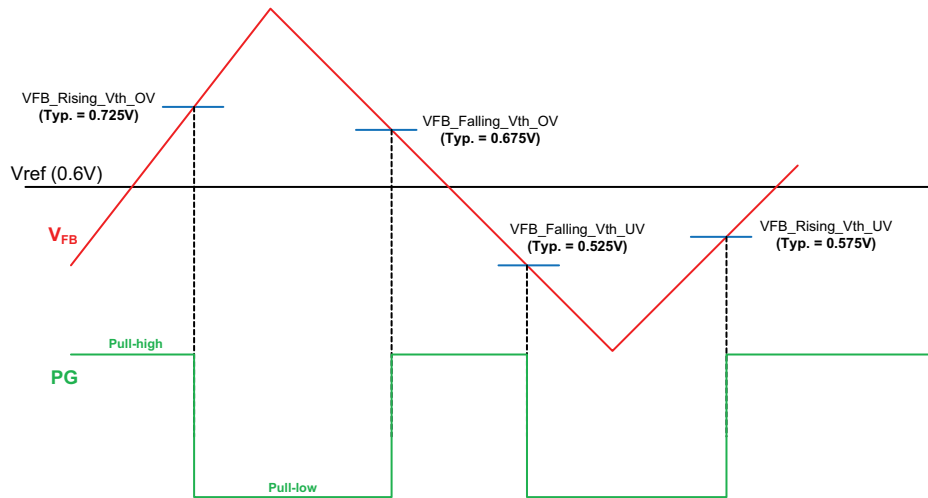


Fig. 23 - PGOOD Window and Timing Diagram



BILL of MATERIAL							
ITEM	QTY	REFERENCE	VALUE	VOLTAGE	FOOTPRINT	PART NUMBER	MANUFACTURER
1	3	C1, C5, C6	0.1 $\mu$ F	35 V	C0402-TDK	GMK105BJ104KV-F	Taiyo Yuden
2	2	C2, C3	22 $\mu$ F	10 V	C0805-TDK	LMK212BJ226MG-T	Taiyo Yuden
3	1	C4	22 $\mu$ F	35 V	C0805-TDK	C2012X5R1V226M125AC	TDK
4	1	C7	2.2 $\mu$ F	16 V	C0603-TDK	C0603C225K4PACTU	Kemet
5	1	C8	10 nF	16 V	C0402-TDK	CC0402KRX7R7BB103	Yageo
6	1	C9	0.47 nF	50 V	C0402-TDK	C1005C0G1H471J050BA	TDK
7	1	IC1	SiP12109	-	QFN16 3 x 3	SiP12109DMP-T1-GE4	Vishay
8	6	J1, J2, J3, J4, J5, J6	V <sub>IN</sub> , V <sub>OUT</sub> , V <sub>O_GND</sub> , V <sub>IN_GND</sub> , EN, PGD	-	TP30	2108-2-00-44-00-00-07	Mill-Max
9	1	L1	1 $\mu$ H	-	IHLP1616	IHLP1616BZER1R0M11	Vishay
10	1	R1	75k	-	R0402-Vishay	CRCW040275K0FKEDHP	Vishay
11	1	R2	0	-	R0402-Vishay	RCG04020000Z0ED	Vishay
12	1	R3	6.04k	-	R0402-Vishay	CRCW04026K04FKED	Vishay
13	2	R4, R5	100k	-	R0402-Vishay	CRCW0402100KFKED	Vishay
14	2	R6, R7	5k11	-	R0402-Vishay	CRCW04025K11FKED	Vishay

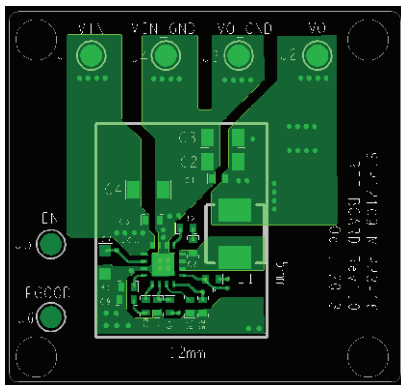
**PCB LAYOUT OF REFERENCE BOARD**


Fig. 25 - Top Layer

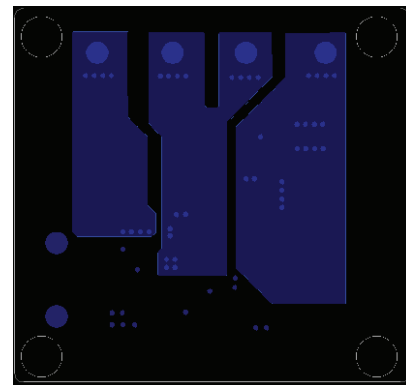


Fig. 27 - Bottom Layer

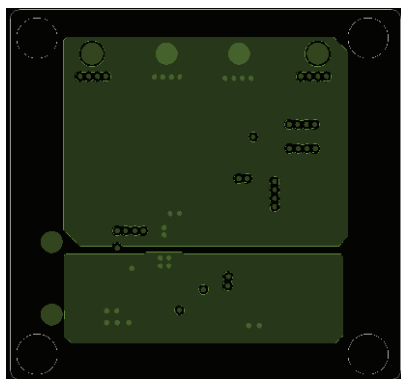


Fig. 26 - Inner Layer1

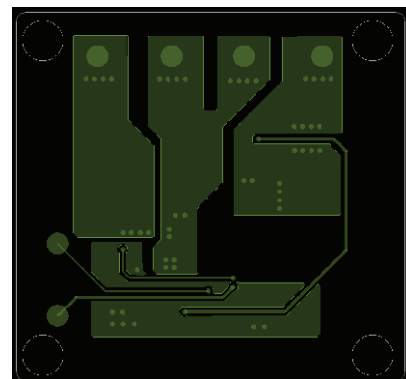
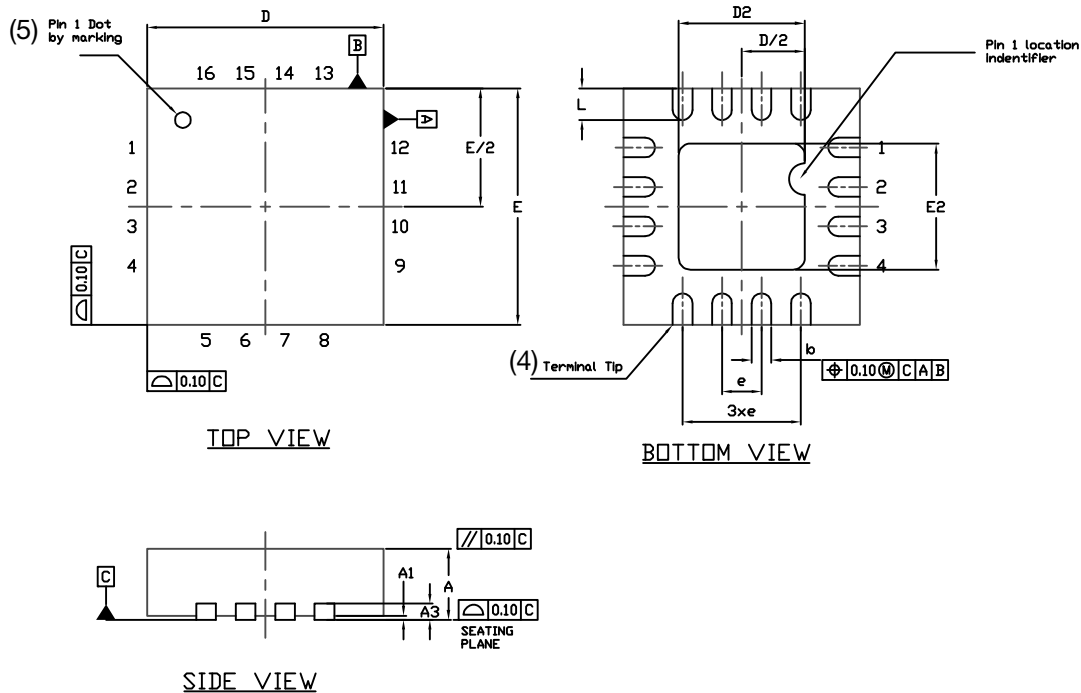


Fig. 28 - Inner Layer2

**CASE OUTLINE**


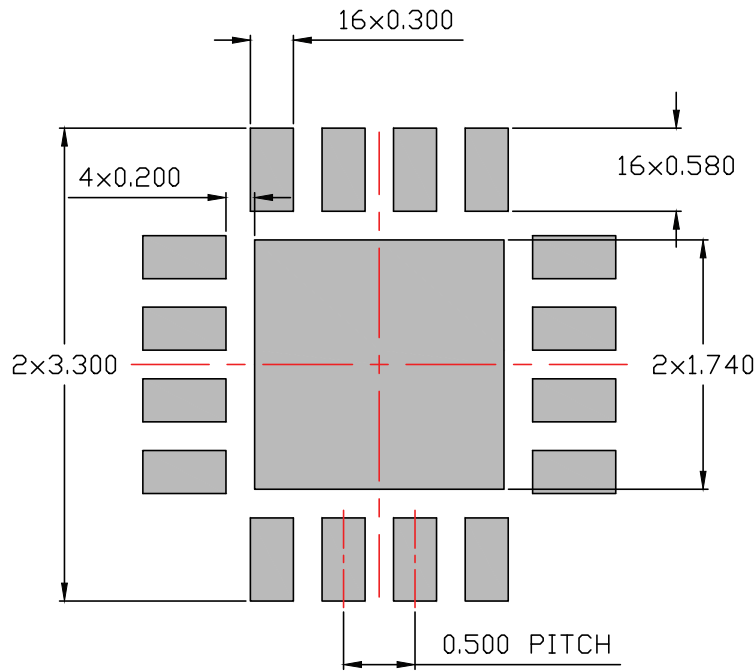
DIMENSION	MILLIMETERS <sup>(1)</sup>			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	3.00 BSC			0.118 BSC		
D2	1.5	1.6	1.7	0.059	0.063	0.067
e	0.50 BSC			0.020 BSC		
E	3.00 BSC			0.118 BSC		
E2	1.5	1.6	1.7	0.059	0.063	0.067
L	0.3	0.4	0.5	0.012	0.016	0.020
N <sup>(3)</sup>	16			16		
Nd <sup>(3)</sup>	4			4		
Ne <sup>(3)</sup>	4			4		

**Notes**

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.



**RECOMMENDED LAND PATTERN FOR QFN16 3 mm x 3 mm**



**DIMENSION ARE IN MILLIMETERS**

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