

## S Series Power MOSFET

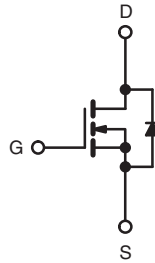
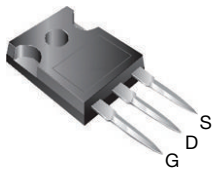
PRODUCT SUMMARY		
$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V	0.07
$Q_g$ max. (nC)	216	
$Q_{gs}$ (nC)	39	
$Q_{gd}$ (nC)	57	
Configuration	Single	

### FEATURES

- Generation one
- Low figure-of-merit  $R_{on} \times Q_g$
- 100 % avalanche tested
- Ultra low gate charge
- Ultra low  $R_{on}$
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

TO-247AC



N-Channel MOSFET

### APPLICATIONS

- PFC power supply stages
- Hard switching topologies
- Solar inverters
- UPS
- Motor control
- Server telecom

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	SiHG47N60S-E3


ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	600	V
Gate-Source Voltage		$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$I_D$	$T_C = 25$ °C	47
			$T_C = 100$ °C	30
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	140	A
Linear Derating Factor			3.3	W/°C
Avalanche Energy (repetitive)		$E_{AR}$	0.42	mJ
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	1800	
Maximum Power Dissipation		$P_D$	417	W
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	°C
Drain-Source Voltage Slope	$T_J = 125$ °C	dV/dt	37	V/ns
Reverse Diode dV/dt <sup>d</sup>			8.5	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s		300	°C

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 73.5$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.3	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	0.7	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	-	4	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 1$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 24\text{ A}$	-	0.057	0.07	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 8\text{ V}, I_D = 3\text{ A}$		-	7.5	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$		-	6630	-	pF
Output Capacitance	$C_{oss}$			-	220	-	
Reverse Transfer Capacitance	$C_{rss}$			-	7	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, V_{DS} = 400\text{ V}$	-	180	216	nC
Gate-Source Charge	$Q_{gs}$			-	39	-	
Gate-Drain Charge	$Q_{gd}$			-	57	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 380\text{ V}, I_D = 47\text{ A}, R_g = 4.4\text{ }\Omega, V_{GS} = 13\text{ V}$		-	30	60	ns
Rise Time	$t_r$			-	12	25	
Turn-Off Delay Time	$t_{d(off)}$			-	115	175	
Fall Time	$t_f$			-	9	20	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$		-	0.62	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	47	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	140	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 47\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S, dI/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	750	1125	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	18	36	$\mu\text{C}$
Body Diode Reverse Recovery Current	$I_{RRM}$			-	39	80	A

**Note**

a.  $C_{oss\text{ eff.}}$  (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

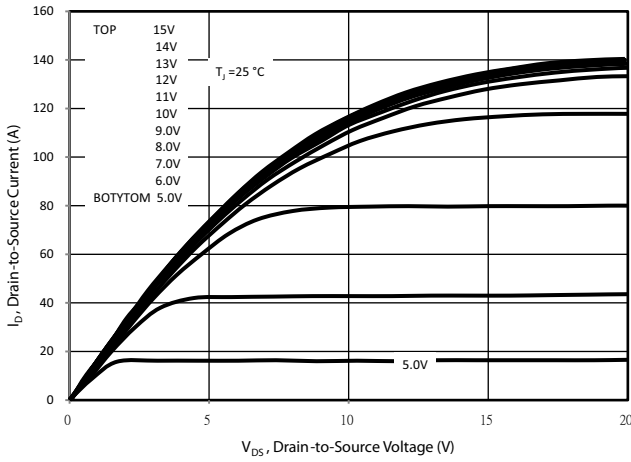


Fig. 1 - Typical Output Characteristics (TO-247)

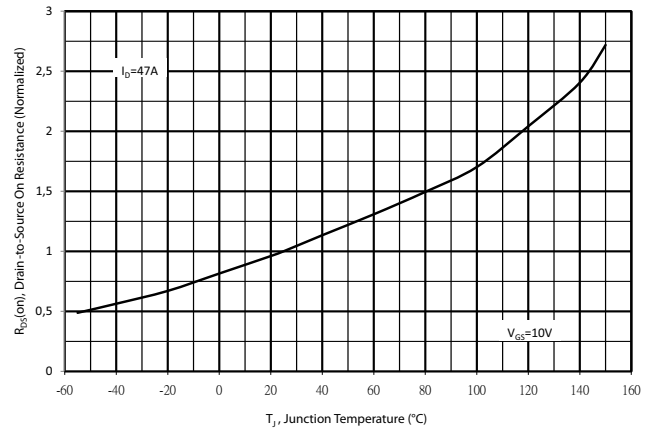


Fig. 4 - Normalized On-Resistance vs. Temperature

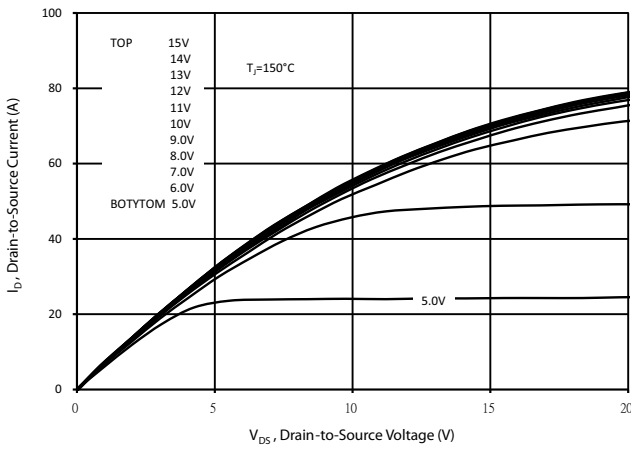


Fig. 2 - Typical Output Characteristics (TO-247)

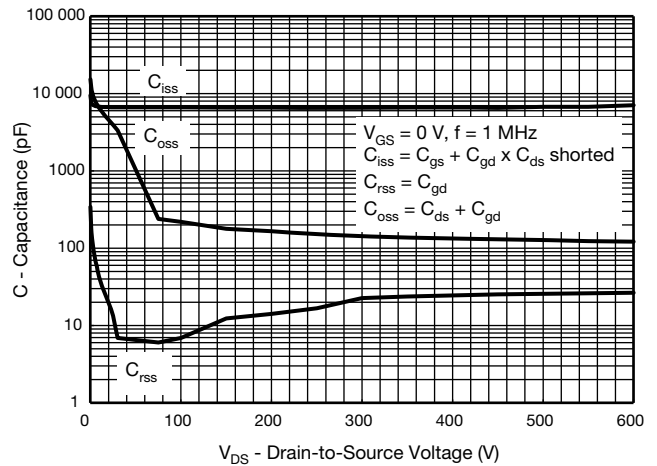


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

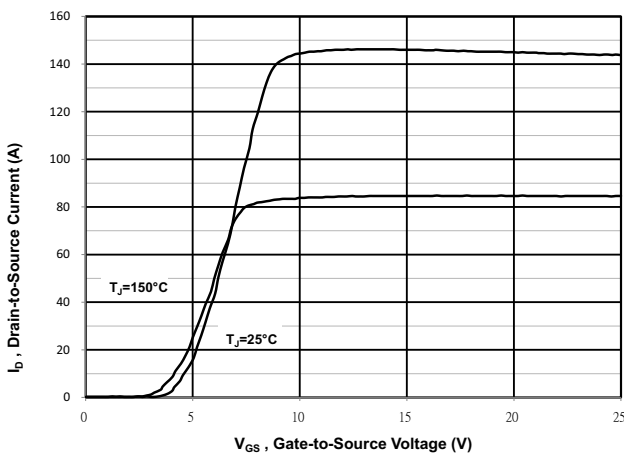


Fig. 3 - Typical Transfer Characteristics

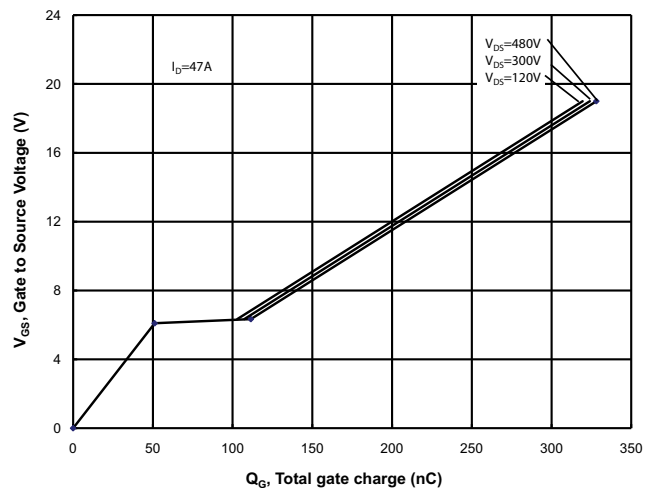


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

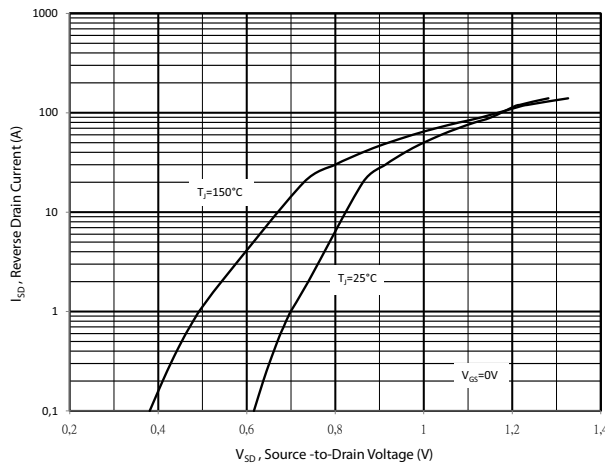


Fig. 7 - Typical Source-Drain Diode Forward Voltage

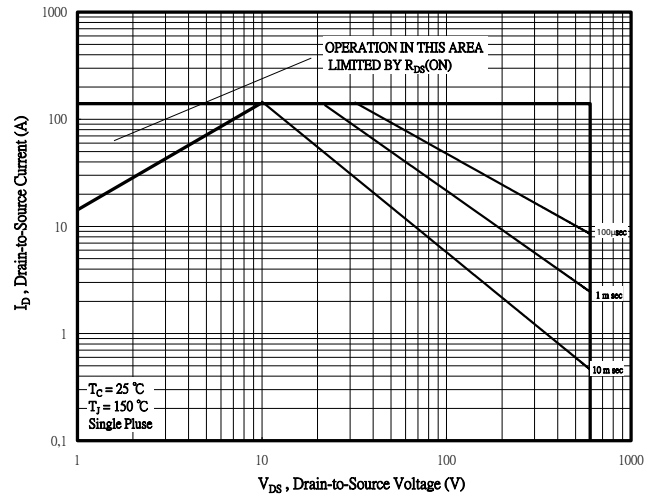


Fig. 8 - Maximum Safe Operating Area

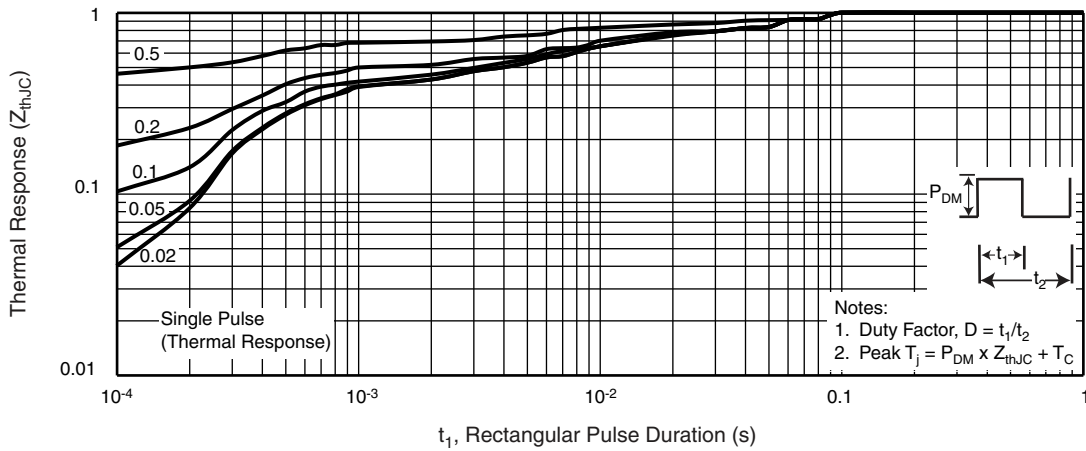


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-247AC)

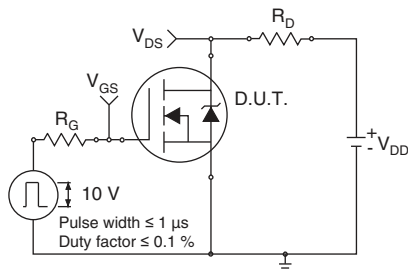


Fig. 10 - Switching Time Test Circuit

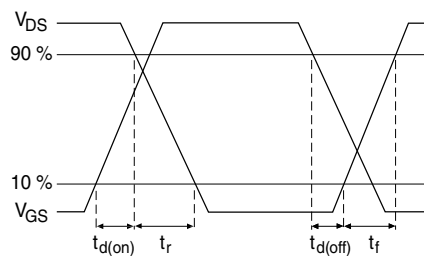


Fig. 11 - Switching Time Waveforms

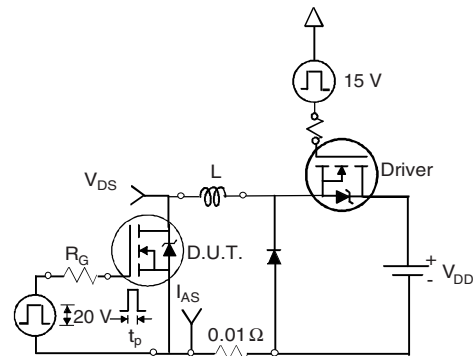
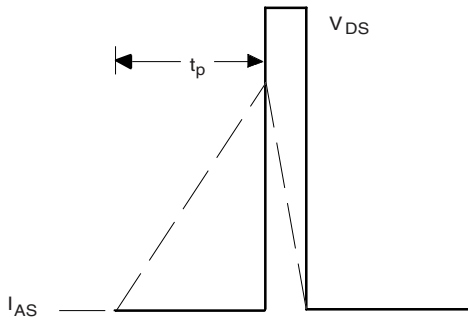
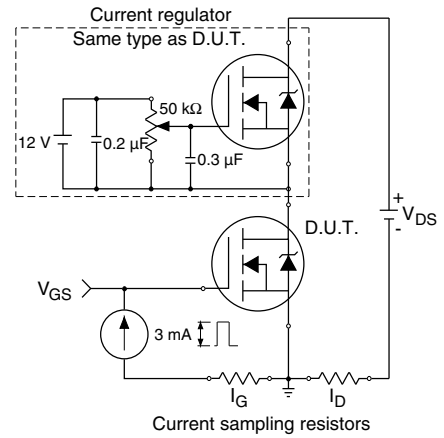


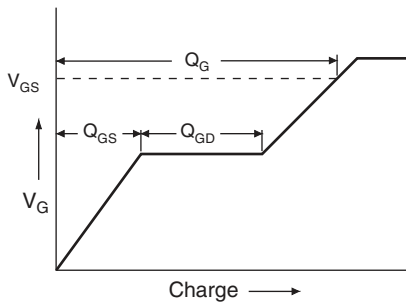
Fig. 12 - Unclamped Inductive Test Circuit



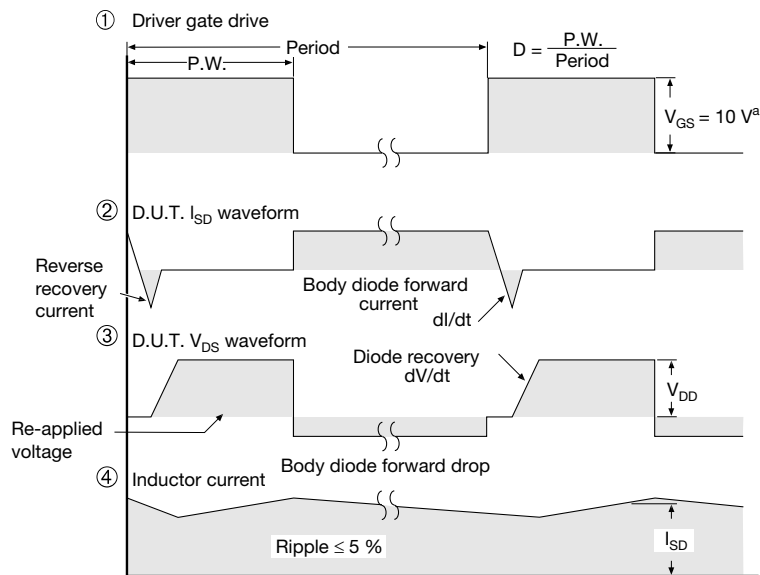
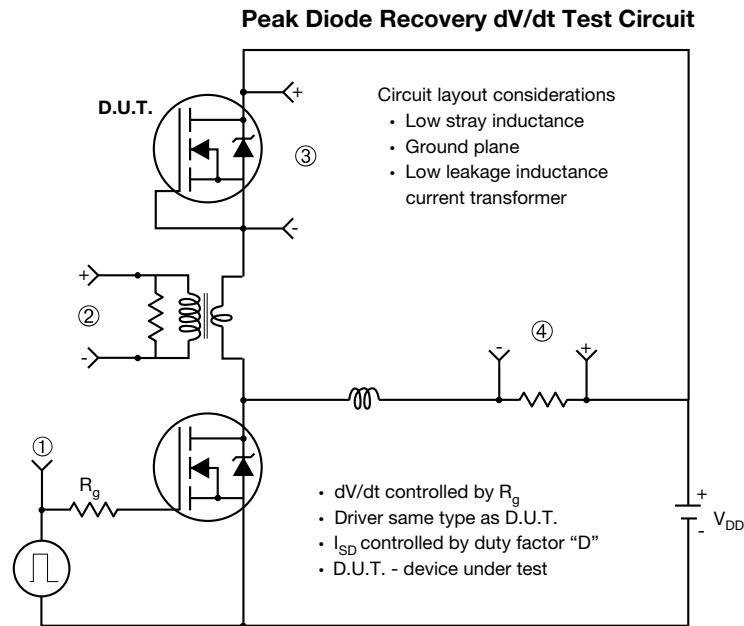
**Fig. 13 - Unclamped Inductive Waveforms**



**Fig. 15 - Gate Charge Test Circuit**



**Fig. 14 - Basic Gate Charge Waveform**



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 16 - For N-Channel**

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